Tech Notes

Digital Focal-Plane Arrays

MIT Lincoln Laboratory's digital focal-plane array technology is improving the long-range infrared capabilities of detectors used in wide-area imaging and surveillance applications.

Long-wave infrared (LWIR) imaging enables a variety of commercial and DoD applications, including nighttime surveillance, acquisition and tracking by missile seekers, and atmospheric imaging. Many of these LWIR sensing applications not only demand large-area coverage at data rates sufficient for object tracking but also must be realized in a sensor design consistent with stressing size, weight, and power (SWaP) constraints.

The Challenge for LWIR Imaging

As with modern digital photography and video recording cameras, the heart of an LWIR imaging sensor is the focal-plane array (FPA)—the device which converts an optical image into an electrical signal that can then be read out and processed and/or stored.

While visible-light-sensitive FPAs can be fabricated using the same integrated circuit (IC) materials and techniques used to produce processor and memory devices, standard IC materials are not sensitive to LWIR radiation. Thus, LWIR detectors must be fabricated using alternative materials and less-well-developed fabrication processes, resulting in devices with smaller formats, lower yields, higher pixel-to-pixel variability, and higher costs.

In the fabrication of a working LWIR FPA, the detector array must be mated to a readout integrated circuit (ROIC) that accumulates the photocurrent from each pixel and then transfers the resultant signal onto output taps for readout. Commercial and DoD communities have been exploring new LWIR detector technologies to enable larger-format, but they have given relatively little attention to ROIC improvements.

Solution: Novel ROIC Technology

Lincoln Laboratory has designed, developed, and tested LWIR ROIC technology that overcomes many performance and scaling limitations imposed by conventional ROIC technology.

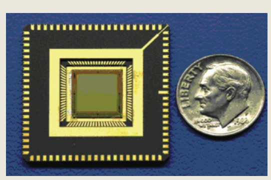
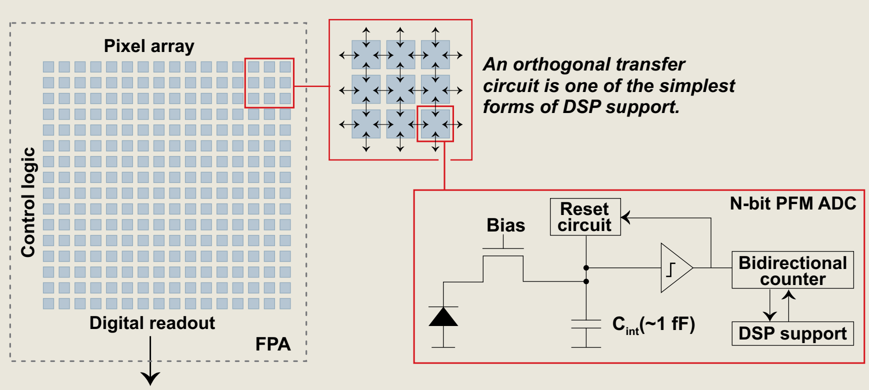


Figure 1. Lincoln Laboratory developed a 256 × 256 30 μm pitch in-pixel DFPA (upper left). Each pixel of the digital ROIC includes a full-dynamic-range analog-to-digital converter as well as local digital signal processing (DSP) support. Each pixel can transfer data to any of its four nearest neighbors (below); the entire array can be read out by using high-speed digital readout circuits.



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Conventional ROIC technology stores signal charge at each pixel and then routes the signal onto output taps for readout. This approach requires storing large signal charge at each pixel site and maintaining signal-to-noise ratio (or dynamic range) as the signal is read out and digitized.

Lincoln Laboratory's alternate approach is to digitize the detector current within each pixel by incrementing a counter each time a small charge bucket is filled; the larger the detector current, the quicker the bucket is filled and the counter incremented. Here the total charge is given by the size of the charge bucket (in electrons) times the digital value in the counter.

The in-pixel digital ROIC can leverage low-voltage, deeply scaled IC processes that enable low-power, high-component-density designs.

This approach is in stark contrast to the conventional methodology in which the signal charge is accumulated on a large integrating capacitor. (The total integrated charge must meet dynamic range needs, typically resulting in large capacitors and bias voltages as the total charge = voltage × capacitance.) In the Laboratory's approach, the counter containing the digital representation of the detector signal is connected through a multiplexor to its four nearest neighbors; high-speed serializers located on the edge of the ROIC transfer the array contents onto a set of high-speed, 2.5-billion-bits-per-second digital output taps for readout.

The relatively large voltage required across the integrating capacitor used in the conventional pixel designs is not compatible with advanced low-voltage (and thus low-power) deeply scaled IC fabrication processes that enable increased circuit density and increased on-chip processing power. Furthermore, the dynamic range requirement limits how fast data can be read out of each output tap; large-format high-data-rate applications may require an excessive number of output taps.

Implications and Future of Digital Focal-Plane Arrays

Lincoln Laboratory's up-front digitization of the detector signal has profound implications for device design and fabrication; the in-pixel digital ROIC can leverage low-voltage, deeply scaled (nanometer class) IC processes that enable low-power, high-component-density designs. Low-power, large-format, small-pixel LWIR FPAs with large dynamic, on-chip digital image processing (for SWaP-efficient sensor designs) and high-speed readout (for large-area coverage) are now possible. In addition, the potential to "package" design components (e.g., analog-to-digital converter, data transfer, high-speed readout) into libraries makes this approach amenable to rapid prototyping of new sensor concepts.

Initial risk-reduction activities demonstrated the viability of in-pixel digital FPA (DFPA) circuits and high-speed digital readout (at the cryogenic temperatures necessary for sensitive LWIR operation).[1] The relatively large pixel (60 µm square) test structures designed and fabricated using a 180 nm IC process validated the in-pixel DFPA approach.

A follow-up multiyear effort initiated in 2006 aimed to design, develop, and demonstrate full-format (256 × 256 30 µm pitch) in-pixel DFPA ROIC technology (Figure 1) using a 90 nm fabrication process for missile seeker and persistent ground-surveillance applications .[2,3,4,5] The in-pixel DFPA ROICs were hybridized to several different detectors from various organizations with detection bands spanning short-wave infrared (SWIR) to very-long-wave infrared (VLWIR). The program successfully demonstrated the following capabilities:

- Wide dynamic range
- Low read noise (~1000 electrons)
- On-chip background suppression
- High-speed data rate
- On-chip image stabilization
- On-chip spatial linear filtering (Figure 2)

Figure 2. On-chip spatial linear filtering produces an edge detection image.

- On-chip change detection
- On-chip synchronous detection of a pulsed laser in the presence of strong spatial clutter
- Near background shot-noise limited detection at low-input currents
- ~30 mW power dissipation at 100 Hz frame rate
- Successful operation with SWIR through LWIR detector arrays

Lincoln Laboratory is working on maturing in-pixel DFPA ROIC technology and developing novel DFPA-based sensors for wide-area persistent surveillance, missile seekers and fire control, and novel passive and/or active sensing applications. ■

References

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