Subwavelength Optical Lithography with Phase-Shift Photomasks

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Optical lithography has been the patterning method of choice for the semiconductor industry for over three decades. Through a continual decrease in exposure wavelength and increase in lens numerical aperture, this technology has kept pace with the exponentially shrinking feature sizes predicted by Moore's law. In the mid-1990s, minimum feature sizes on semiconductor chips began to drop below the available imaging wavelengths, ushering in the era of subwavelength optical lithography. Imaging in this challenging regime has been enabled by the development of resolution enhancement technologies (RETs) that work to overcome diffraction limits on imaging resolution. We have developed, as part of a Defense Advanced Research Projects Agency–sponsored program in advanced complementary metal-oxide semiconductor (CMOS) technology, phase-shift-photomask optical lithography processes capable of imaging features as small as 16% of the exposure wavelength. We have applied these processes to the development of advanced silicon-on-insulator (SOI) device technology utilizing standard commercial optical lithography equipment. We are also exploring methods of cost-effective implementation of this type of resolution enhancement technology for applications that require high-resolution imaging for relatively small quantities of wafers.

Optical lithography has been the patterning method of choice for the semiconductor industry for over three decades, providing a combination of resolution, cost effectiveness, and production rate that is unmatched by alternative technologies. (To learn the fundamentals of optical lithography, see the sidebar in the article entitled "Recent Trends in Optical Lithography," by Rothschild et al.) By the mid-1990s, demand for minimum feature sizes below the available exposure wavelengths ushered in the era of subwavelength optical lithography. In this challenging regime, diffraction effects can distort the pattern being imaged on the photoresist.

This article discusses resolution enhancement methods that enable optical lithography to succeed in the subwavelength regime. We focus on phase-shift-photomask methods that significantly extend resolution and overcome such diffraction limitations as the isodense-proximity effect and the spatial-frequency effect. We demonstrate how these methods can be used to fabricate highly scaled complementary metal-oxide semiconductor (CMOS) devices, emphasizing a cost-effective implementation for low-volume applications of interest to the Department of Defense.

The isodense-proximity effect, shown in Figure 1, is caused by a loss of contrast as feature pitch—the

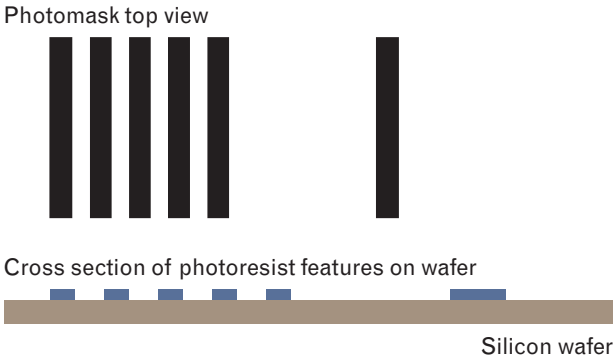


FIGURE 1. Illustration of the isodense-proximity effect. A cluster of identical features images differently in the photoresist than an isolated feature of the same size.

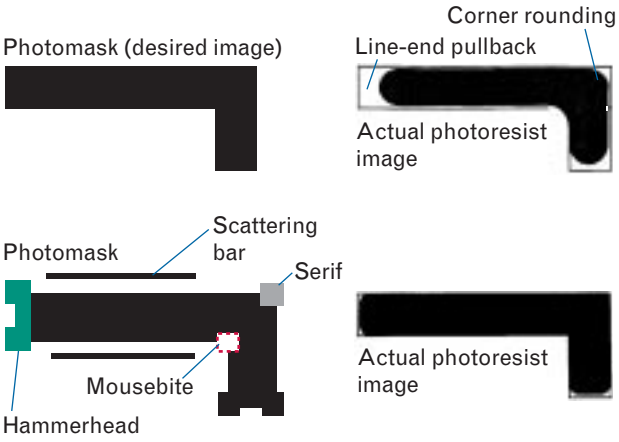


FIGURE 2. Schematic diagram of optical proximity correction. The spatial-frequency effect distorts the image patterned on the photoresist by rounding sharp corner features and shortening narrow line ends. The addition of photomask correction features such as mousebites, hammerheads, serifs, and scattering bars produces an image closer to the desired result.

length of the feature plus the distance between two adjacent features—decreases. The effect occurs when dense and isolated features of identical size on the photomask image with differing sizes on the wafer.

The spatial-frequency effect occurs because of the finite spatial bandwidth of the optical projection lens. The lens system behaves as a low-pass spatial frequency filter acting upon the photomask features; the high-order spatial frequencies are not passed by the projection lens. The image patterned on the photoresist is therefore distorted—sharp corner features are rounded (corner rounding) and narrow line ends are shortened (line-end pullback).

To compensate for these effects, the optical lithography community has developed a number of resolution enhancement technologies (RETs), including optical proximity correction, off-axis illumination, and phase-shift masks [1]. Figure 2 illustrates the optical-proximity-correction method, which involves adding correction features to the photomask, such as mousebites, hammerheads, serifs, and scattering bars, so that the pattern imaged on the photoresist more closely resembles the desired pattern. When the required feature sizes are significantly below the imaging wavelength, the correction features become more intricate and the pattern on the photomask bears little resemblance to the desired pattern on the wafer. In this case, complex correction software is utilized to design the photomask, and the photomask becomes difficult to manufacture. Despite these challenges, optical proximity correction enjoys widespread commercial use because of its effectiveness in improving the lithographic process.

Off-axis illumination uses an aperture to force the illuminating laser beam to strike the photomask at an angle with respect to the optical axis of the lithography system. This technique helps improve the imaging of dense features at a given wavelength. It is simple to implement since modern lithography sys-

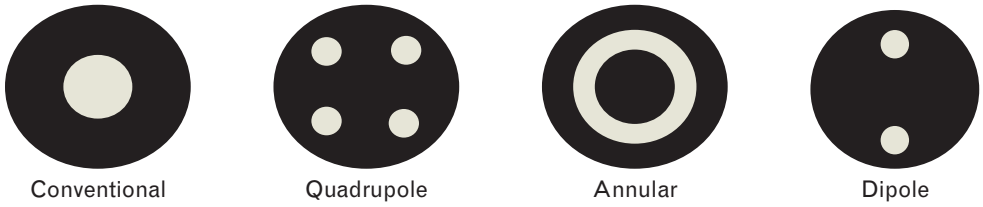


FIGURE 3. Comparison of conventional illumination source to several types of off-axis illumination sources. Note that the black areas are opaque, and the other areas are transparent.

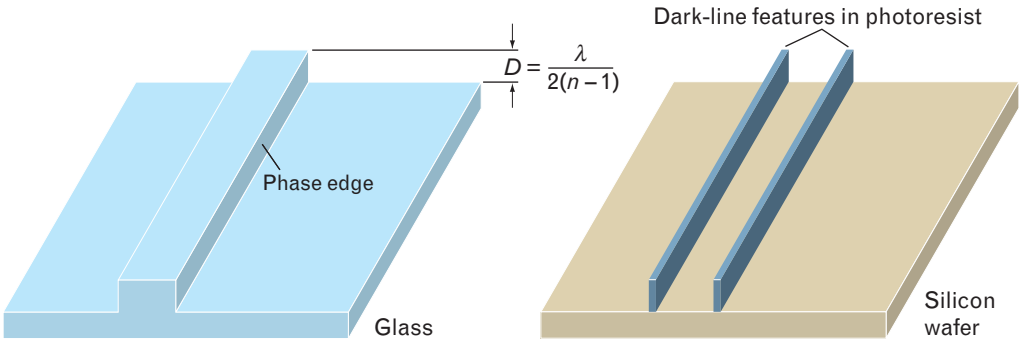


FIGURE 4. Schematic of a chromeless phase-shift photomask (left) and the features it creates in the photoresist (right). The depth D of the photomask feature equals $\lambda/2(n-1)$, where λ is the illumination wavelength and n is the index of refraction of glass for this λ. D corresponds to a half-wavelength path difference for the illumination light used. Note that the single relief feature in the glass photomask produces two dark-line features in the photoresist, one along each phase edge.

tems feature built-in variable illumination options. Because drawbacks include increased isodense-proximity effect, off-axis illumination is usually combined with some form of optical proximity correction.

Phase-shift photomasks represent the greatest resolution enhancement method in the subwavelength regime [2]. This method utilizes the phenomenon of destructive interference to generate dark-line features smaller than the wavelength of the illumination source. In this approach, shown in Figure 4, features are etched into the photomask glass surface to a depth D corresponding to a half-wavelength path difference for the particular illumination source used. For a 248-nm lithography system, this depth is approximately 244 nm in quartz. When the illumination light shines through a phase edge on the photomask, destructive interference causes the formation of a dark-line feature in the photoresist. Our work involved the simplest of many types of phase-shift masks—the chromeless phase-shift photomask—in which the final photomask pattern, etched in glass, does not contain chrome in the regions with critical dimensions.

The resolution enhancement produced by a phase-shift photomask is seen in Figure 5, which compares cross-sectional intensity plots of a narrow, dark-line feature imaged in the photoresist with a conventional

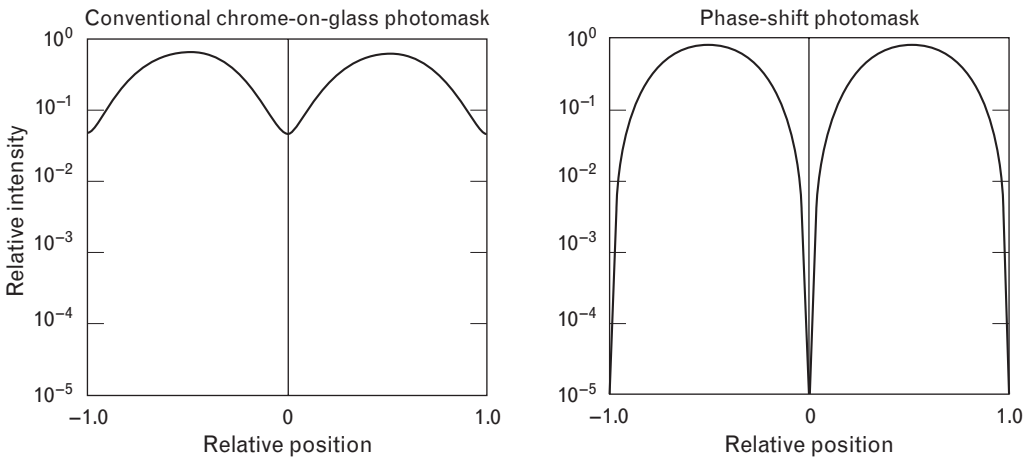


FIGURE 5. Simulated cross-sectional intensity plots of a narrow, dark-line feature imaged with a conventional chrome-on-glass photomask (left) and a phase-shift photomask (right). The phase-shift-formed dark line is significantly deeper and narrower.

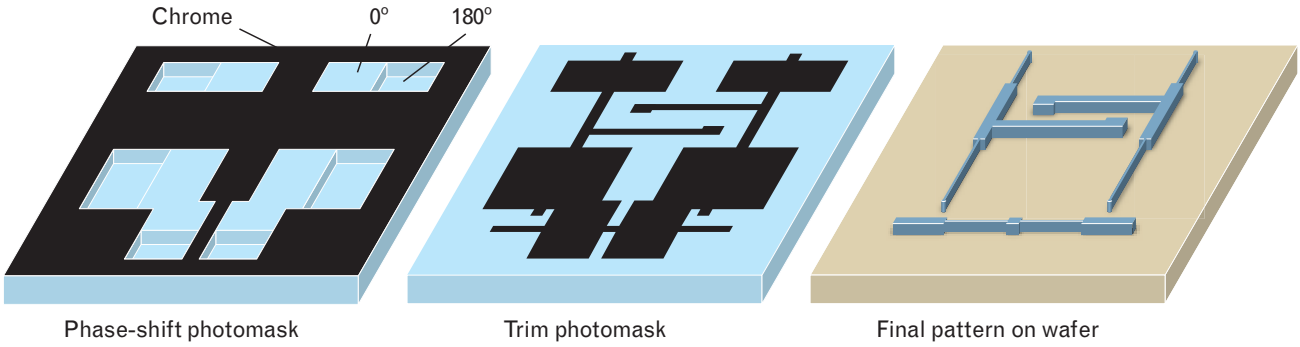


FIGURE 6. Schematic of the double-exposure phase-shift lithography process. The phase-shift and trim photomasks are sequentially exposed on the same region of the wafer. The final developed pattern of photoresist on the wafer is a combination of these two exposures.

chrome-on-glass photomask and with a phase-shift photomask [3]. The dark-line feature imaged with the phase-shift photomask is deeper and narrower, which allows imaging of photoresist features at sizes that are significantly smaller than the illumination wavelength.

Because all edge features produce a dark line, only closed patterns can be imaged with a phase-shift photomask. Two exposures are typically required; the second erasure exposure removes undesired features. Fabrication for the phase-shift photomask is more complex than for the standard chrome photomask, and advanced computer-aided design (CAD) software is required to decompose and verify the layout.

Applying Chromeless Phase-Shift Photomasks to Complementary Metal-Oxide Semiconductors

Lincoln Laboratory has pursued the fabrication of transistors with gate lengths in the 25-nm range. This research was part of a Defense Advanced Research Projects Agency (DARPA)–sponsored program in advanced complementary metal-oxide semiconductor (CMOS) technology. Lincoln Laboratory collaborated with Numerical Technologies, a start-up company that developed a novel method of double-exposure phase-shift imaging. We also worked closely with a photomask company, Photronics Inc., to fabricate the necessary custom phase-shift photomasks.

Figure 6 shows the basic double-exposure, phase-shift lithography approach developed by Numerical Technologies [4]. The desired integrated-circuit feature pattern is decomposed into two photomask patterns. The minimum-width features are placed on a primarily opaque (dark field) phase-shift photomask, and the interconnection and trim features are placed on a primarily transparent (bright field) chrome photomask. The first exposure images the narrow features on the wafer, and the second exposure images the interconnection features and trims the undesired phase-shift edge features. Both exposures are performed before the photoresist is developed. Numerical Technologies has developed sophisticated CAD tools to decompose and verify typical circuit patterns into such double-exposure photomask sets.

The double-exposure phase-shift technology allowed us to achieve isolated 25-nm minimum feature sizes, which are a remarkable 10% of the 248-nm illumination wavelength used. Gratings with feature pitch significantly smaller than any previously reported were also fabricated. For our experiments, we used a Canon EX-4 248-nm stepper, an industry standard in 1999 and 2000, with a numerical aperture of 0.6 and variable illumination. Compared to single-exposure techniques, wafer production takes longer with this method, but the improved patterning makes it worthwhile for many applications.

Figure 7 shows electron-microscope images of a ring oscillator circuit with 25-nm polysilicon gate lengths [5]. The smooth sidewalls of the very small polysilicon features, shown in the enlarged view, indicate a well-designed pattern-transfer etch process. These devices are made with fully depleted silicon-on-insulator technology [6], a type of advanced CMOS technology in which Lincoln Laboratory spe-

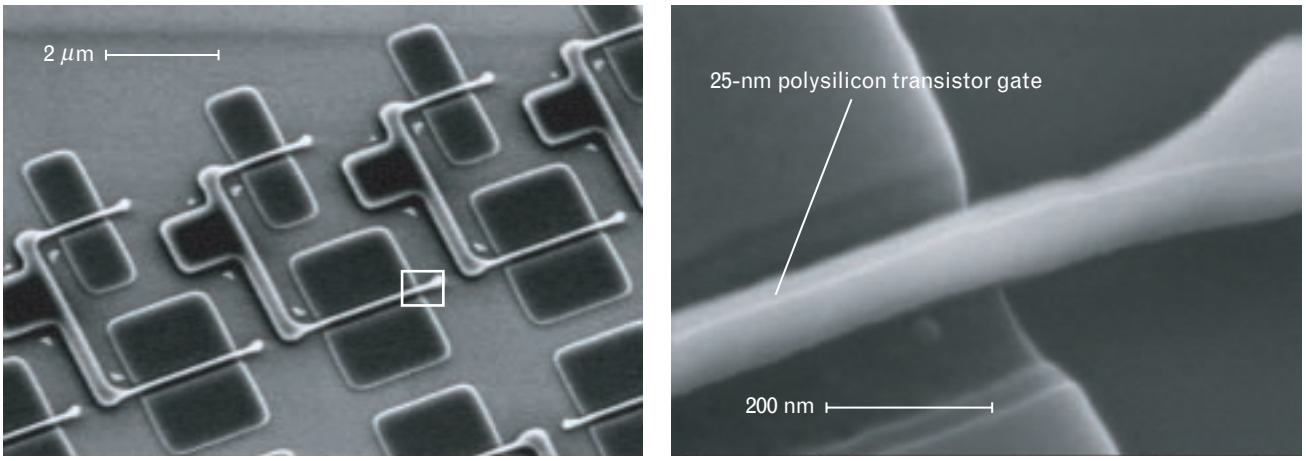


FIGURE 7. Electron-microscope images of a silicon-on-insulator circuit containing 25-nm polysilicon gate-length features. The enlarged view at right of one transistor segment shows the desirable smooth sidewalls of these narrow transistor gates.

cializes. At the time of this work (1999 to 2000), these gate lengths were among the smallest features ever imaged with optical lithography. This type of phase-shift imaging has since been adopted by major semiconductor companies, including Intel, United Microelectronics Corporation, Motorola, Texas Instruments, Lucent, and Samsung [7–9].

Our results were achieved by optimizing a number of aspects of the phase-shift imaging process. We chose to use chromeless features in the phase-shift part of the double-exposure process, shown in Figure 6. We used an ultrathin photoresist layer (255 nm thick) that performed well even when highly overexposed. Finally, we obtained the most effective illumination between the two exposures by using highly spatially coherent light for the interference-based phase-shift exposure, and light with moderate spatial coherence for the interconnect exposure.

Figure 8 shows the process latitude for the double-exposure phase-shift lithography technique. Figure 8(a) plots feature size versus focus for several exposure doses. We find that a depth of focus in excess of 0.5 μm is maintained even at resist feature sizes of 40 nm [10]. Figure 8(b) plots feature size versus exposure dose to show the exposure latitude, the sensitivity of the phase-shift lithography process to exposure dose. These data indicate that for the chromeless phase-shift process, the feature size is set by the exposure dose and not the photomask feature size. Fitting this exposure-dose curve with a power law results in an ex-

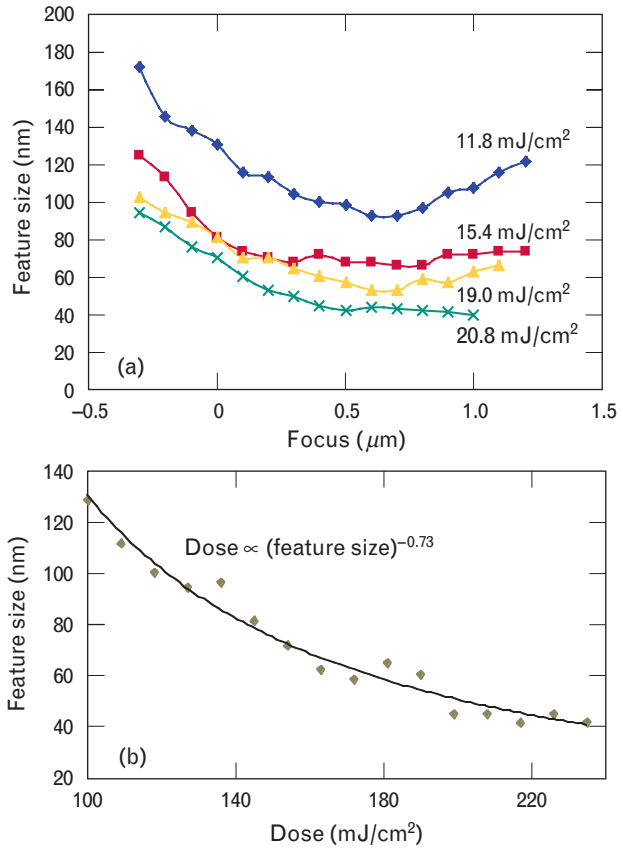


FIGURE 8. Process latitude for the double-exposure phase-shift-lithography technology. (a) The plot of feature size versus focus shows that a depth of focus in excess of 0.5 μm is maintained even at resist feature sizes of 40 nm. (b) The plot of feature size versus exposure dose shows that the feature size is set by the exposure dose and not the size of the photomask feature. Note the power law behavior of the exposure-dose curve.

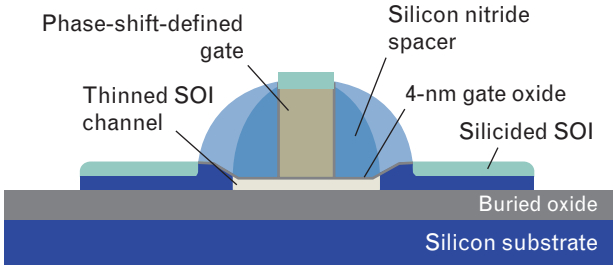


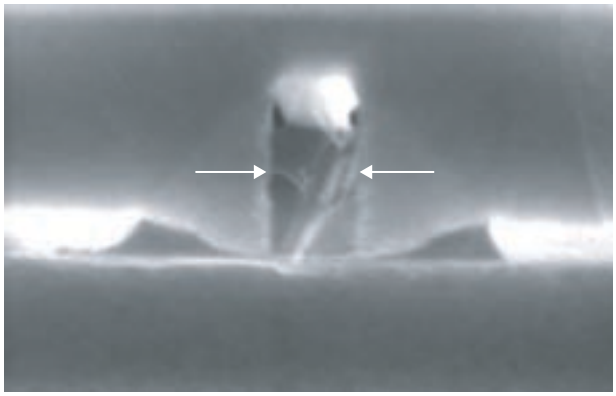
FIGURE 9. Schematic cross section of the type of silicon-on-insulator (SOI) transistor we worked on. The device has a fairly simple geometry, with key aspects being the phase-shift defined gate and the locally thinned channel beneath the gate.

posure latitude of 7.3 % independent of dose (up to the critical value at which the pattern suddenly collapses). This type of exposure latitude is in stark contrast to that obtained by using conventional chrome-on-glass masks, where significant overexposure results in a total loss of exposure latitude.

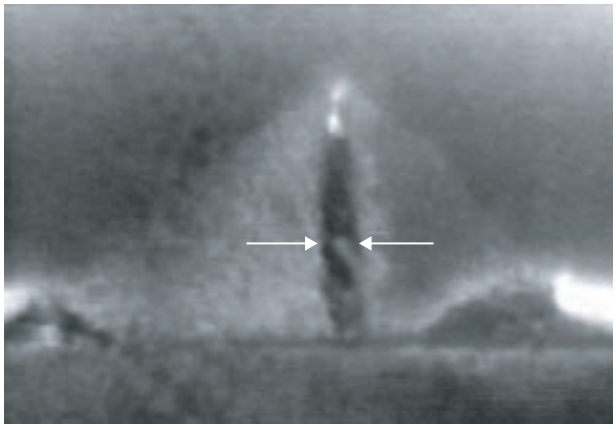
We used the double-exposure phase-shift lithography process to image transistor gates onto the photoresist. Figure 9 shows a cross-sectional schematic of the transistor design [5]. The silicon channel region under the narrow phase-shift defined gate is quite thin (7 to 15 nm), which is required to obtain good electrical performance from a small gate-length device in this technology. The rule of thumb for such a design is a silicon channel thickness of approximately one-fourth the gate length. To transfer this photoresist gate pattern to the underlying polysilicon, we developed a plasma-etch process that further shrank the 40-nm resist features to 25 nm [11]. The etch required vertical profiles, some lateral linewidth loss, and the ability to stop on thin 4-nm gate oxides.

Figure 10 shows a series of cross-sectional scanning-electron micrographs of silicon-on-insulator (SOI) transistors. These devices were imaged by using the same phase-shift photomask and by simply varying the exposure dose. Note that the vertical profiles for the polysilicon gate depict feature sizes as small as 9 nm, which corresponds to only 18 silicon lattice constants in size and less than 4% of the exposure wavelength.

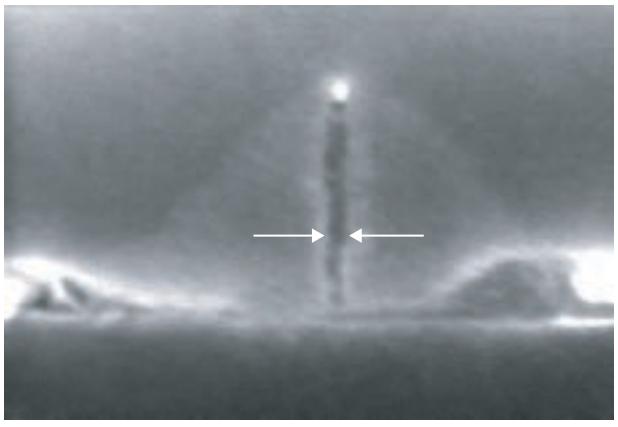
By using the double-exposure phase-shift lithography process, we were able to fabricate advanced SOI



Gate length = 90 nm



Gate length = 25 nm



Gate length = 9 nm

FIGURE 10. Series of cross-sectional electron-microscope images of SOI transistors fabricated by using the double-exposure phase-shift lithography method illustrated in Figure 6. These transistors were imaged with the same phase-shift photomask; we were able to achieve the order-of-magnitude reduction in gate length shown by applying different exposure doses. Figure 9 illustrates the transistor design.

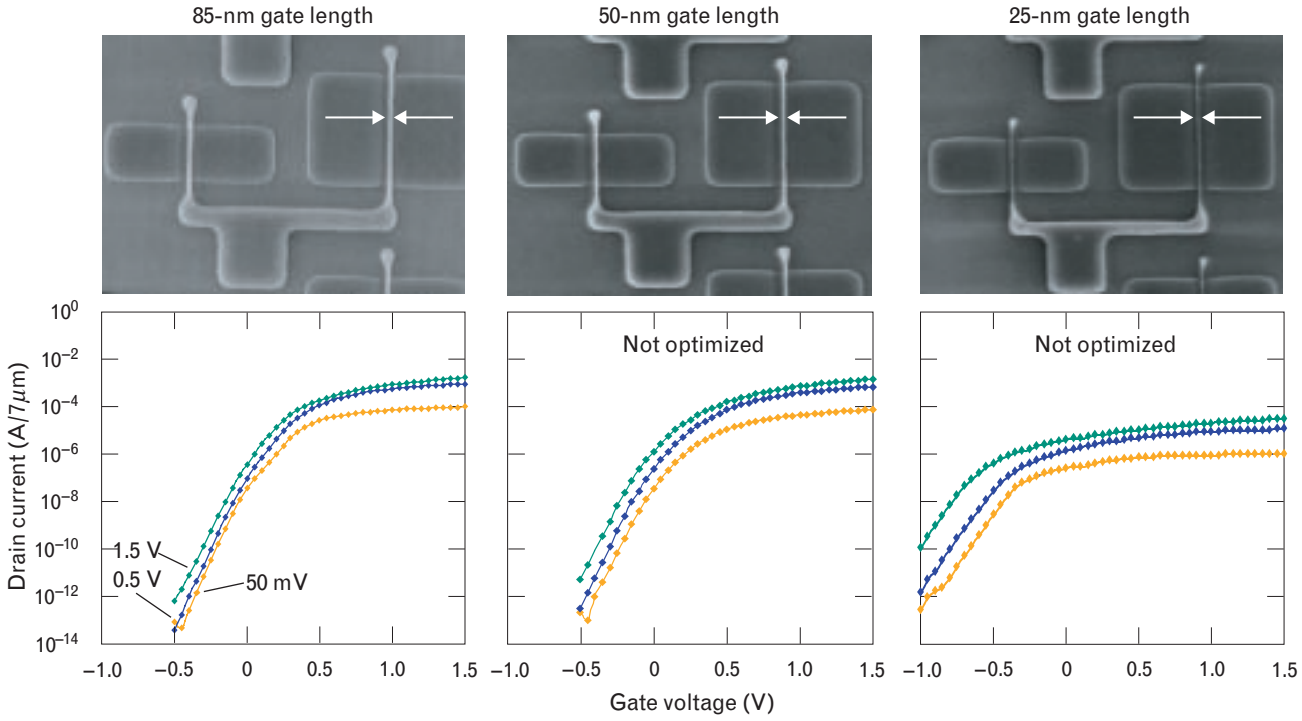


FIGURE 11. Performance test results for transistors of several different gate lengths. The decline in performance for gate lengths less than or equal to 50 nm indicates that the transistor design at these gate lengths was not optimized.

transistors with gate lengths in the 25-nm size regime specified by DARPA. We could then study the performance of highly scaled SOI CMOS technology years before its anticipated commercial introduction. The advantages of this technology include low power performance and improved scalability and radiation tolerance.

Typical transistor characteristics for this design are shown in Figure 11 for gate lengths of 85, 50, and 25 nm. The decline in performance for gate lengths of 50 nm or less indicates that the transistor design at these gate lengths was not optimized.

Our device research required us to fabricate primarily isolated narrow features, but we explored dense grating imaging as well. For practical implementation of phase-shift technology, narrow features must be imaged through a wide range of pitch values. Figure 12 shows an example of a dense grating feature that we fabricated using chromeless phase-shift imaging [12]. This 212-nm pitch grating was imaged in the photoresist by a 248-nm lithography tool with a numerical aperture of 0.65. The feature pitch is significantly below the exposure wavelength in this case, showing the potential for applying phase-shift methods to quite dense patterns.

Cost-Effective Implementation of Phase-Shift Lithography

The increased fabrication complexity associated with phase-shift lithography can add substantial photomask cost. Such increased photomask costs are difficult to amortize for applications that require a low-to-moderate number of wafers exposed per photomask. Application-specific integrated circuits (ASICs) and system-on-a-chip (SOC) designs, such as those used in the defense and telecommunications industries, are produced in low volumes compared with the microprocessors and memory found in personal computers. For these applications, many of the advantages of RET lithography are not economically viable. In addition, it is becoming increasingly difficult to correct for image nonuniformities caused by the isodense-proximity and spatial-frequency effects as feature sizes become much smaller than the imaging wavelength.

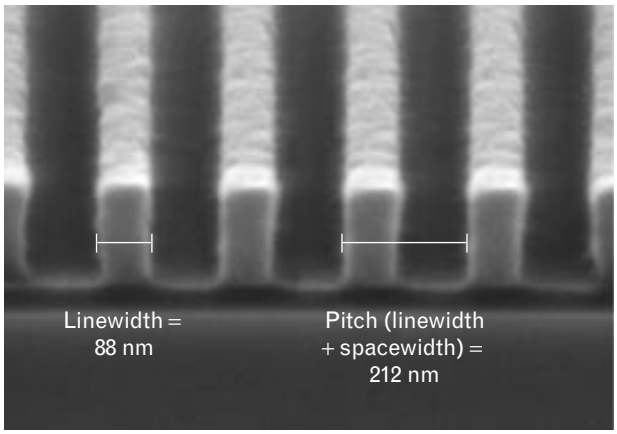


FIGURE 12. Electron-microscope cross section of a 212-nm pitch grating formed by using a chromeless phase-shift photomask and a 248-nm exposure tool. In this case, the grating pitch is smaller than the exposure wavelength.

Under the sponsorship of Lincoln Laboratory's Advanced Concepts Committee, we have developed an implementation of phase-shift lithography that addresses a number of issues, including high photomask cost and proximity effect distortions [12]. We have dubbed this method GRATEFUL, which stands for gratings of regular arrays and trim exposures for ultra-large-scale integration (ULSI) lithography. In this method, all critical circuit features are imaged by using simple one-dimensional phase-shift-grating template photomasks, which are customized with subsequent trim exposures. The template photomask can be reused for a wide variety of designs together with different trim masks. Simple grating phase-shift photomask patterns are easier to fabricate and inspect than arbitrary geometry masks, thus reducing their cost and enhancing their yield. In addition, because all fine feature imaging is done with dense gratings, proximity effects are effectively eliminated along with the complex photomask features typically used to correct them. This approach has two restrictions: all fine features must be placed on the design grating grid, and all pitch values must be integer multiples of the minimum resolvable pitch.

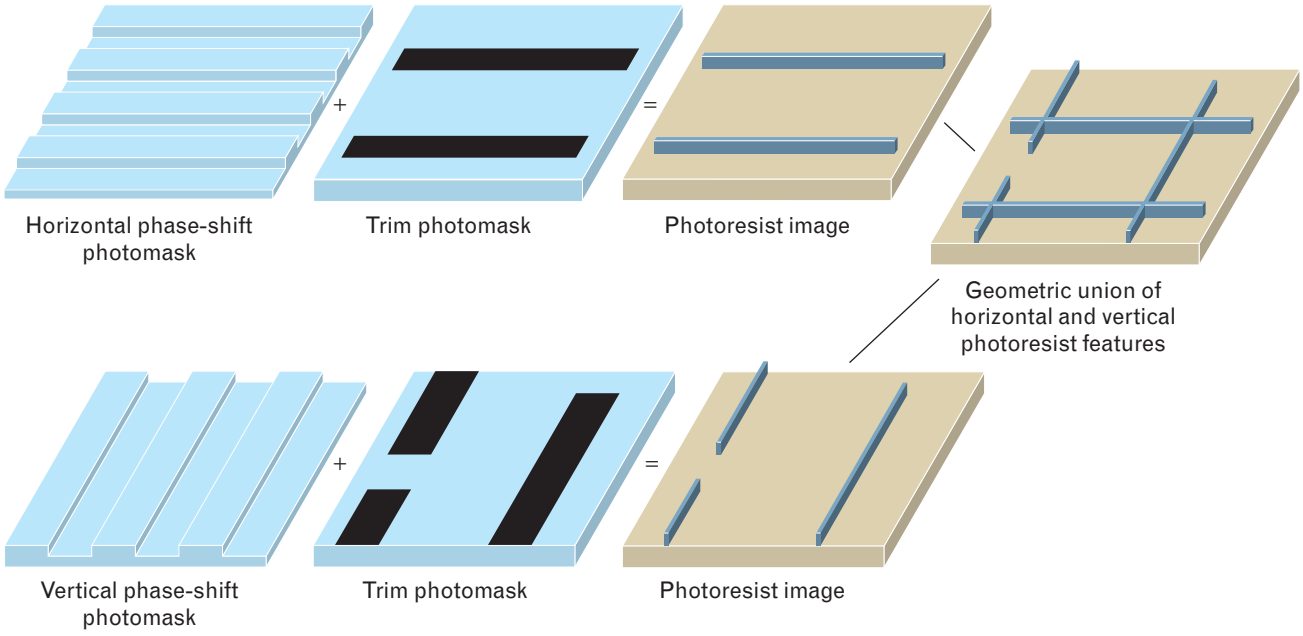


FIGURE 13. Schematic diagram of the GRATEFUL imaging method, a cost-effective implementation of phase-shift lithography. The acronym stands for gratings of regular arrays and trim exposures for ultra-large-scale integration (ULSI) lithography. Features in the *x*-direction on the photoresist (top) are created by using a horizontal phase-shift photomask (*x*-oriented grating) and a trim photomask. Features in the *y*-direction on a different photoresist layer (bottom) are created using the identical process with a vertical phase-shift photomask (*y*-oriented grating) and a trim photomask. The final result on the photoresist combines features in both directions.

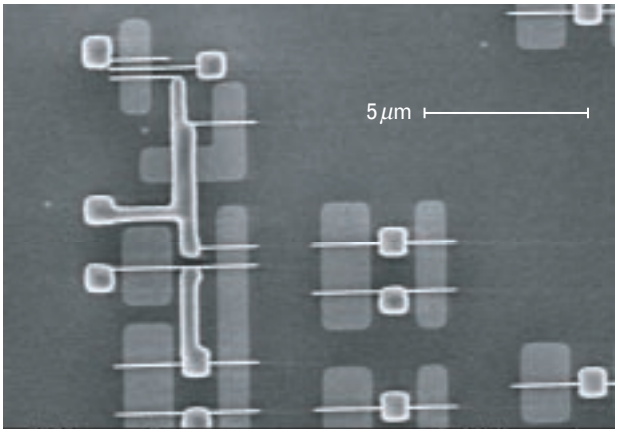


FIGURE 14. Experimental example of the GRATEFUL imaging method applied to a circuit pattern with fine features oriented only in the *x*-direction. Note the absence of isodense proximity effects as shown by good feature size control through a variety of pitch values.

A schematic outline of the GRATEFUL method is shown in Figure 13 [13]. The first step uses a one-dimensional grating in the *x*-orientation combined with a trim exposure to form a series of narrow line features in the *x*-direction. The photoresist is then baked to make it insensitive to further developing, and a second layer of photoresist is coated over these features. The process is repeated with a *y*-oriented phase-shift grating and trim. The final result is a complex pattern with critical features in both orientations. This type of method limits feature geometries to Manhattan (*x*-axis and *y*-axis) orientations.

Figure 14 shows an example of the GRATEFUL method [12]. In this case, the circuit pattern has narrow line features in only the *x*-orientation. A simple one-dimensional phase-shift grating was used together with a conventional trim exposure to create the fine lines. The larger interconnect features were added in the second layer of photoresist. Linewidths are maintained through a large pitch range, which indicates an absence of isodense-proximity effects.

Figure 15 shows a second GRATEFUL example [13]. Here, fine features in the *x*- and *y*-orientations were formed in separate layers of photoresist. A different dose was used in each orientation, resulting in different feature sizes. Because the imaging was performed in two layers of photoresist, spatial-frequency corner-rounding effects were effectively eliminated, as shown by the sharp corners. Figure 16 shows an example of a circuit pattern with fine features in both *x*-

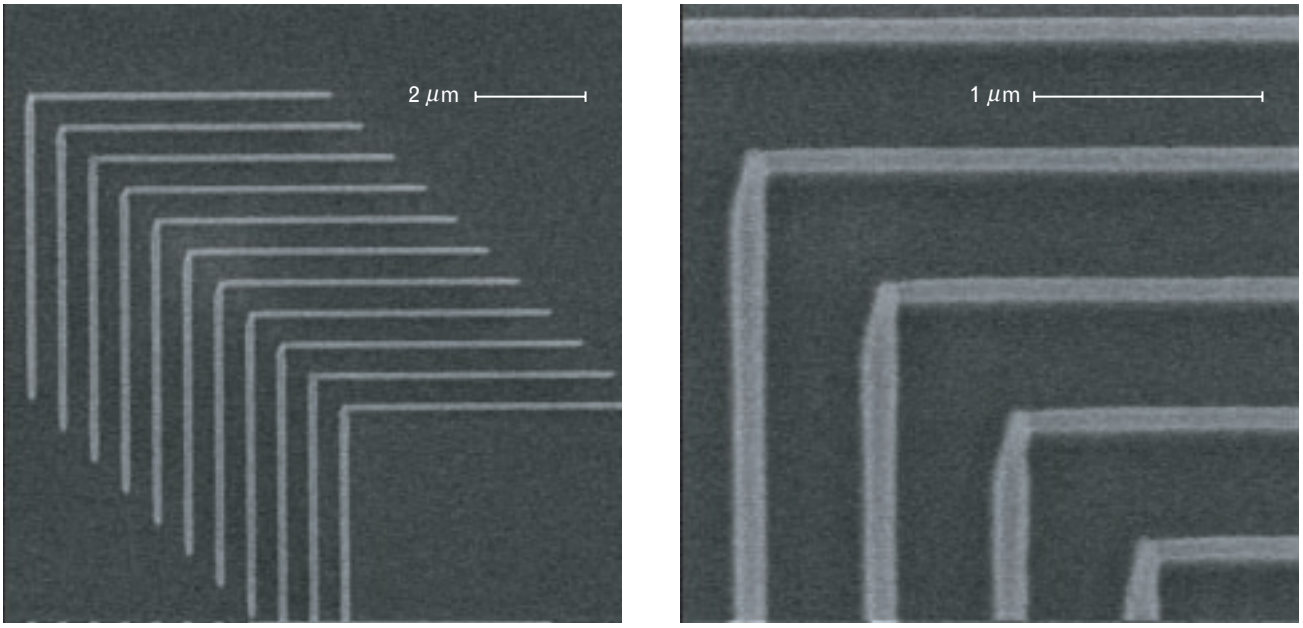


FIGURE 15. Two magnifications of experimental example of the GRATEFUL imaging method applied to a test pattern with fine features in two orientations. The sharp corner features produced in this manner, seen in the magnified view on the right, indicate minimal spatial-frequency effects.

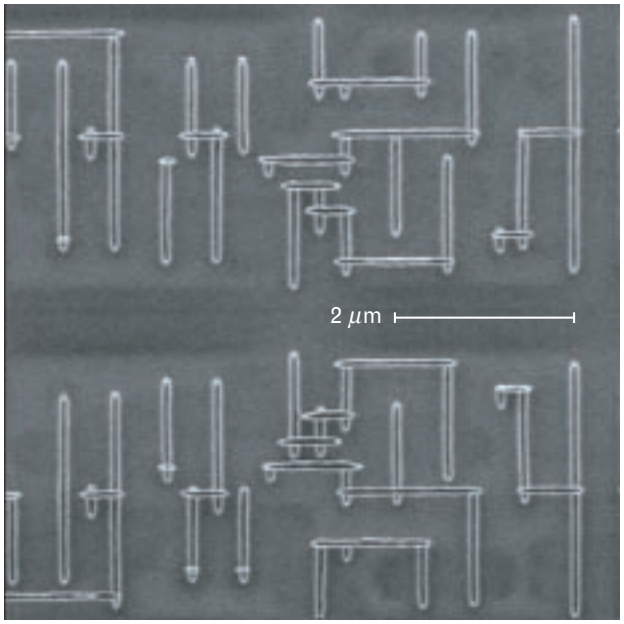


FIGURE 16. GRATEFUL method applied to a circuit pattern with fine features in both *x*- and *y*-orientations. The fundamental pitch is 280 nm, corresponding to k_1 = 0.34 for our system. Note the absence of optical proximity effects.

and *y*-orientations. The phase-shift photomask used to create this pattern was a simple one-dimensional grating.

We have performed a cost analysis of our template-based lithography approach and compared it to current methods used for critical-level lithography in industry [14]. We modeled the cost per critical level per wafer as a function of the number of wafers per photomask for 90-nm-node technology currently under development. The model assumptions were a stepper cost of $15 million with five-year depreciation, 7% maintenance cost per year, and 100% uptime; a photomask set cost of $2 million, for a 30-photomask set with highly critical gate and contact level; a tool throughput of 130 wafers per hour; and a resist processing cost of $5 per wafer. Labor and clean-room costs were neglected. We also modeled direct-write lithography, which does not require photomasks, assuming a tool cost of $15 million and an optimistic throughput of one wafer per hour.

Figure 17 summarizes the results of this analysis. Three regions are clearly evident. For very low wafer volume, direct write is the cheapest method, and for very high volume, the one- or two-exposure custom phase-shift-photomask method (currently practiced by industry) is the most economical. In the large intermediate regime, however, template-based methods such as GRATEFUL are the most cost effective, despite the fact that some implementations require more than two exposures and possibly two levels of resist. Figure 17 also shows the results of a survey of photomask usage conducted by the Semiconductor Manufacturing Technology (SEMATECH) consortium in 2000. Large peaks in industrial photomask usage fall within the regime of template-based methods, and typical defense integrated-circuit applications at the low end of template methods and the high end of direct write.

Summary

We have developed a phase-shift lithography process capable of imaging feature sizes as small as 16% of the 248-nm exposure wavelength. Using this process together with a controlled etch bias, we have fabricated transistor gates as small as 9 nm, corresponding to only 18 silicon lattice constants in size. This lithography method has allowed us to fabricate next-generation SOI transistors by using currently available optical-lithography equipment. We have also been developing a method of phase-shift technology that uses simple reusable template photomasks with fine features. This method has the potential to make advanced phase-shift imaging cost effective for moderate-to-low wafer counts per photomask, a situation encountered in low-volume manufacturing applications such as ASICs used by commercial and Department of Defense systems.

Acknowledgments

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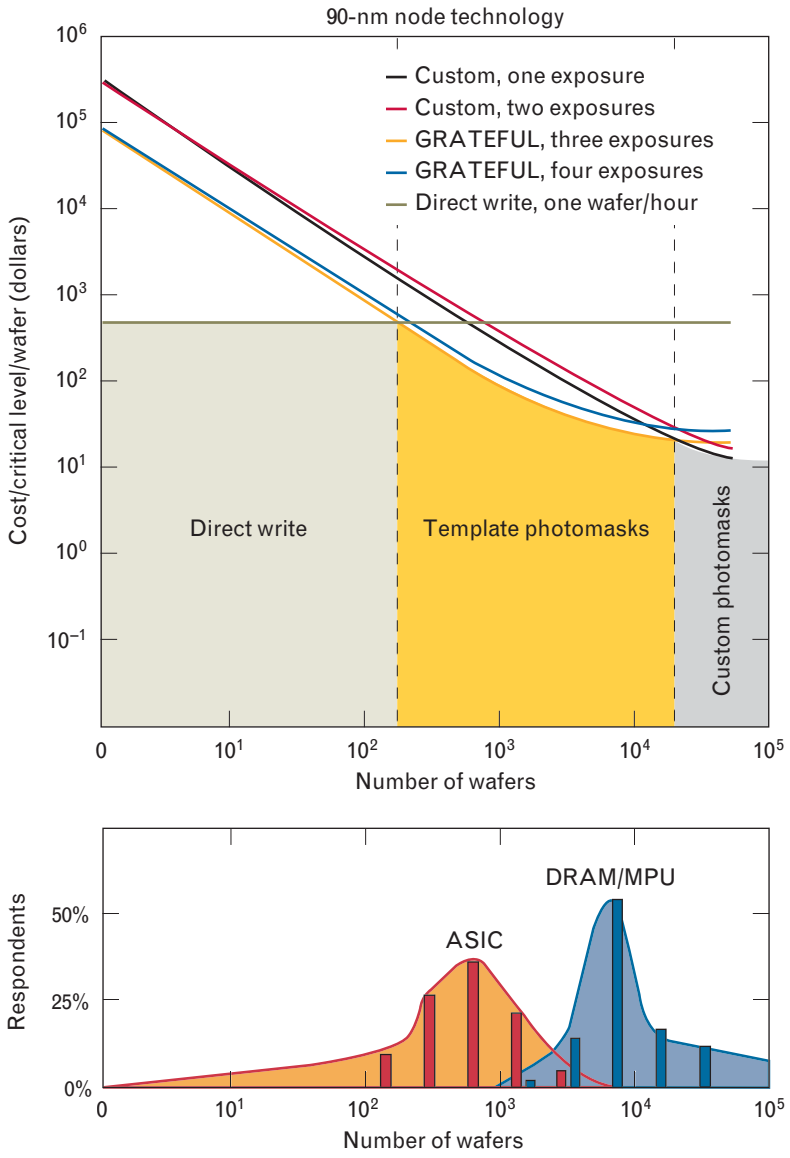

FIGURE 17. Comparison of 90-nm node lithography costs for various fabrication methods: direct write, template photomask, and custom photomask (top) and results of a 2000 survey of photomask usage conducted by the Semiconductor Manufacturing Technology (SEMATECH) consortium (bottom). At low wafer volumes, the direct-write method is the most cost-effective. At high wafer volumes, the one- or two-exposure custom phase-shift-photomask method is the most cost-effective. Large peaks in industrial photomask usage, which includes application-specific integrated circuits (ASIC) and dynamic random access memory (DRAM) and microprocessor unit (MPU) chips, fall within the regime of template photomasks.

REFERENCES

1. A.K.-K. Wong, *Resolution Enhancement Techniques in Optical Lithography* (SPIE Press, Bellingham, Wash., 2001).
2. M.D. Levenson, N.S. Viswanathan, and R.A. Simpson, "Improving Resolution in Photolithography with a Phase-Shifting Mask," *IEEE Trans. Electron Devices* **29** (12), 1982, pp. 1828–1836.
3. M.D. Levenson, "Extending the Lifetime of Optical Lithography Technologies with Wavefront Engineering," *Jpn. J. Appl. Phys.* **33** (12B, pt. 1), 1994, pp. 6765–6773.
4. H.-Y. Liu, L. Karklin, Y.-T. Wang, and Y.C. Pati, "The Application of Alternating Phase-Shifting Masks to 140 nm Gate Patterning (II): Mask Design and Manufacturing Tolerances," *SPIE* **3334,** 1998, pp. 2–14.
5. M. Fritze, J. Burns, P.W. Wyatt, C.K. Chen, P. Gouker, C.L. Chen, C. Keast, D. Astolfi, D. Yost, D. Preble, A. Curtis, P. Davis, S. Cann, S. Deneault, and H.Y. Liu, "Sub-100 nm Silicon on Insulator Complementary Metal-Oxide Semiconductor Transistors by Deep Ultraviolet Optical Lithography," *J. Vac. Sci. Technol. B* **18** (6), 2000, pp. 2886–2890.
6. J.M Burns, C.L. Keast, J.M. Knecht, R.R. Kunz, S.C. Palmateer, S. Cann, A. Soares, and D.C. Shaver, "Performance of a Low Power Fully-Depleted Deep Submicron SOI Technology and Its Extension to 0.15 μm," *Proc. 1996 Int. SOI Conf., 30 Sept.–3 Oct., Sanibel Island, Fla.,* pp. 102–103.
7. R. Schenker, H. Kirchauer, A. Stivers, and E. Tejnil, "Alt-PSM for 0.10μm and 0.13μm Poly Patterning," *SPIE* **4000,** pt. 1, 2000, pp. 112–120.
8. C.-M. Wang, C.-W. Lai, J. Huang, and H.-Y. Liu, "Patterning 80-nm Gates Using 248-nm Lithography: An Approach for 0.13 Micron VLSI Manufacturing," *SPIE* **4346,** pt. 1, 2001, pp. 452–463.
9. C. Nelson-Thomas, M. Kling, M. Thomson, R. Wang, N. Cave, and C.-C. Fu, "Effects of Complementary Phase Shift Imaging on Gate CD Control," *SPIE* **4346,** pt. 1, 2001, pp. 464–470.
10. M. Fritze, J.M. Burns, P.W. Wyatt, D.K. Astolfi, T. Forte, D. Yost, P. Davis, A. Curtis, D.M. Preble, S. Cann, S. Deneault, H.-Y. Liu, J.C. Shaw, N.T. Sullivan, R. Brandom, and M. Mastovich, "Application of Chromeless Phase-Shift Masks to Sub-100 nm SOI CMOS Transistor Fabrication," *SPIE* **4000,** pt. 1, 2000, pp. 388–407.
11. D. Yost, T. Forte, M. Fritze, D. Astolfi, V. Suntharalingam, C.K Chen, and S. Cann, "Dry Etching of Amorphous-Si Gates for Deep Sub-100 nm Silicon-on-Insulator Complementary Metal-Oxide Semiconductor," *J. Vac. Sci Technol B* **20** (1), 2002, pp. 191–196.
12. M. Fritze, B. Tyrrell, D. Astolfi, D. Yost, P. Davis, B. Wheeler, R. Mallen, J. Jarmalowicz, S. Cann, D. Chan, P. Rhyins, C. Carney, J. Ferri, and B.A. Blachowicz, "Gratings of Regular Arrays and Trim Exposures for Ultralarge Scale Integrated Circuit Phase-Shift Lithography," *J. Vac. Sci. Technol. B* **19** (6), 2001, pp. 2366–2370.
16. B. Tyrrell, M. Fritze, R. Mallen, B. Wheeler, P. Rhyins, and P. Martin, "Investigation of the Physical and Practical Limits of Dense-Only Phase Shift Lithography for Circuit Feature Definition," *JM*^{3} **1** (3), 2003, pp. 243–252.
17. B. Tyrrell, M. Fritze, R. Mallen, B. Wheeler, P. Rhyins, and P. Martin, "Dense-Only Phase Shift Template Lithography," *SPIE* **5042,** 2003, pp. 15–29.

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