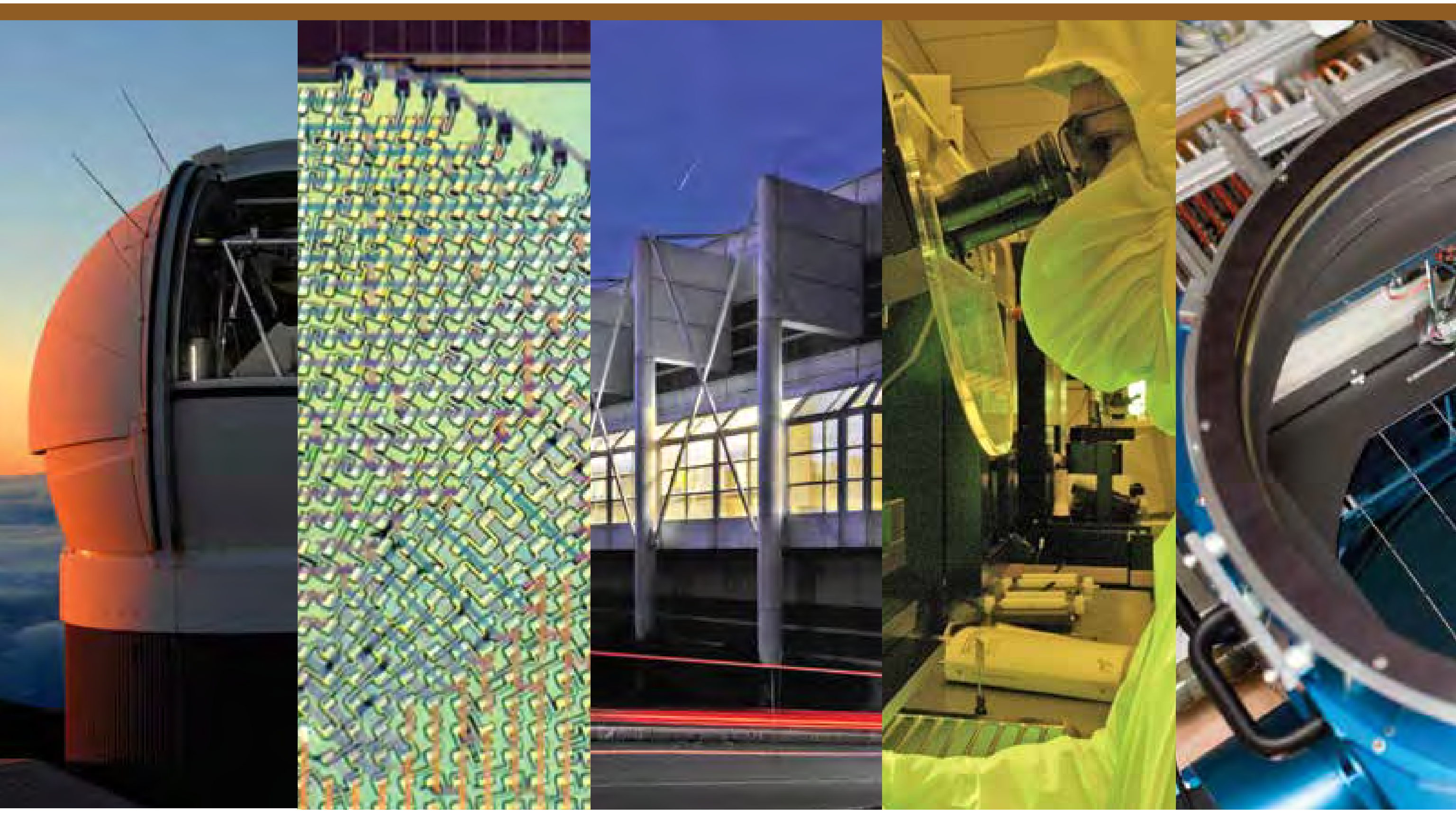
20 INNOVATIONS
OVER TWENTY YEARS

Highlights of Technology Advancements at the

Microelectronics Laboratory



LINCOLN LABORATORY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY

From the Director

MIT Lincoln Laboratory is very pleased to be celebrating the Microelectronics Laboratory's 20th year of operation. The technology developed through this laboratory has been critically important to advancing the system prototypes and components Lincoln Laboratory transitions through the Department of Defense, Department of Homeland Security, Federal Aviation Administration, National Aeronautics and Space Administration, and other sponsors. Many of the innovations driven by the Microelectronics Laboratory in semiconductor processes, charge-coupled-device technology, optical projection lithography, and integrated-circuit fabrication have pushed beyond the current state of the art and become industry standards.

Since its opening in 1994, the Microelectronics Laboratory has evolved to meet the requirements for a research and development fabrication facility that develops increasingly small and powerful electronics. The 2011 upgrade to enable sub-90 nm processing on 200 mm wafers added new capabilities for advancing technology over the next several years. The expertise of our researchers, combined with an upgraded tool set, has contributed to establishing the Microelectronics Laboratory's reputation as a strong center for innovation in support of national security. Lincoln Laboratory will continue to invest in new microelectronics equipment and processes as national security needs arise.

We encourage you to review this publication to get an overview of the technology developed in the Microelectronics Lab. As the demand for micro- and nano-systems continues to grow, we look forward to meeting the research and development challenges with the technical excellence and creativity that have been the hallmarks of our microelectronics work.

Eric D. Evans
Director

About MIT Lincoln Laboratory

Lincoln Laboratory is a federally funded research and development center (FFRDC) focused on the development and prototyping of new technologies and capabilities to meet national security needs. Principal core competencies are in sensors, information extraction (signal processing and embedded computing), communications, integrated sensing, and decision support, all supported by a broad research base in advanced electronics. Program activities extend from fundamental investigations through design and field testing of prototype systems using new technologies.

For 62 years, Lincoln Laboratory has met the government's FFRDC goals of providing independent perspective on critical issues, maintaining long-term competency, and developing technology for both long-term interests and short-term, high-priority needs. The Laboratory places a strong emphasis on transitioning its innovative systems and technology to the military services, government agencies, industry, and academia.

Program activities are centered in ten mission areas

- Space Control
- Air and Missile Defense Technology
- Communication Systems
- Cyber Security and Information Sciences
- Intelligence, Surveillance, and Reconnaissance Systems and Technology
- Tactical Systems
- Advanced Technology
- Homeland Protection
- Air Traffic Control
- Engineering

From the Advanced Technology Division

The Advanced Technology Division identifies new phenomenology that can be exploited in innovative system applications and develops revolutionary advances in subsystem and component technologies that allow key, new system capabilities. The continuing vision of the Advanced Technology mission is to provide the breakthroughs that enable novel sensing, computation, and communication systems to address the most challenging national security concerns. This goal is accomplished by a community of researchers with deep technical expertise, collectively knowledgeable across a significant range of disciplines, working in unique, world-class facilities.

The division operates and maintains specialized electronic, materials growth, fabrication, and integration facilities to support our advanced electronics work, which ranges from fundamental investigations in materials science, through the development of new electronic devices and components, to the design, development, and field demonstration of complex prototype systems.

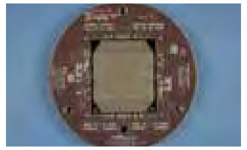
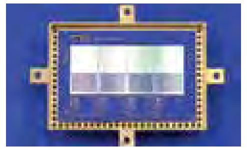
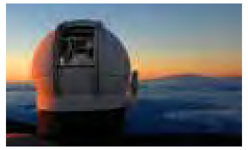
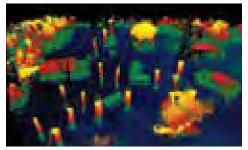
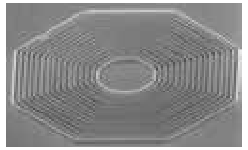
In the early 1990s, Lincoln Laboratory built the Microelectronics Laboratory to support its silicon-based electronics work. This laboratory has successfully undergone two major upgrades in the last 20 years and stands out as the nation's premier silicon-based research and advanced prototyping facility dedicated to supporting the needs of the Department of Defense and the broader national security community.

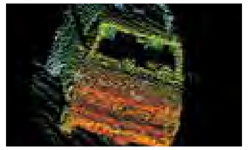
Lincoln Laboratory has a long and rich history of transferring advanced electronic devices and processes important to a wide array of applications. From the co-invention of the diode laser in the 1960s, to the seminal work on 193 nm lithography that is currently used to fabricate most modern integrated circuits, to the development of specialized three-dimensional laser-radar focal plane arrays that have flown more than 800 mapping sorties over Afghanistan, the Laboratory continues to leverage its specialized facilities to the benefit of the nation and the world.

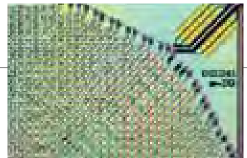
Robert G. Atkins
Division Head

Craig L. Keast
Associate Division Head

Simon Verghese
Assistant Division Head



20 INNOVATIONS OVER TWENTY YEARS

Highlights of Technology Advancements at the

Microelectronics Laboratory

About the Microelectronics Laboratory

The MIT Lincoln Laboratory Microelectronics Laboratory is a state-of-the-art semiconductor research and fabrication facility supporting a wide range of Lincoln Laboratory programs. The 70,000-square-foot facility has 8100 square feet of class-10 and 10,000 square feet of class-100 cleanroom areas.

The equipment set in this laboratory is continually updated and includes a production-class complementary metal-oxide semiconductor (CMOS) toolset with angled ion-implantation, cluster-metallization, dry-etch, chemical-mechanical planarization equipment, and rapid thermal processing and advanced lithography capabilities. A molecular-beam epitaxy system is used to provide highly sensitive and highly stable back-illuminated devices in the ultraviolet and extreme ultraviolet ranges.

Current activities include work on the following

- The fabrication of flight-quality gigapixel charge-coupled-device (CCD) imager focal planes
- Photon-counting avalanche photodiode arrays
- Radio-frequency and optical microelectrical mechanical systems (MEMS)
- Niobium-based superconducting circuits
- A fully depleted silicon-on-insulator (FDSOI) CMOS circuit prototyping capability

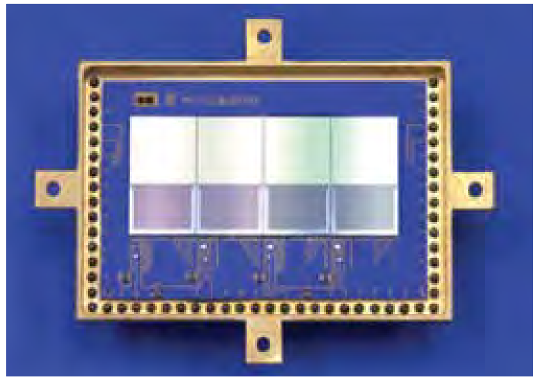
In addition, the Microelectronics Laboratory supports advanced packaging with a precision-multichip-module technology and an advanced three-dimensional circuit stacking technology. Currently, more than 40 different programs from five of the eight divisions at Lincoln Laboratory, as well as industrial sponsors involved through cooperative research and development agreements, are supported by the Microelectronics Laboratory, which is staffed by approximately 60 technicians, engineers, and scientists working two shifts each day, five days a week.

1993

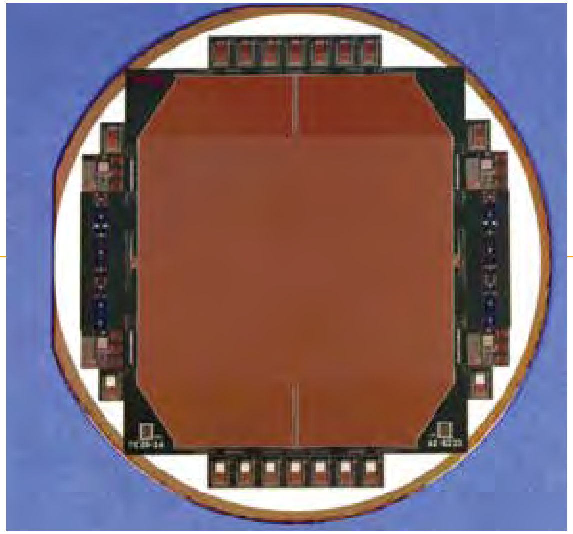
Space-Based Visible

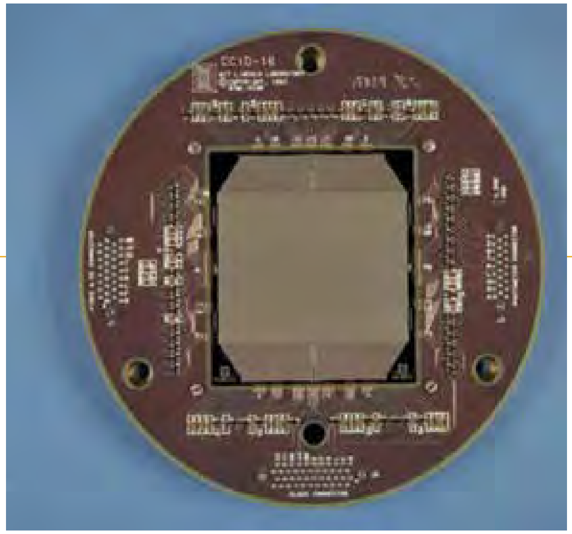
The Space-Based Visible (SBV) sensor was the first successful space-based space surveillance system. This sensor combined a small (6-inch aperture) telescope and a focal plane array of four precisely aligned visible-band charge-coupled-device (CCD) imagers that were fabricated in the Microelectronics Laboratory. Because of the very low noise of the CCDs (less than 4 electrons), this camera could detect faint objects, comparable in size to a golf ball at a 1000 km distance, against stellar backgrounds.

The SBV instrument was launched in 1996 as part of a larger Midcourse Space Experiment (MSX) satellite. Over its life, the SBV sensor collected data on several domestic ballistic missile tests, providing a wealth of knowledge on the properties of sun-illuminated objects and the capabilities of visible-band optics to capture their signatures and estimate their trajectories. After 12 years of operation, the SBV system was shut down in 2008, but its success led to the Air Force's next-generation system, the Space-Based Space Surveillance satellite. The CCD technology developed for SBV was successfully applied to several other satellite programs whose imagers were also fabricated in the Microelectronics Laboratory.



Left, Midcourse Space Experiment; above, the SBV focal plane





GEODSS imagers: left, on a 100 mm wafer; right, integrated with support electronics

1994

Ground-Based Electro-optical Deep-Space Surveillance Systems

The ground-based electro-optical deep-space surveillance (GEODSS) systems at the Experimental Test Site (ETS) in New Mexico provide the U.S. Air Force with excellent imagery of small satellites. In 1991, the Air Force was seeking a modern replacement for the large Ebsicon vacuum-tube cameras used in GEODSS. Because Lincoln Laboratory's Microelectronics Laboratory was fabricating CCD imagers that met all GEODSS specifications except large focal plane size, the Laboratory was asked to investigate the development of an imager that could meet that final requirement. The resulting imager was so large that one imager completely filled the 100 mm silicon wafer used for fabrication at the time. In addition to its large size, the GEODSS device also used high-quantum-efficiency back-illuminated technology, which had been demonstrated on small-area CCDs but was very challenging to reliably produce over larger areas. The GEODSS experience in scaling back-illuminated technology to a wafer scale was so successful that today most CCDs developed at the Laboratory use this feature to improve the quantum efficiency of the device and to extend its wavelength range, especially toward the ultraviolet and into the X-ray regime.

The successful fabrication of this imager was accomplished in 1994 and supplied to Photometrics to build the prototype CCD camera. The prototype cameras were used in the GEODSS Upgrade Prototype System to develop operational image processing software and demonstrate the enhanced performance of CCD cameras in GEODSS. The unique CCD technology developed at Lincoln Laboratory has significantly expanded the capabilities of GEODSS systems, making them the most successful ground-based optical space surveillance systems ever developed. These cameras continue to be used to search for asteroids at the ETS under the Lincoln Near-Earth Asteroid Research (LINEAR) program, which has made 98% of all worldwide detections and observations of near-Earth objects.

1994

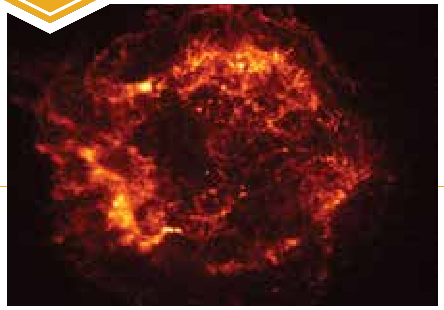
World's first 193 nm wafer exposure system in the Microelectronics Laboratory

National Center for Advanced Photoresist Development

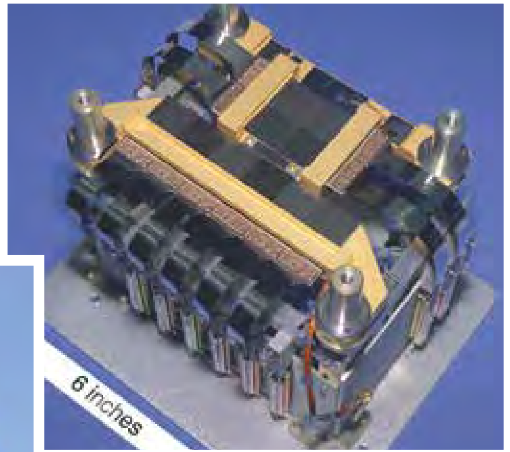
The National Center for Advanced Photoresist Development was instrumental in enhancing the competitiveness of U.S. companies in a technology area that underpins much of the microelectronics industry's ability to keep apace of Moore's Law. This center was unique in that it was a joint project, for which all the U.S. photoresist companies (Shipley, OCG, Hoechst Celanese, Brewer Science), as well as organizations involved in photoresist development (IBM, AT&T Bell Laboratories, SEMATECH, Semiconductor Research Corporation), pooled their resources. State-of-the-art lithographic equipment was provided by SEMATECH, and operating costs were covered by the other members of this ad hoc consortium. Lincoln Laboratory's new Microelectronics Laboratory, including the world's first 193 nm projection scanner installed there, was an enabler of the center. Engineers and scientists from the member companies worked shoulder to shoulder with Lincoln Laboratory personnel to develop, improve upon, and qualify new photoresists and photoresist-related processes. As a result, the center rapidly advanced 248 nm and 193 nm resist patterning with improvements to resolution and line-edge roughness, and the implementation of antireflective layers.

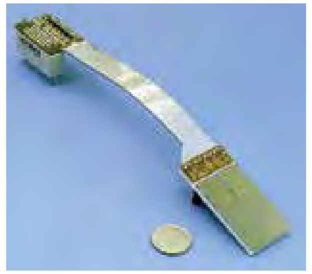
1995

Chandra



The Chandra X-ray Observatory, one of the NASA Great Observatories, was deployed by the Space Shuttle *Columbia* in 1999. It was designed for high-resolution imaging of X-ray astronomical objects from space. Lincoln Laboratory developed and assembled the Advanced CCD Imaging Spectrometer (ACIS), one of two imaging systems on board Chandra. The ACIS contains ten CCD imaging arrays that were fabricated in Lincoln Laboratory's Microelectronics Laboratory. Fabrication development increased sensitivity of the device by the removal of defects from the silicon substrates. Each CCD array comprises a million pixels. Two of the imaging arrays were specially designed back-illuminated devices fabricated by using a novel high-temperature oxidation and annealing technology developed in the Microelectronics Laboratory in order to achieve high quantum efficiency for the detection of very-low-energy X rays. The Chandra Observatory continues to make important contributions to astrophysics and to rely on the ACIS for 95% of its science imagery.





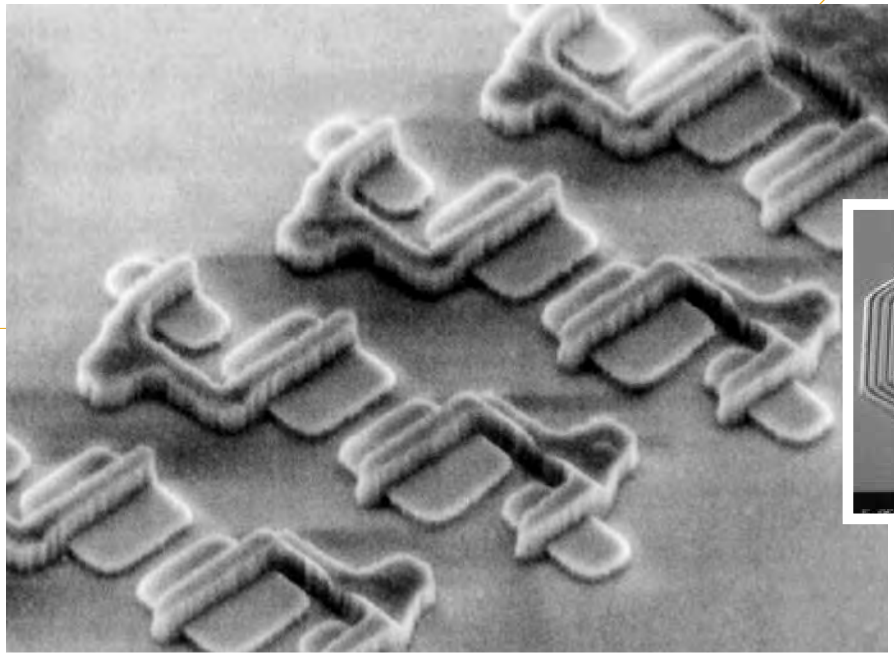
Facing page, X-ray image of the Cassiopeia A supernova; top, lens optics for Chandra; bottom right, 10-chip array; bottom left, single chip and readout connector

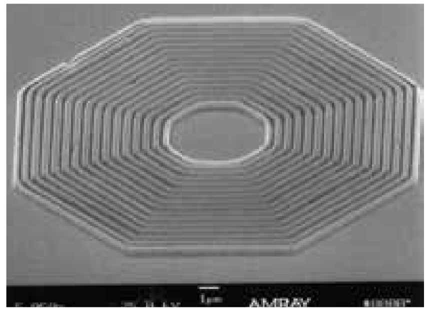
193 nm Lithography Devices

1996

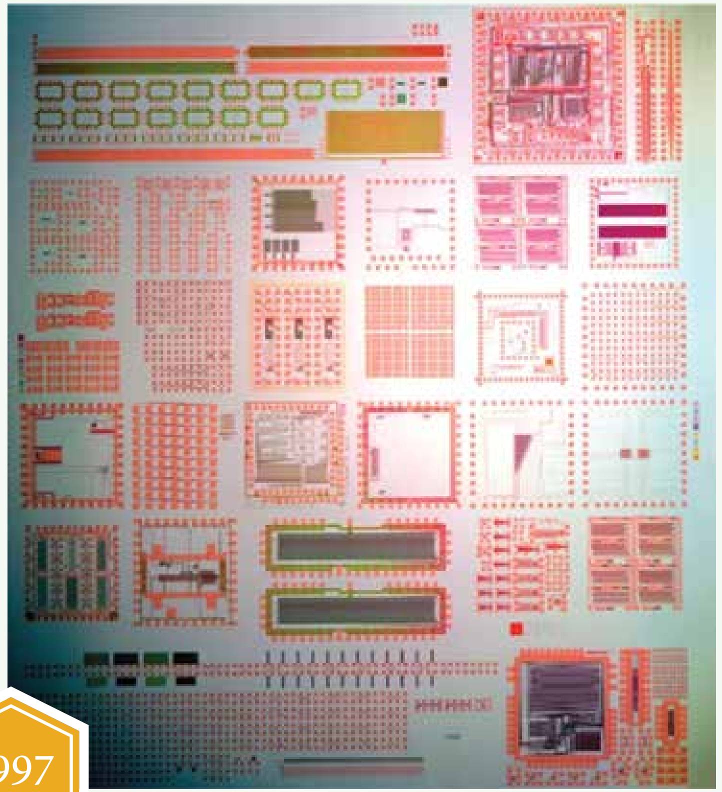
Optical projection lithography at 193 nm, pioneered by Lincoln Laboratory, became the industry standard by the early 2000s and to this date remains the prevailing patterning technique used for critical-level integrated-circuit device fabrication. This work has enabled the microelectronics industry to continue following Moore's Law of miniaturization for the last decade and a half. The Laboratory started a project in 1988 to demonstrate the feasibility of using the deep-ultraviolet wavelength of 193 nm for optical projection lithography (a process for producing patterned silicon wafers for the fabrication of integrated circuits). At the time, 248 nm lithography was considered the limit of wavelength reduction. This limit had been achieved as industry sought to reduce the size of microelectronic circuits by using shorter wavelengths of radiation in optical lithography.

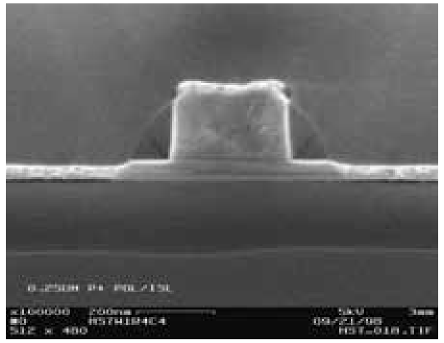
By 1993, the Laboratory had addressed challenges of the lens materials and the wafer coatings needed for 193 nm lithography. Working with the Laboratory under a subcontract, Silicon Valley Group Lithography in Wilton, Connecticut, designed and built the world's first commercial 193 nm prototype projection system. This prototype system was installed in the Microelectronics Laboratory and used to fabricate the first all-193 nm microelectronic devices and simple circuits.





Scanning electron micrographs of 200 nm transistor gates, left, and printed features, right





Left, first multiproject chip; above, scanning electron micrograph of a 250 nm transistor used in early multiproject runs

1997

Multiproject Fabrication Runs

In 1994, staff at the Microelectronics Laboratory began the development of a fully depleted silicon-on-insulator (FDSOI) complementary metal-oxide semiconductor (CMOS) process technology. Interest in this integrated-circuit fabrication technology was driven by its distinctive low-power, high-performance, and extreme-environment operational capabilities. In 1996, the Microelectronics Lab offered its original multiproject fabrication run, providing the first U.S. research access to a FDSOI CMOS process technology. This initial run contained more than 25 different circuit designs from university, government laboratory, and precompetitive industry collaborators, and set the stage for what would ultimately be more than a dozen multiproject runs that exploited the unique properties of the FDSOI CMOS technology targeting ultralow-power, RF, analog mixed-signal, and three-dimensional integrated-circuit demonstrations of interest to the research community and Lincoln Laboratory's sponsors.

Circuits from these runs have flown in space, operated in temperature environments as low at 15 mK and as high as 573 K (300°C), and helped to lay the groundwork for modern fully depleted device and circuit design techniques. In total, the Microelectronics Laboratory has fabricated more than 350 different integrated-circuit designs for more than 90 different organizations and, to-date, remains the only U.S. organization offering research access to this unique process technology.

Canada-France-Hawaii Telescope Focal Plane

1998

In 1995, a group of observatories led by the University of Hawaii's Institute for Astronomy signed a cooperative research and development agreement with Lincoln Laboratory to develop a large-area, high-sensitivity CCD imager for a new generation of focal plane arrays for astronomy. The fruits of that effort resulted in the fabrication in the Microelectronics Laboratory of large numbers of CCDs that were deployed in several observatories around the world. For two of these, the Canada-France-Hawaii Telescope (CFHT) and the W.M. Keck Observatory, both atop Mauna Kea in Hawaii, the Laboratory assembled arrays of these chips that set new standards for high sensitivity, low noise, and pixel count. The CFHT 100-megapixel array comprised 12 chips and was used for direct sky imaging, while Keck used an array of eight CCDs (67 megapixels) for a spectrograph called DEIMOS (for DEep Imaging Multi-Object Spectrograph). The DEIMOS focal plane array is still in service at the Keck Observatory, while the CFHT array is now used at the Palomar Observatory in California.

The CCD design for this program was adopted with some design changes for use in the Space Surveillance Telescope (SST) focal plane array (see page 21).

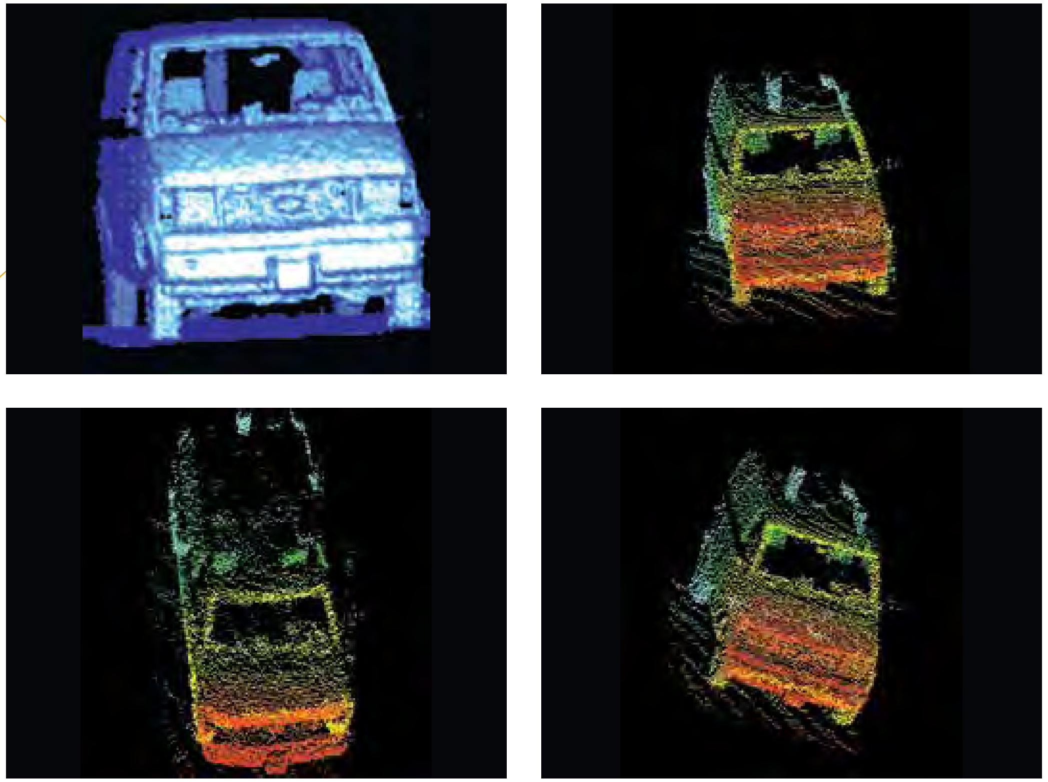
CFHT focal plane undergoing assembly; above, images captured by CFHT of two nebulae

Geiger-Mode Avalanche Photodiode Integrated Devices

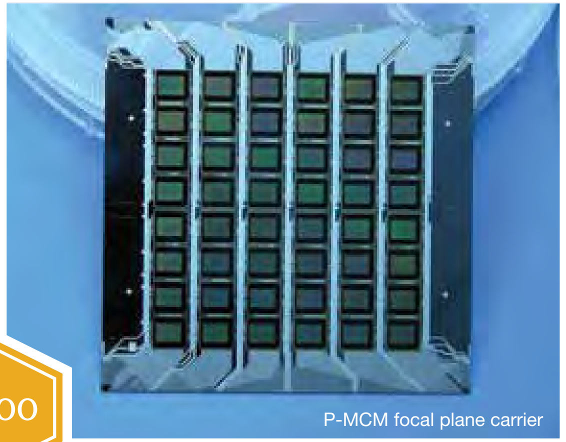
1999

The Microelectronics Laboratory developed the first arrays of single-photon-sensitive avalanche photodiodes (APDs) bonded to all-digital integrated circuits. An APD is a high-sensitivity, high-speed semiconductor electronic device that converts light to electricity. This technology enables the development of imaging devices that can count or digitally time-stamp arriving photons. The pixel architecture is based on a simple scheme to convert photons to bits, eliminating complex and noisy analog sensing circuitry. Lincoln Laboratory also developed some of the first large-sized imaging arrays of APDs fabricated in the indium-gallium-aluminum-phosphide–material system. This material system is sensitive at a 1-micron wavelength and longer, where small-sized and powerful laser sources are available.

The Laboratory's work has extended APD technology to large-area arrays of single-photon-counting detectors that have become the foundation of new communications, three-dimensional (3D) imaging, and foliage penetration concepts. The Laboratory has also demonstrated an array of Geiger-mode avalanche photodiodes for adaptive optics uses. Future work will integrate these arrays in telescope systems, speed up the image acquisition in large sky surveys, and improve imaging performance.



3D imaging of a van



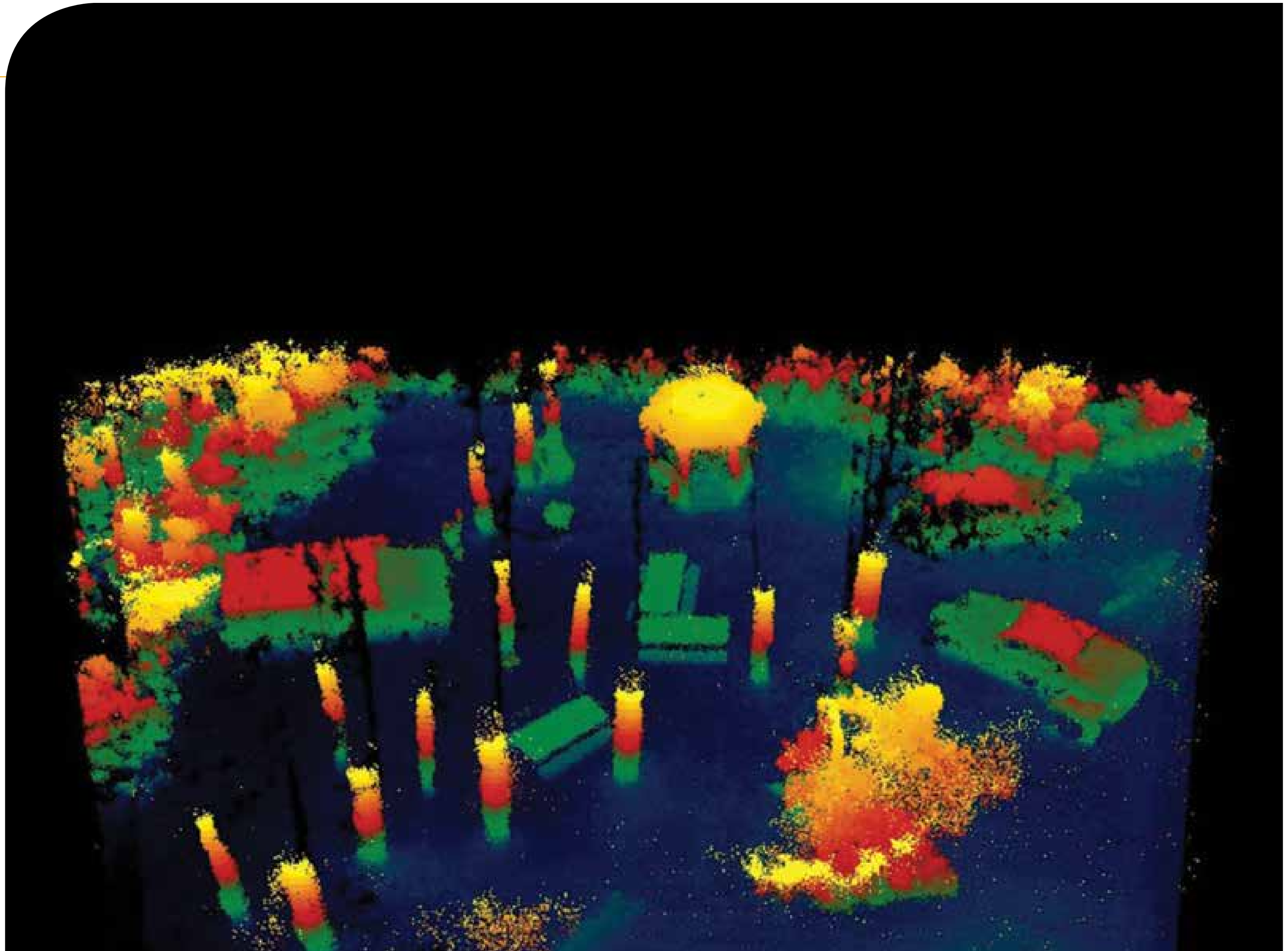
P-MCM focal plane carrier

2000

Precision-Multichip Module

The precision-multichip module (P-MCM) was developed to be a high-performance packaging solution for digital, mixed-signal and high-performance analog circuits. Its defining characteristic is the use of CMOS-like back-end processing techniques, including chemical-mechanical planarization and damascene vias. Several variations of the process have been developed and successfully deployed in system demonstrations. The high-performance analog variation uses five aluminum metal layers, separated by a silicon dioxide intermetal dielectric. The process includes embedded passive devices. A resistor layer and an anodized aluminum layer between the ground and power planes at the bottommost layers of the metal stack provide an embedded capacitor layer. The process also supports a thick, gold top metal and silicon micromachining beneath the inductors to enhance their quality factors.

P-MCM technology has been used in a number of applications and demonstrated in field-tested prototype systems. The analog P-MCM process has been used on an X-band radar receiver module and other microwave applications. Here, silicon-germanium integrated circuits have been integrated with embedded filters and bias decoupling circuits to form complete up and down block converter subsystems. These subsystems are combined on a printed circuit board with digital waveform generation and received signal processing circuits to form advanced prototype radars. A digital variant of the P-MCM process with only three metal layers has been successfully used for imager applications. Forty-eight commercial imager integrated circuits have been integrated on the MCM, with their outputs digitally combined in off-MCM field-programmable gate arrays. These MCMs were used as the core of the Multiaperture Sparse Imager Video System gigapixel imaging system.



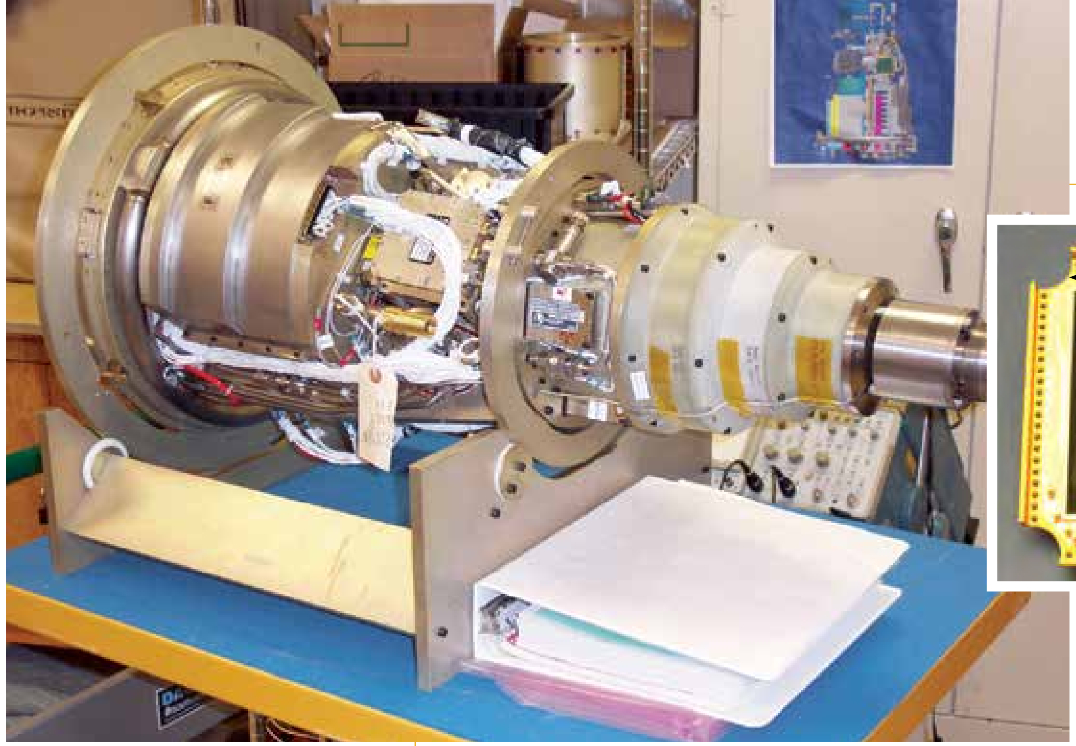
The foliage penetration topological image of a wooded area is color-coded for height, yellow is tall end of spectrum

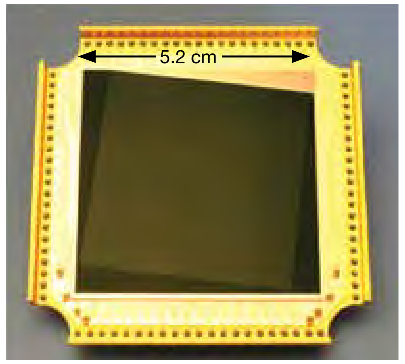
Flash Ladar

2002

Laser radar (ladar) systems take 3D images of scenes by transmitting light pulses and measuring how long it takes for them to return. Traditionally, 3D imaging was accomplished by mechanically scanning a single light spot over the scene. Lincoln Laboratory developed a ladar system that can acquire images of an entire scene with a single laser flash. The concept combines two enabling technologies developed at the Laboratory: compact high-energy microchip lasers and single-photon-sensitive avalanche photodiode arrays, with the latter fabricated in the Microelectronics Laboratory. After successfully demonstrating the flash ladar at a competitive field trial at Eglin Air Force Base in Florida, the Laboratory went on to demonstrate other flash ladar systems for foliage penetration and terrain mapping.

Left, dense foliage through which the ladar system "looked"; above, the gazebo, vehicles, and trees here are identifiable in the ladar image





Left, interior of FASP unit; above, packaged 448 × 448 imager

2004

Midcourse Fly-Away Sensor Package

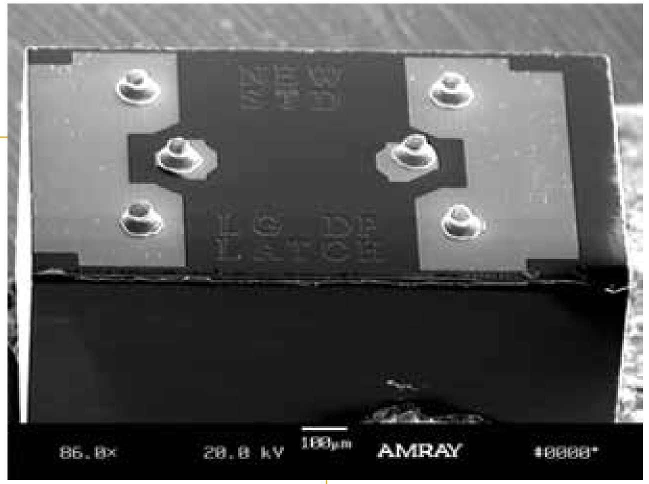
Lincoln Laboratory developed the Midcourse Fly-Away Sensor Package (MFASP), an autonomous vehicle released from a host spacecraft and flown in formation with ballistic missile test payloads to capture and transmit images of test objects. An important intended application for the MFASP platform was the video capture of a high-speed (10–14 km/s) missile intercept of a target payload. Achieving this goal required researchers in the Microelectronics Laboratory to develop a large-format (448 × 448 pixels), high-speed, CCD imager to capture snapshots of the missile intercept event from a distance of approximately 1 km at speeds from 10 to 15 thousand frames per second. The imager architecture, designed to capture and store 50 frames at speeds from 1 kHz to 2 MHz for subsequent readout, leads to an unusual tilted pixel array. This same high-speed imager has been used by Lawrence Livermore National Laboratory for high-energy explosives analysis and by the U.S. Army Armament Research, Development and Engineering Center for small-caliber projectile analysis.

MFASP was a major upgrade to the first Fly-Away Sensor Package. Design modifications enabled a variety of significant capability enhancements besides the imager: telemetry with advanced data compression and forward error correction; an onboard global positioning system; an extended operating time of up to 30 minutes; space for developmental sensors such as microbolometers and range finders; and advanced control algorithms to achieve multiple viewing aspects in a given mission.

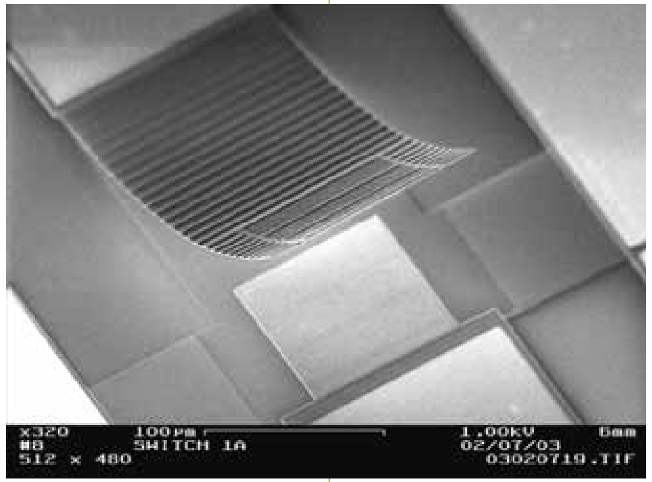
2005

RF Microelectromechanical Switches

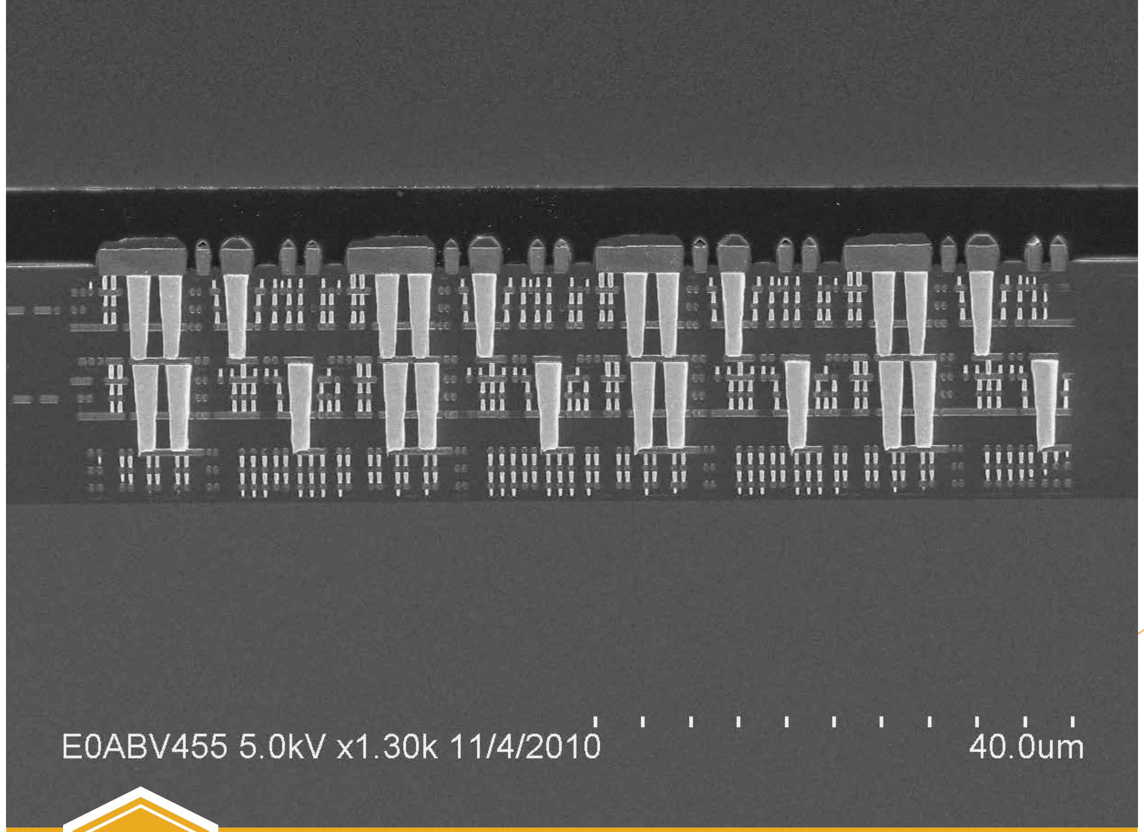
Radio-frequency microelectromechanical switches (RFMEMS) use micron-scale mechanical elements to create switches that can have very high impedance in the off state and only fractions of an ohm in the on state. These capabilities are increasingly important for multiantenna and radio systems found in cell phones and frequently in complex communications systems for the Department of Defense. Lincoln Laboratory utilized the Microelectronics Laboratory to develop and manufacture CMOS-compatible, fully packaged RFMEM capacitive switches and phase shifters that have the lowest insertion loss and highest on-state to off-state capacitance ratio of any reported RFMEM switches. These devices were tested in parallel to beyond 450 billion switch cycles over three years, outlasting the RF test equipment in reliability. The excellent performance comes from the reliable fabrication of a unique curled cantilever design made possible by the control and advanced processing capabilities of the Microelectronics Laboratory. The precisely controlled residual stress of the layers causes the cantilever to curl up from the substrate in the off state, and electrostatic actuation pulls the cantilever to the substrate for high down-state capacitance in the on state. This technology has been successfully transferred to a MEMS manufacturing company for production for Department of Defense applications and has recently been licensed for commercial production.



Wafer-scale packaged RFMEMS device



Scanning electron micrograph of RFMEM switch



Cross section of a three-tier, 3D integrated circuit

2006

3D Integrated Circuit

Three-dimensional logic one (3DL1), the first of three Defense Advanced Research Projects Agency (DARPA)–sponsored 3D multiproject programs, provided the circuit-design community with the first research access to a three-tier 3D circuit process, many years in advance of industry availability. This 3D technology developed in the Microelectronics Laboratory incorporated three active transistor layers, eleven metal layers, and the world's highest density of 3D circuit-layer-to-circuit-layer interconnects. 3DL1 allowed Lincoln Laboratory to engage Department of Defense designers in the exploration of circuit applications enabled by 3D integration, not only in design, but also by test and characterization of fully fabricated circuits. More than 100 3D designs submitted by approximately 50 government, academic, and industry design teams were fabricated over the course of the 3D multiproject runs.

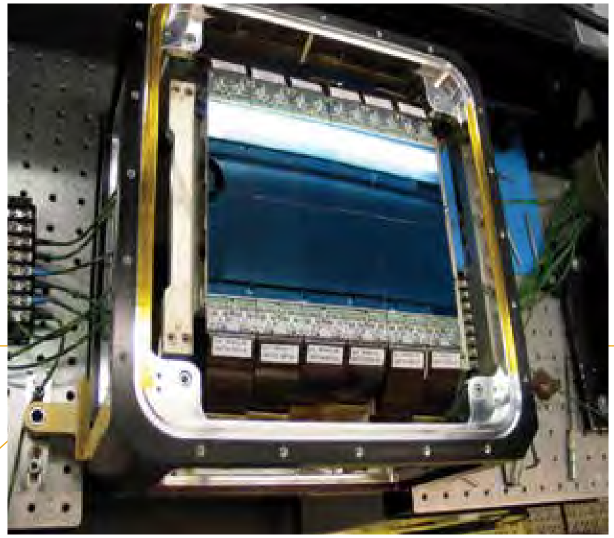
2007

Panoramic Survey Telescope and Rapid Response System

The Panoramic Survey Telescope and Rapid Response System (Pan-STARRS) 1.4-gigapixel focal plane array (FPA) built by Lincoln Laboratory is currently the world's largest and most advanced FPA. It utilizes a unique architecture called the orthogonal-transfer array (OTA), which the Laboratory developed in collaboration with the University of Hawaii's Institute for Astronomy, which built and operates Pan-STARRS. An OTA uses an array of orthogonal CCDs, fabricated in the Microelectronics Laboratory, to compensate electronically for two-dimensional image motion at the pixel level. To enable high-quality imaging, the Pan-STARRS FPA is equipped with 60 OTAs, each of which comprises an 8 × 8 array of orthogonal-transfer CCDs.

This large focal plane was installed in the prototype Pan-STARRS telescope in Hawaii and has been used in regular science observations since 2009. The prototype focal plane and three additional ones will compose the full Pan-STARRS, which will be able to image a large percentage of the night sky with great sensitivity and will be used to detect Earth-approaching asteroids and comets that could be dangerous to the planet.

Pan-STARRS images: top, the first prototype observatory on Haleakala, Hawaii; middle, galaxy M51 imaged by Pan-STARRS; bottom, focal plane array



Focal surface array for the Space Surveillance Telescope (facing page)

2008

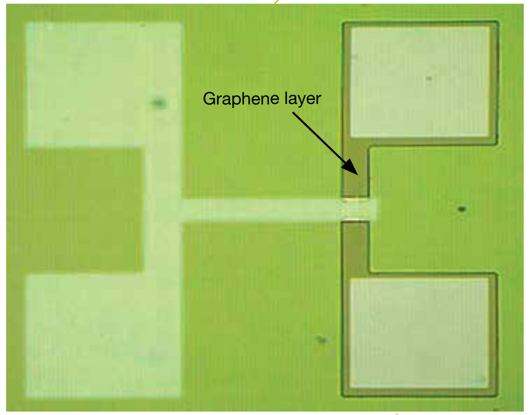
Space Surveillance Telescope

The Space Surveillance Telescope (SST) installed at the White Sands Missile Range in New Mexico provides an unprecedented wide-angle view of deep space. The SST is an advanced ground-based optical system designed to enable detection and tracking of faint objects in space while providing rapid, wide-area search capability. These capabilities of the system were made possible by utilizing a unique, spherically curved charge-coupled-device imager, developed in the Microelectronics Laboratory. The curving of silicon, which is usually considered a brittle material, to a spherical surface allowed integration of the detectors with a very wide-field-of-view, large-aperture (3.5-meter diameter) fast (f/1.0) telescope. The SST program was initiated in 2002 under the sponsorship of the Defense Advanced Research Projects Agency (DARPA). In February 2011, the telescope achieved “first light.” The SST is transitioning to the Air Force as part of its expanded Space Surveillance Network.

2009

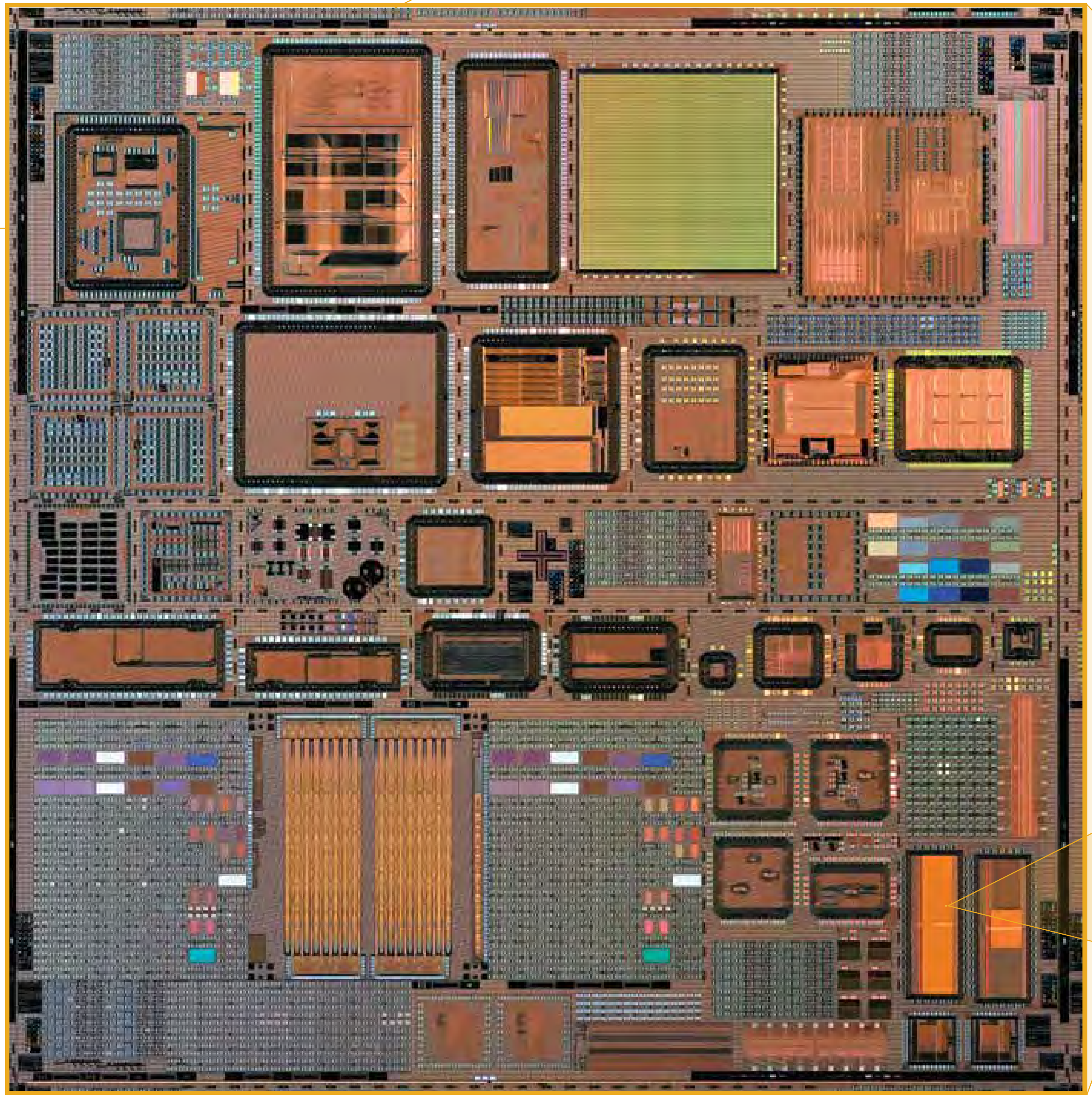
Graphene Transistors

In 2007, Lincoln Laboratory initiated one of the world’s first efforts in building graphene-based field-effect transistors. The single atomic sheet of graphite, graphene, has unique electrical and material properties. Graphene combines high electron mobility, subnanometer conduction-layer thickness, zero band-gap, and unique chemical sensitivity. One exciting application of graphene is as a replacement for silicon in transistors, potentially revolutionizing the silicon-based electronics industry. Researchers at the Laboratory, working in collaboration with scientists at MIT, were able to build the first top-gated graphene transistor, demonstrating good turn-on characteristics and a high mobility.



Top-gated graphene transistor

A paper on the innovative graphene devices developed at the Laboratory received the George E. Smith Award for the best technical paper published in *IEEE Electron Device Letters* in 2009. The pioneering graphene work at the Laboratory has helped the research community understand the integration and material challenges in graphene electronics, and has led to insights into other two-dimensional electronic materials, such as molybdenum disulfide.

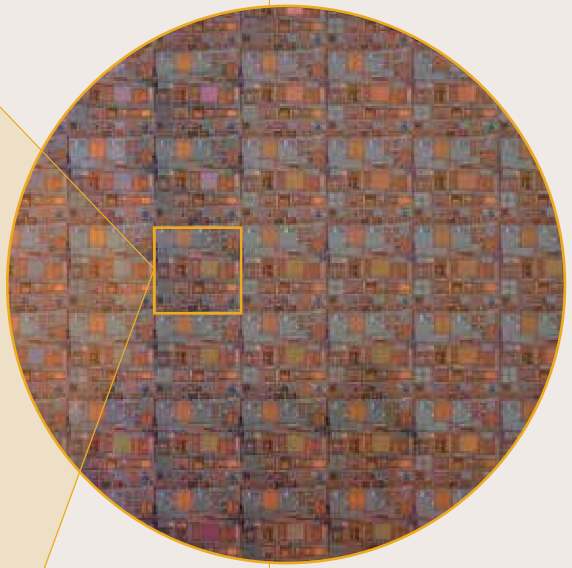


Completed 22 mm x 22 mm xLP multiproject die

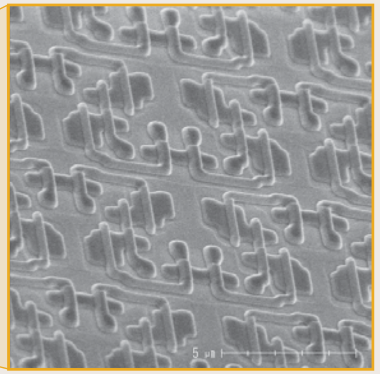
Ultra-Low-Power CMOS

2010

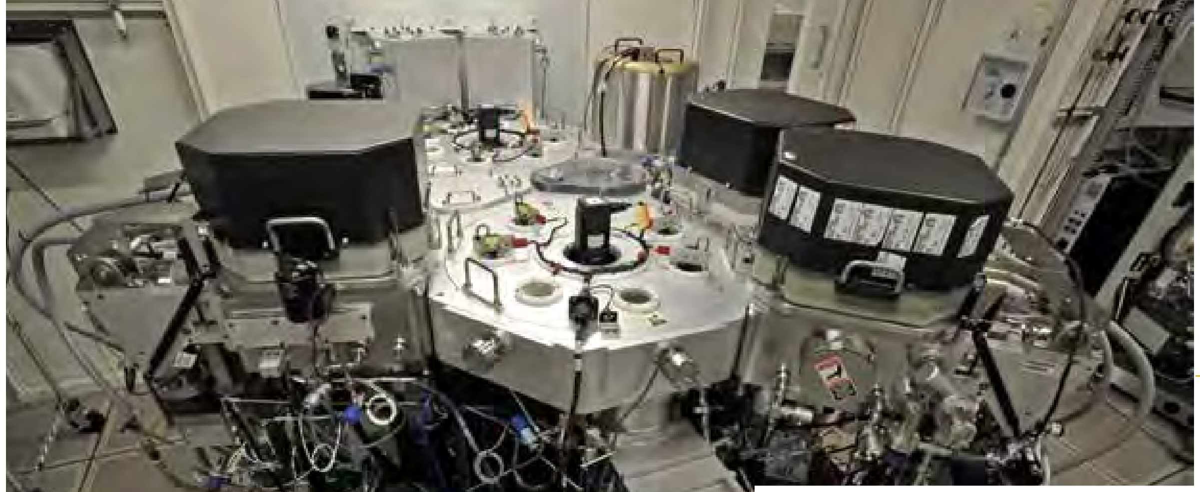
The ultra-low-power (or xLP) CMOS program is developing a silicon microelectronics technology capable of providing order-of-magnitude energy savings over commercially available microelectronics. Building upon the 1990s seminal research conducted in the Microelectronics Laboratory on fully depleted silicon-on-insulator (FDSOI) transistor technology, xLP CMOS technology is based on transistors specifically engineered for optimal operation at voltages as low as 300 mV. At such a low voltage, both dynamic and static circuit power dissipation are reduced significantly, enabling an order-of-magnitude increase in either battery life or processing power in energy-starved systems, such as unattended sensors, space-based systems, wearable electronics, or implantable biomedical sensors. Extremely low-energy circuit operation also opens the possibility of batteryless perpetual operation of devices powered through energy-harvesting techniques. Several circuit demonstrations of xLP technology have been performed, including fabrication of the world's largest extremely low-voltage field-programmable gate array, which promises to provide an ultra-low-power flexible computing platform for government systems.



Completed xLP wafer



Scanning electron micrograph of a static random-access memory cell



2011

Large image, metal-deposition tools; inset, technician inspecting a wafer

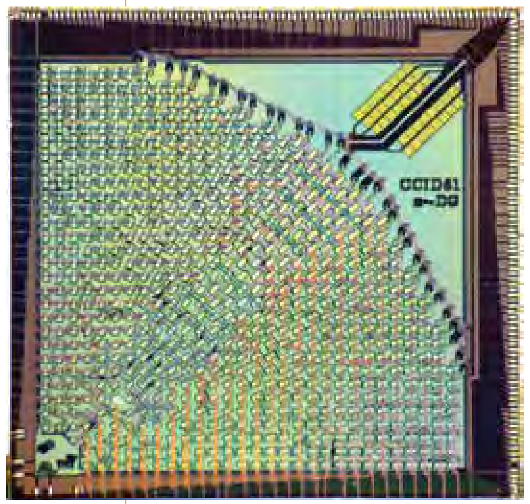
200-Millimeter Upgrade

Spring 2011 saw the completion of a major three-year recapitalization of the Microelectronics Laboratory to convert the entire facility to 200 mm–diameter wafer processing with sub-90 nm feature-size capability. The 200 mm conversion was a significant undertaking that required the replacement of more than 80 pieces of major process equipment with a total market value greater than $58 million. Over the three years, the Microelectronics Laboratory team successfully accomplished a phased conversion, allowing them to continue delivering 150 mm–diameter wafer-based devices into important Laboratory programs while the new 200 mm tools were brought on line, a task similar to trying to change the wheels on a bus as it is rolling down the highway. The facility was only off line for two one-month-long periods during the entire conversion process. By fall 2011, the first complex circuits on the new 200 mm–diameter wafer tool were completing fabrication and demonstrating the tighter feature sizes, enhanced process control, and higher yields associated with the more modern equipment set. Within the broader Department of Defense, Department of Energy, and government research laboratory community, the upgraded Microelectronics Laboratory stands out as offering the best combination of tool set, process capabilities, and staff expertise in the silicon microelectronics area.

Polar Imager

2012

The Thirty-Meter Telescope is currently being constructed at Mauna Kea, Hawaii, by the TMT Observatory Corporation, a partnership of CalTech, the University of California, and an association of Canadian universities. The new telescope will increase the sensitivity of astronomical observations by 10- to 100-fold over the current capability. To achieve this increase, it is necessary to compensate for the aberrations introduced by the atmosphere. The CCD-based Polar Coordinate Detector will be used as part of the adaptive optics wavefront sensing system of Shack-Hartmann (SH) wavefront sensors in conjunction with sodium-wavelength laser guide stars (LGS). The large number of CCD subapertures required and the significant perspective elongation of the LGS image are both challenges to SH wavefront sensor design. To surmount these obstacles, a new detector design was implemented. The first-generation proof-of-concept detector covers 90° of the arc generated by the LGS and consists of 800 subapertures. In order to meet the 800-frames/second readout rate, each frame is stored in a serpentine serial register running between the individual subapertures. Each subaperture is oriented along a polar grid to obtain the maximum information from the elongated LGS images. Significant design and photolithography challenges were addressed in fabricating these imagers in the Microelectronics Laboratory. Plans are under way to transition the design to cover the full 360° field of view.



Top, rendering of the Thirty-Meter Telescope; bottom, the polar coordinate detector

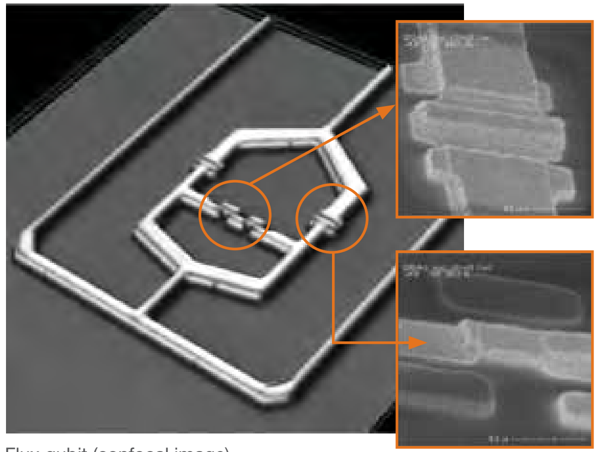
Superconducting Qubits

2013

Lincoln Laboratory's superconducting qubit (quantum bit) efforts grew out of earlier work in the 1980s and 1990s on the fabrication of digital superconducting circuits. These devices are made with thin-film fabrication techniques that are similar to the CMOS back-end process. The core element in these devices is the two-terminal, superconducting-insulating-superconducting, Josephson junction. For proper qubit operation, the diameter of this junction must be less than 400 nm. The Laboratory successfully developed the techniques to fabricate these devices with both optical and electron-beam lithography. The niobium-based, multilayer qubit with optically defined Josephson junctions, shown in the figure, had an order-of-magnitude longer coherence time than similar qubits being produced in the community.

Today, researchers in the Microelectronics Laboratory are using electron-beam lithography to make superconducting qubits with molecular-beam-epitaxy (MBE)–grown metals that have fewer defects than sputtered films. Qubits are being produced with state-of-the-art lifetimes greater than 100 µs. Digital superconducting circuits are also being produced in the Microelectronics Laboratory. Building on the optically defined Josephson junction fabrication techniques developed for the superconducting qubits, the process supports eight metal layers with feature sizes as small as 500 nm and junctions with diameters of 700 nm. This digital superconducting circuit process is currently the most advanced in the world.

Fabrication on 200 mm wafers



Flux qubit (confocal image)

Josephson junctions

U.S. Patents on Work from the Microelectronics Laboratory

2013

Wide Band and Radio Frequency Waveguide and Hybrid Integration in a Silicon Package
Inventors: Carl O. Bozler, Jeremy Muldavin, Peter W. Wyatt, Craig L. Keast, and Steven Rabe
Date issued: 19 November 2013
U.S. Patent no.: 8,587,106

Directed Material Assembly
Inventors: Theodore H. Fedynyshyn and Richard Kingsborough
Date issued: 8 October 2013
U.S. Patent no.: 8,551,566

Electronic Shutter with Photogenerated Charge Extinguishment Capability for Back-Illuminated Image Sensors
Inventor: Barry E. Burke
Date issued: 17 September 2013
U.S. Patent no.: 8,536,625

Waveguide Coupler Having Continuous Three-Dimensional Tapering
Inventors: Steven J. Spector, Reuel B. Swint, and Milos Popovic
Date issued: 25 June 2013
U.S. Patent no.: 8,472,766

Micro-electromechanical Tunneling Switch
Inventors: Carl O. Bozler, Craig L. Keast, and Jeremy Muldavin
Date issued: 30 April 2013
U.S. Patent no.: 8,432,239

CMOS Readout Architecture and Method for Photon-Counting Arrays
Inventors: Brian F. Aull, Matthew J. Renzi, Robert K. Reich, and Daniel R. Schuette
Date issued: 23 April 2013
U.S. Patent no.: 8,426,797

Optical Limiting Using Plasmonically Enhancing Nanoparticles
Inventors: Vladimir Liberman and Mordechai Rothschild
Date issued: 1 January 2013
U.S. Patent no.: 8,345,364

2012

Single-Electron Detection Method and Apparatus for Solid-State Intensity Image Sensors with a Charge-Metering Device
Inventors: David C. Shaver, Bernard B. Kosicki, Robert K. Reich, Dennis D. Rathman, Daniel R. Schuette, and Brian F. Aull
Date issued: 4 December 2012
U.S. Patent no.: 8,324,554

Inorganic Resist Sensitizer
Inventors: Theodore H. Fedynyshyn and Russell B. Goodman
Date issued: 4 December 2012
U.S. Patent no.: 8,323,866

Resist Sensitizer
Inventor: Theodore H. Fedynyshyn
Date issued: 17 April 2012
U.S. Patent no.: 8,158,338

Multi-tone Resist Compositions
Inventor: Theodore H. Fedynyshyn
Date issued: 7 February 2012
U.S. Patent no.: 8,110,339

High Fill-Factor Avalanche Photodiode
Inventors: Matthew J. Renzi, Brian F. Aull, Robert K. Reich, and Bernard B. Kosicki
Date issued: 10 January 2012
U.S. Patent no.: 8,093,624

2011

System and Method for Providing Amplitude Spectroscopy of a Multilevel Quantum System
Inventors: David Berns, Karl K. Berggren, Leonid S. Levitov, Mark Rudner, Terry P. Orlando, Sergio Valenzuela, and William D. Oliver
Date issued: 22 March 2011
U.S. Patent no.: 7,912,656

System and Method for Providing a High Frequency Response Silicon Photodetector
Inventors: Michael W. Geis, Steven J. Spector, Donna M. Lennon, Matthew E. Grein, Robert T. Schulein, Jung U. Yoon, Franz Xaver Kaertner, Fuwan Gan, and Theodore M. Lyszczarz
Date issued: 1 February 2011
U.S. Patent no.: 7,880,204

2010

Digital Photon-Counting Geiger-Mode Avalanche Photodiode Solid-State Monolithic Intensity Imaging Focal-Plane with Scalable Readout Circuitry
Inventors: Alvin Stern, Brian F. Aull, Bernard B. Kosicki, Robert K. Reich, Bradley J. Felton, David C. Shaver, Andrew H. Loomis, and Douglas J. Young
Date issued: 28 December 2010
U.S. Patent no.: 7,858,917

Device for Subtracting or Adding Charge in a Charge-Coupled Device
Inventor: Michael P. Anthony
Date issued: 6 July 2010
U.S. Patent no.: 7,750,962

Immersion Fluids for Lithography
Inventors: Theodore H. Fedynyshyn and Indira Pottebaum
Date issued: 29 June 2010
U.S. Patent no.: 7,745,102

Method and System of Lithography Using Masks Having Gray-Tone Features
Inventors: Brian M. Tyrrell and Michael Fritze
Date issued: 26 January 2010
U.S. Patent no.: 7,651,821

2009

Multi-element Optical Detectors with Sub-wavelength Gaps
Inventors: Eric A. Dauler, Andrew J. Kerman, Karl K. Berggren, Vikas Anant, and Joel K.W. Yang
Date issued: 29 December 2009
U.S. Patent no.: 7,638,751

Contrast Enhancing Layers
Inventor: Theodore H. Fedynyshyn
Date issued: 24 November 2009
U.S. Patent no.: 7,622,246

Method for Photolithography Using Multiple Illuminations and a Single Fine Feature Mask
Inventors: Michael Fritze and Brian M. Tyrrell
Date issued: 1 September 2009
U.S. Patent no.: 7,583,360

Method and System for Distribution of an Exposure Control Signal for Focal Plane Arrays
Inventors: Robert K. Reich, Bernard B. Kosicki, Dennis D. Rathman, Richard Osgood, Michael Rose, R. Allen Murphy, and Robert Berger
Date issued: 10 March 2009
U.S. Patent no.: 7,501,634

Light Modulating Mirror Device and Array
Inventors: Carl O. Bozler, W. Gregory Lyons, and Jeremy Muldavin
Date issued: 3 February 2009
U.S. Patent no.: 7,484,857

2008

High-Speed Electrical Interconnect Using an Optically Distributed Carrier Signal
Inventors: Brian M. Tyrrell and Robert K. Reich
Date issued: 22 April 2008
U.S. Patent no.: 7,363,018

2007

Method and System of Lithography Using Masks Having Gray-Tone Features
Inventors: Michael Fritze and Brian M. Tyrrell
Date issued: 11 December 2007
U.S. Patent no.: 7,306,881

Micro-electromechanical Switch Designs
Inventors: Carl O. Bozler, Shaun R. Berry, Jeremy Muldavin, and Craig L. Keast
Date issued: 15 May 2007
U.S. Patent no.: 7,218,191

High-Yield Single-Level Gate Charge-Coupled Device Design and Fabrication
Inventors: Barry E. Burke and Vyshnavi Suntharalingam
Date issued: 15 May 2007
U.S. Patent no.: 7,217,601

Device for Subtracting or Adding Charge in a Charge-Coupled Device
Inventor: Michael P. Anthony
Date issued: 3 April 2007
U.S. Patent no.: 7,199,409

2006

Adjustable CCD Charge Splitter
Inventor: Michael P. Anthony
Date issued: 26 December 2006
U.S. Patent no.: 7,154,134

Resist with Reduced Line Edge Roughness
Inventor: Theodore H. Fedynyshyn
Date issued: 26 December 2006
U.S. Patent no.: 7,153,630

High-Speed, High-Sensitivity Charge-Coupled Device with Independent Pixel Control of Charge Collection and Storage
Inventors: Robert K. Reich, Bernard B. Kosicki, Jonathan C. Twichell, and Dennis D. Rathman
Date Issued: 15 August 2006
U.S. Patent no.: 7,091,530

Fabrication of a High-Precision Blooming Control Structure for an Image Sensor
Inventors: Barry E. Burke and Eugene D. Savoye
Date issued: 11 July 2006
U.S. Patent no.: 7,074,639

Charge-Domain A/D Converter Employing Multiple Pipelines for Improved Precision
Inventor: Michael P. Anthony
Date issued: 21 March 2006
U.S. Patent no.: 7,015,854

2005

Sub-Ranging Pipelined Charge-Domain Analog-to-Digital Converter with Improved Resolution and Reduced Power Consumption
Inventor: Michael P. Anthony
Date issued: 6 December 2005
U.S. Patent no.: 6,972,707

Resist with Reduced Line Edge Roughness
Inventor: Theodore H. Fedynyshyn
Date issued: 30 August 2005
U.S. Patent no.: 6,934,007

Method for Photolithography Using Multiple Illuminations and a Single Fine Feature Mask
Inventors: Michael Fritze and Brian M. Tyrrell
Date issued: 23 August 2005
U.S. Patent no.: 6,934,007

Surface Modified Encapsulated Inorganic Resist
Inventor: Theodore H. Fedynyshyn
Date issued: 5 July 2005
U.S. Patent no.: 6,913,865

Rolling Shutter Optical Switch Device with Latch Electrode and Slits in Shutter
Inventors: Carl O. Bozler and Steven Rabe
Date issued: 14 June 2005
U.S. Patent no.: 6,907,153

Method and System of Lithography Using Masks Having Gray-Tone Features
Inventors: Michael Fritze and Brian M. Tyrrell
Date issued: 26 April 2005
U.S. Patent no.: 6,884,551

Method and Apparatus for Reducing Driver Count and Power Consumption in Micromechanical Flat Panel
Inventor: Ernest Stern
Date issued: 12 April 2005
U.S. Patent no.: 6,879,307

High Sensitivity X-Ray Photoresist
Inventor: Theodore H. Fedynyshyn
Date issued: 29 March 2005
U.S. Patent no.: 6,872,504

2004

Rolling Shutter Optical Switch Device with Dimples on Shutter Annular Rim at Optical Port and Shortened Shutter Attachment Edge
Inventors: Carl O. Bozler, Dale C. Flanders, Peter S. Whitney, and Steven Rabe
Date issued: 7 December 2004
U.S. Patent no.: 6,829,399

Method of Design and Fabrication of Integrated Circuits Using Regular Arrays and Gratings
Inventors: Brian M. Tyrrell and Michael Fritze
Date issued: 16 November 2004
U.S. Patent no.: 6,818,389

Resist Materials for 157-nm Lithography
Inventor: Theodore H. Fedynyshyn
Date issued: 9 November 2004
U.S. Patent no.: 6,815,145

Low Absorbing Resists for 157 nm Lithography
Inventors: Michael Sworin, Roderick R. Kunz, Roger S. Sinta, and Theodore H. Fedynyshyn
Date issued: 21 September 2004
U.S. Patent no.: 6,794,109

Encapsulated Inorganic Resists
Inventor: Theodore H. Fedynyshyn
Date issued: 31 August 2004
U.S. Patent no.: 6,783,914

Resist Methods and Materials for UV and Electron-Beam Lithography with Reduced Outgassing
Inventor: Theodore H. Fedynyshyn
Date issued: 20 January 2004
U.S. Patent no.: 6,680,157

2003

Microelectro-mechanical System Actuator Device and Reconfigurable Circuits Utilizing Same
Inventors: Carl O. Bozler, Lawrence J. Kushner, Richard G. Drangmeister, and Robert J. Parr
Date issued: 11 November 2003
U.S. Patent no.: 6,646,525

2002

Large Field of View CCD Imaging System
Inventor: Eugene D. Savoye
Date issued: 3 December 2002
U.S. Patent no.: 6,489,992

Resist Materials for 157-nm Lithography
Inventor: Theodore H. Fedynyshyn
Date issued: 22 October 2002
U.S. Patent no.: 6,468,712

Dynamic Double Sampling Charge Integrator
Inventor: Susanne A. Paul
Date issued: 8 October 2002
U.S. Patent no.: 6,463,566

Thermophoretic Pump and Concentrator
Inventors: Margaret B. Stern, Michael W. Geis, and Roderick R. Kunz
Date issued: 2 July 2002
U.S. Patent no.: 6,413,781

2001

High-Precision Blooming Control Structure for an Image Sensor
Inventors: Barry E. Burke and Eugene D. Savoye
Date issued: 18 December 2001
U.S. Patent no.: 6,331,873

Pipelined Oversampling A/D Converter
Inventor: Susanne A. Paul
Date issued: 6 March 2001
U.S. Patent no.: 6,198,417

Satellite Navigation Receiver for Precise Relative Positioning in Real Time
Inventors: Brian P. Burke, Michael M. Pratt, and Pratap Misra
Date issued: 30 January 2001
U.S. Patent no.: 6,181,274

2000

Microelectro-mechanical System Actuator Device and Reconfigurable Circuits Utilizing Same
Inventors: Carl O. Bozler, Lawrence J. Kushner, Richard G. Drangmeister, and Robert J. Parr
Date issued: 3 October 2000
U.S. Patent no.: 6,127,908

Laser Induced Cutting of Buried Metal Interconnect
Inventors: Joseph Bernstein and Zhihui Duan
Date issued: 2 May 2000
U.S. Patent no.: 6,057,221

1999

Surface Emission Cathodes
Inventors: Jonathan C. Twichell, Keith E. Krohn, Michael W. Geis, Nikolay N. Efremow Jr., and Theodore M. Lyszczarz
Date issued: 26 October 1999
U.S. Patent no.: 5,973,451

Spatial Light Modulator
Inventors: Carl O. Bozler and Steven Rabe
Date issued: 28 September 1999
U.S. Patent no.: 5,959,763

Linearized Optical Sampler
Inventors: Jonathan C. Twichell and Roger Helkey
Date issued: 21 September 1999
U.S. Patent no.: 5,955,875

Vapor Deposition of Polymer Films for Photolithography
Inventor: Mark W. Horn
Date issued: 20 July 1999
U.S. Patent no.: 5,925,494

Interconnection Technique for Hybrid Integrated Devices
Inventors: Barry E. Burke and Bernard B. Kosicki
Date issued: 18 May 1999
U.S. Patent no.: 5,904,495

Structure and Fabrication of Electron-Emitting Devices Utilizing Electron-Emissive Particles Which Typically Contain Carbon
Inventors: Christopher J. Curtin, George R. Brandes, John M. Macaulay, Jonathan C. Twichell, Michael W. Geis, and Robert M. Duboc Jr.
Date issued: 4 May 1999
U.S. Patent no.: 5,900,301

Polymeric Anti-reflective Compounds
Inventor: Roderick R. Kunz
Date issued: 6 April 1999
U.S. Patent no.: 5,891,959

Low-Light-Level Imaging and Image Processing
Inventors: Alan N. Gove, Allen M. Waxman, Andrew H. Loomis, Barry E. Burke, Bernard B. Kosicki, David A. Fay, Eugene D. Savoye, James Carrick, James A. Gregory, Robert K. Reich, Robert W. Mountain, and William H. McGonagle
Date issued: 9 March 1999
U.S. Patent no.: 5,880,777

1998

Reduction of Trapping Effects in Charge Transfer Devices
Inventor: Barry E. Burke
Date issued: 11 August 1998
U.S. Patent no.: 5,793,070

Spatial Light Modulator
Inventors: Carl O. Bozler and Steven Rabe
Date issued: 21 July 1998
U.S. Patent no.: 5,784,189

Micromechanical Optical Switch and Flat Panel Display
Inventor: Ernest Stern
Date issued: 23 June 1998
U.S. Patent no.: 5,771,321

Integrated Beam Forming and Focusing Processing Circuit for Use in an Ultrasound Imaging System
Inventor: Alice M. Chiang
Date issued: 9 June 1998
U.S. Patent no.: 5,763,785

Multidirectional Transfer Charge-Coupled Device
Inventors: Barry E. Burke, Eugene D. Savoye, and John Tonry
Date issued: 2 June 1998
U.S. Patent no.: 5,760,431

Charge-Domain Generation and Replication Devices
Inventor: Susanne A. Paul
Date issued: 7 April 1998
U.S. Patent no.: 5,736,757

Charge Modulation Device
Inventors: Bernard B. Kosicki, Eugene D. Savoye, and Robert K. Reich
Date issued: 27 January 1998
U.S. Patent no.: 5,712,498

1997

Method of Producing Sheets of Crystalline Material and Devices Made Therefrom
Inventors: Carl O. Bozler, John C. Fan, and Robert W. McClelland
Date issued: 14 October 1997
U.S. Patent no.: 5,676,752

Sub-Octave Bandpass Optical Remote Antenna Link Modulator and Method Therefor
Inventors: Frederick O'Donnell, Gary E. Betts, and Kevin G. Ray
Date issued: 25 March 1997
U.S. Patent no.: 5,615,037

Polymeric Anti-reflective Compounds
Inventor: Roderick R. Kunz
Date issued: 28 January 1997
U.S. Patent no.: 5,597,868

1996

Method of Producing Sheets of Crystalline Material and Devices Made Therefrom
Inventors: Carl O. Bozler, John C. Fan, and Robert W. McClelland
Dates issued: 31 December 1996; 27 August 1996
U.S. Patent nos.: 5,588,994; 5,549,747

Charge-to-Digital Converter
Inventor: Susanne A. Paul
Date issued: 26 November 1996
U.S. Patent no.: 5,579,007

Charge Domain Bit-Serial Multiplying Digital-Analog Converter
Inventor: Alice M. Chiang
Date issued: 10 September 1996
U.S. Patent no.: 5,555,200

Single Chip Adaptive Filter Utilizing Updatable Weighting Techniques
Inventor: Alice M. Chiang
Date issued: 9 July 1996
U.S. Patent no.: 5,535,150

1995

Ionic Liquid-Channel Charge-Coupled Device
Inventors: Michael W. Geis, Nancy Geis, and Stephanie Gajar
Date issued: 26 December 1995
U.S. Patent no.: 5,479,035

Microstructure Arrays and Methods for the Fabrication Thereof
Inventors: Anthony R. Forte and Mordechai Rothschild
Date issued: 25 July 1995
U.S. Patent no.: 5,435,887

A Monolithic Capillary Electrophoretic Device
Inventors: Michael W. Geis and Stephanie Gajar
Date issued: 4 July 1995
U.S. Patent no.: 5,429,734

Voltage Programmable Links Programmed with Low-Current Transitions
Inventors: Jack I. Raffel and Simon S. Cohen
Date issued: 14 February 1995
U.S. Patent no.: 5,390,141

1994

An Ionic Liquid-Channel Charge-Coupled Device
Inventors: Michael W. Geis, Nancy Geis, and Stephanie Gajar
Date issued: 20 December 1994
U.S. Patent no.: 5,374,834

Method of Producing Sheets of Crystalline Material and Devices Made Therefrom
Inventors: Carl O. Bozler, John C. Fan, and Robert W. McClelland
Date issued: 8 November 1994
U.S. Patent no.: 5,362,682

1993

Integrated Electronic Shutter for Charge-Coupled Devices
Inventors: Bernard B. Kosicki, Eugene D. Savoye, and Robert K. Reich
Date issued: 14 December 1993
U.S. Patent no.: 5,270,558

Facing page, thinned, curved silicon wafer

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Rendering of the telescope courtesy of the TMT Observatory Corporation.

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