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DABS Timing: Clocks, Synchronization and Restart

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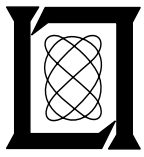

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16. Abstract

The DABS sensor timing subsystem, which consists of two clocks driven from a common station standard, is the subject of this paper. The subsystem configuration is described and the rationale for this design briefly given. Emphasis is on the techniques for synchronization to an external standard, coordination with other sensors and system restart after a failure or deliberate shut-down.

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1. INTRODUCTION

The DABS sensor makes use of two internal clocks. Each clock is a counter driven by a pulse train at an appropriate frequency, and the two frequencies are derived from a common station standard. One clock is arranged to register multiples and binary submultiples of one second, and it is called the "time-of-day" (TOD) clock. The other, referred to as the "real-time" (RT) clock, or "station time" clock, registers multiples and binary submultiples of one microsecond. The one-second-oriented TOD clock is convenient for synchronization with an external time standard and for the coordination of a group of sensors. The one-microsecond-oriented RT clock is convenient for timing events on the RF channel in units commensurate with the DABS waveform structure.

The TOD clock is used for the tagging of replies with their actual arrival time and for the reporting of antenna North passages, besides the synchronization and coordination tasks mentioned above. The RT clock is used in connection with interrogation and reply control commands and in the determination of target range. These uses of the RT clock are described in detail in Reference 1.

The need to coordinate sensors, which arises from the synchro-DABS feature of DABS, is responsible for the external synchronization and restart capabilities of the sensor. Sensor coordination takes two forms; one weak and one strong. The weak coordination applies to all DABS sensors in the entire network, and results from the requirement that the EPOCH field contents of a synchronized interrogation received by an aircraft at a given

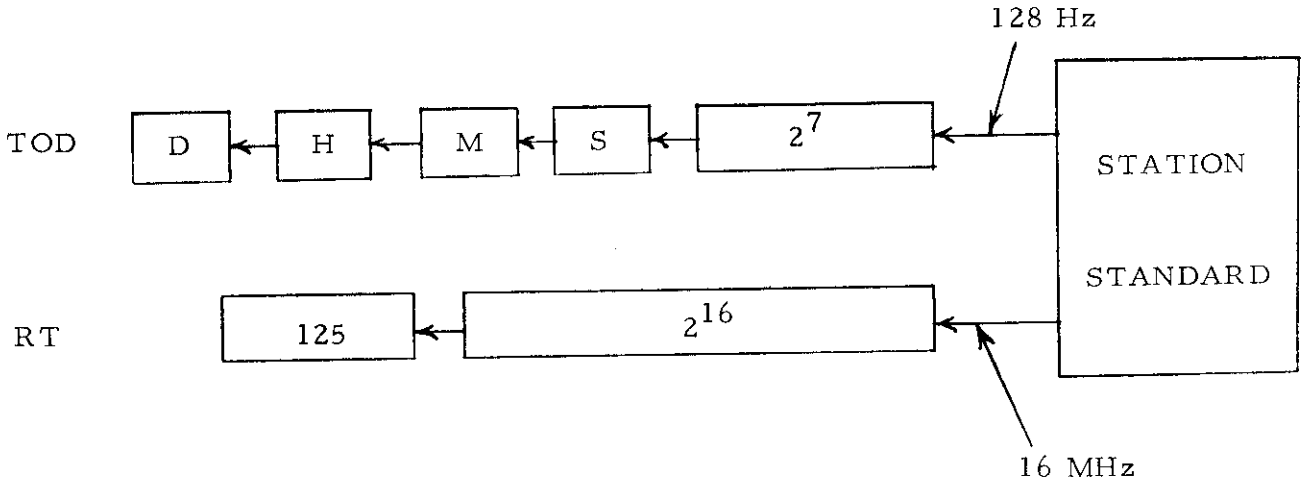
time must be independent of the sensor which originates the interrogation. The EPOCH field is derived from a portion of the RT clock, hence, this portion of all RT clocks must read alike at a given instant of time, to within a tolerance small compared to the least significant bit (the so-called "subepoch") of the EPOCH field.

Strong coordination is an optional feature which may apply only to a group of sensors participating in the coverage of a metroplex area, where the target density is often very high. If the strong coordination feature is employed the sensors must coordinate their ATCRBS and DABS activities, following a strict "firing time" sequence for ATCRBS and time-sharing the RF channel for synchronized DABS interrogations. In this case the frames (which structure the sensor's time line) must be synchronized and kept in phase between sensors of the group. In either case, coordination is maintained by means of the synchronization to a common external standard. The complications associated with sensor coordination show up in the restart algorithms described in this report.

The basic DABS timing subsystem is described in Section 2 below. External synchronization is discussed in Section 3. The issues of system restart, maintaining weak coordination (Section 4) and frame synchronization in the case of strong sensor coordination (Section 5), are implied but not specified in the basic DABS design. The suggested algorithms in this paper are offered as examples, which may be found useful and which, in any case, help to define the problems involved.

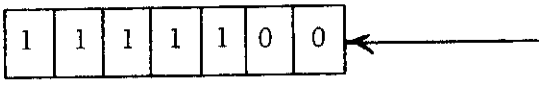
2. THE TIMING SUBSYSTEM

If we ignore, momentarily, the means of external synchronization, then the basic timing subsystem can be represented as a pair of special counters, as follows:

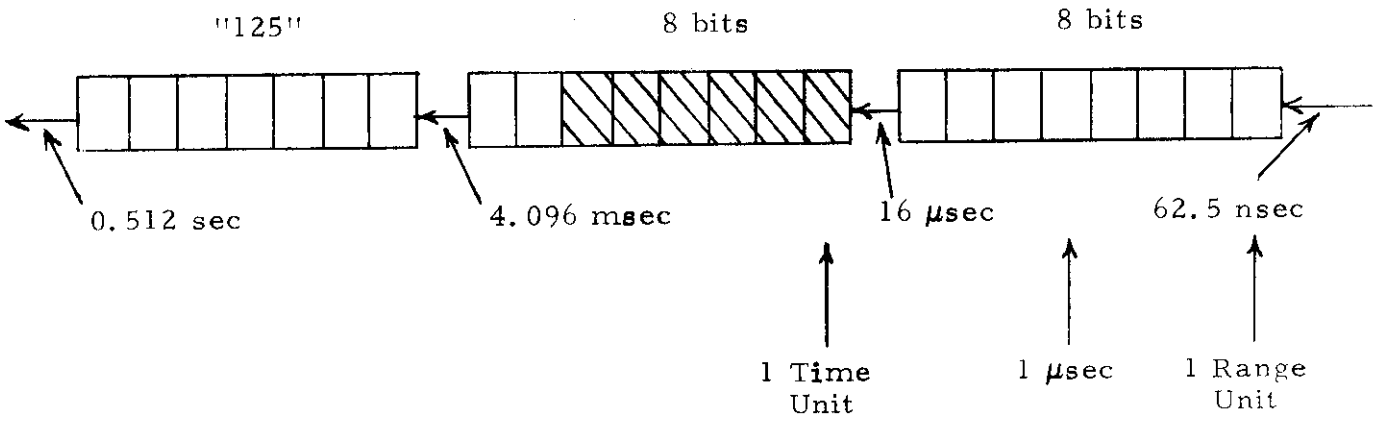


The TOD clock is driven at a rate of 128 Hz, and the low-order portion of the register is a seven-bit binary counter. This counter carries out every second, driving, in turn, a sequence of BCD counters which register seconds (S), minutes (M), hours (H), and days of the year (D).

The RT clock, driven at 16 MHz, consists of two counters in sequence. The fast counter is a 16-bit binary counter, which carries out every 4.096 msec, driving a special counter which resets to zero every 125 input counts. The "125" counter is implemented as a seven-bit binary counter, wired to clear on the next count when it registers 124:



The RT clock registers may be further broken up as follows, where all carry-in and carry-out periods are shown.

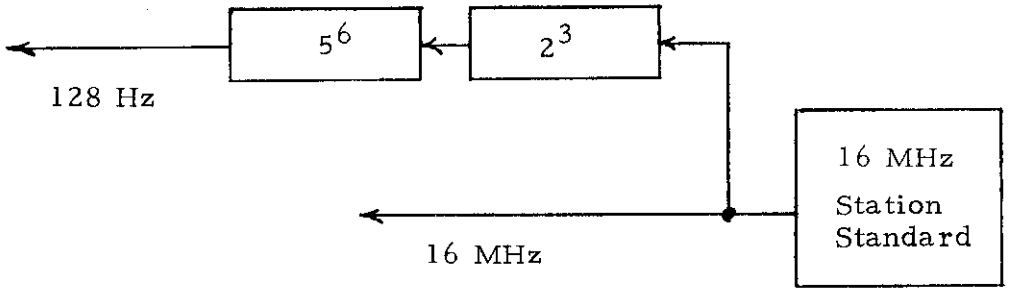


The 16-bit counter is shown here split into two eight-bit counters which correspond to the high and low order bytes of a word representing time in an interrogation or reply control command. These commands are sent from the channel management processor to the hardware (transmitter/modulation control unit and reply processors), and their contents are compared to the corresponding RT clock registers for the timing of interrogations and the enabling of reply preamble detection. When time information is transferred from the hardware to the channel management processor, only the 15 bits representing the contents of the "125" counter and the slower eight-bit counter are included. These features are fully discussed in Reference 1.

The least significant bit (LSB) of the RT clock register represents 62.5 nsec, which is called a "range unit." The LSB of the slower eight-bit counter represents 16 μsec, sometimes referred to as a "time unit." The synchro-DABS EPOCH field (six bits) is shown cross-hatched in the diagram, for

the nominal value of the synchro-DABS subepoch, 16 μsec. This quantity is a system parameter, NSUB, and the nominal value corresponds to 256 range units (Ru). Other permitted values are 128 Ru and 64 Ru (i.e., 8 μsec and 4 μsec), and their use would shift the EPOCH field to the right by one or two bits from the position shown here.

The driving signals for the two clocks must be obtained from a common frequency standard. The simplest arrangement is to count down a 16 MHz signal as follows:

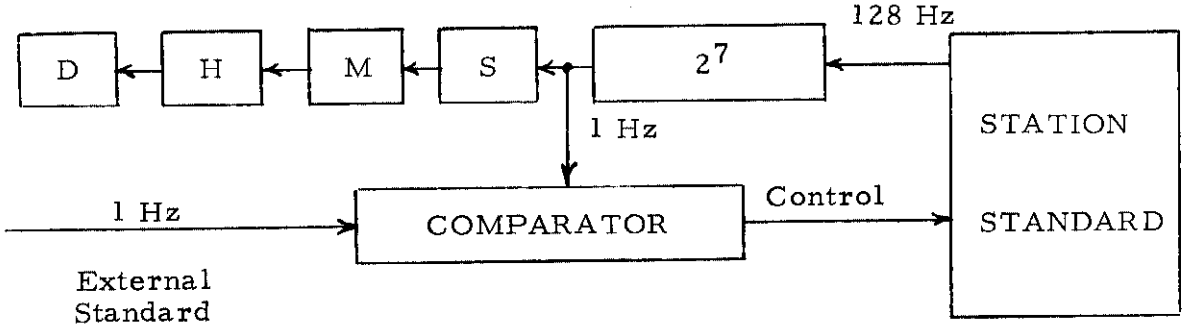


The "5^6" counter may be a sequence of six "5" counters or a sequence of two "125" counters, and the three-bit binary counter may coincide with the three lowest-order bits of the RT clock.

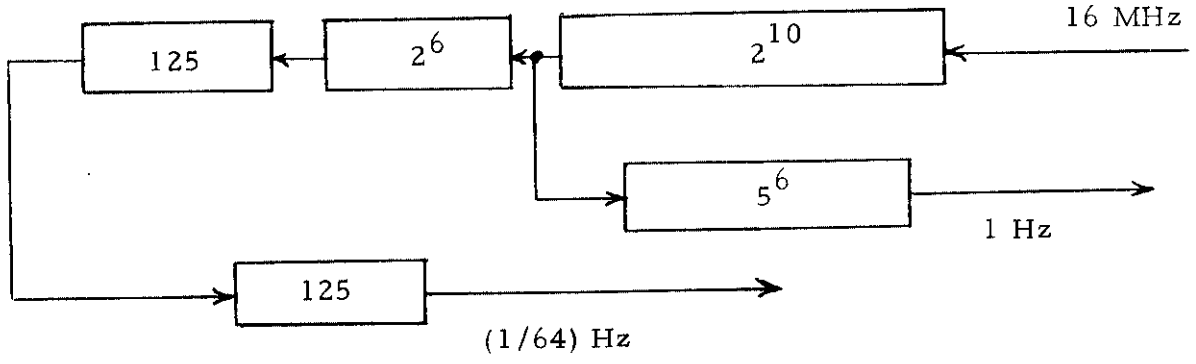
3. SYNCHRONIZATION WITH AN EXTERNAL STANDARD

The DABS sensor must be capable of receiving some external timing source from which a precise 1 Hz signal is derived. This externally-derived 1 Hz signal is constantly compared with a 1 Hz signal derived from the DABS timing subsystem to produce an error signal. The error signal is used to correct the station standard (master oscillator).

The internal 1 Hz may be taken from the TOD clock, so that the synchronization loop takes the following form:



Internal signals of 1 Hz and (1/64) Hz are also derived from the RT clock for performance monitoring purposes, as follows:



The 1 Hz output shown here is tested for coincidence with the TOD-derived 1 Hz signal, or the external standard, either of which is counted down by six bits to produce a comparison signal for the (1/64) Hz output.

4. TIMING SUBSYSTEM RESTART

Restart after a shutdown begins with the TOD clock. It is assumed that the externally-derived 1 Hz signal is reestablished and that both the TOD and RT clock registers are released from their driving signals. The RT clock register is always preset to read all zeros while the TOD registers are capable of being preset to any assigned values (only zero values of the seven bits representing binary fraction of one second need be used). With the station standard running and an approximate knowledge of current time of day, the TOD register is preset to a convenient future time, the least significant seven bits being set to zero. It must be possible to recognize the occurrence of that particular pulse in the externally-derived 1 Hz signal which corresponds to the preset reading of the TOD register, and also to cause the TOD clock to begin counting again upon the arrival of that pulse. The TOD clock will thus be restarted with the correct reading, although the 1-second carries into the "seconds" field will initially be a little late. This error will be automatically corrected by the external synchronization control loop, and some display should be provided to indicate when the internally-generated 1-Hz timing signal is within tolerance of the external standard.

In order to restart the RT clock, we must recognize the arrival of an externally-derived 1-second pulse which coincides with the clearing of the RT clock registers of all other sensors. Now one second is 16×10^6 Ru (range units), or $5^6 \times 2^{10}$ Ru. The RT clock period, P, is equal to 125×2^{16} Ru = $5^3 \times 2^{16}$ Ru. The largest common factor in these two numbers is $5^3 \times 2^{10}$, hence 64 seconds = 125 P. Thus every 125th clearing of the RT clock register

coincides with a carry into the seconds field of the TOD clock. These occasions will be called "start times."

Start times occur every 64 seconds, and on a minute change every 16 minutes. They occur on an hour change every four hours and hence can be made to recur at the same times every day. There are 1350 start times each day, and by choosing midnight as a start time, a convenient pattern results. We assume that this choice is made, so that the restart procedure can be carried out autonomously by a single sensor as soon as its TOD clock is running. Given the current TOD reading, a simple algorithm can determine the next convenient future start time, and it can be arranged to start the RT clock counting upon the arrival of the corresponding pulse.

5. FRAME SYNCHRONIZATION

When a set of sensors is strongly coordinated, they share a common frame duration. This frame duration is an integer, F, representing the actual frame length in time units. The recurring moments when new frames begin may be called "frame start times." As mentioned before, frame start times occur simultaneously at each sensor of a strongly coordinated group. If one of these sensors must restart, it is desirable for this sensor to be able to begin at the proper phase within a frame without reference to the activities of the other sensors. This is possible if frame start times occur at predictable times during the day, so that the sensor can determine how far into the frame it will be at restart time.

The most convenient scheme results when frame start times recur at the same times every day, in analogy to system start times. This will happen only if there are an integral number of frames in a day, which restricts the permissible frame durations. We assume this restriction is accepted, and that strong coordination is always implemented so that midnight is a frame start time. A sensor can then restart in the proper place within a frame, knowing only the frame duration, without communicating with other sensors.

The possible frame durations are found as follows: Since one time unit equals 16 μsec, there are $N = 24\text{x}60\text{x}60\text{x}10^6/16 = 5.4\text{x}10^9$ time units per day. If there are to be M frames per day, we must have

$$N = M \cdot F$$

Since

$$N = 5^8 \cdot 3^3 \cdot 2^9 ,$$

the possible values of F all have the form

$$F = 5^i \cdot 3^j \cdot 2^k ,$$

where

$$0 \le i \le 8$$

$$0 \le j \le 3$$

$$0 \le k \le 9$$

There are 360 values in all, ranging from one time unit to one day. Table 1 provides a list of all values between 125 and 3125 Tu, which corresponds to the range from 2.0 to 50.0 msec. The frame lengths are given both in time units and milliseconds.

The largest gaps in this list of permissible frame lengths occur at the values 160 and 320 Tu. In each case, the next available frame is longer by 12.5%. No other gaps representing increases larger than 8% occur. Since the matching of frame length to antenna dwell time is not a precise one, the restriction to frame lengths in the above table should not be serious.

Tu	msec	Tu	msec
125	2.000	750	12.000
128	2.048	768	12.288
135	2.160	800	12.800
144	2.304	864	13.824
150	2.400	900	14.400
160	2.560	960	15.360
180	2.880	1000	16.000
192	3.072	1080	17.280
200	3.200	1125	18.000
216	3.456	1152	18.432
225	3.600	1200	19.200
240	3.840	1250	20.000
250	4.000	1280	20.480
256	4.096	1350	21.600
270	4.320	1440	23.040
288	4.608	1500	24.000
300	4.800	1536	24.576
320	5.120	1600	25.600
360	5.760	1728	27.648
375	6.000	1800	28.800
384	6.144	1875	30.000
400	6.400	1920	30.720
432	6.912	2000	32.000
450	7.200	2160	34.560
480	7.680	2250	36.000
500	8.000	2304	36.864
512	8.192	2400	38.400
540	8.640	2500	40.000
576	9.216	2560	40.960
600	9.600	2700	43.200
625	10.000	2880	46.080
640	10.240	3000	48.000
675	10.800	3125	50.000
720	11.520		

Table 1. Frame Lengths

REFERENCE

1. E. J. Kelly, "DABS Channel Management," Project Report ATC-43, Lincoln Laboratory, M. I. T. (in preparation).