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The Aircraft Reply and Interference Environment Simulator (ARIES) Volume 3: Programmer's Manual

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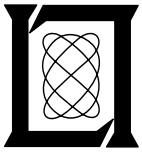

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16. Abstract

The Aircraft Reply and Interference Environment Simulator (ARIES) makes possible the performance assessment of a Discrete Address Beacon System (DABS) sensor under its specified maximum aircraft load. To do this ARIES operates upon a taped traffic model to generate simulated aircraft replies and fruit, feeding them to the sensor at RF. Support documentation for ARIES, of which this is the third volume, consists of:

Volume 1: Principles of Operation
Volume 2: Appendices to the Principles of Operation
Volume 3: Programmer's Manual

The ARIES Programmer's Manual describes the operation, signal formats and protocols of the Lincoln Laboratory-built input/output devices controlled by the Eclipse computer. The descriptions are primarily concerned with the logic of the interface boards that reside in the computer chassis and the formats of the words transferred to and from the computer. The logic of the devices themselves is described only to the extent necessary to understand the interface protocols and data formats.

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1.0 INTRODUCTION

1.1 Purpose

The Aircraft Reply and Interference Environment Simulator (ARIES) is a test system designed to simulate a high density radar beacon environment for the purpose of evaluating Discrete Address Beacon System (DABS) sensors. DABS is an improved surveillance and communication system designed to support the needs of the civil air traffic control system. For a more complete description of both the DABS system and ARIES, please see Volume 1 of this document. It is recommended that the overview sections of that volume be read before reading this manual, in order to give the correct context to the material presented here.

This manual describes Lincoln Laboratory-built input/output devices used in the ARIES system from the point of view of persons trying to control these devices from the computer. The descriptions are primarily concerned with the logic of the interface boards that reside in the computer chassis and the formats of the words transferred to and from the computer. The logic of the devices themselves is described only to the extent necessary to understand the interface protocols and data formats.

Devices not built by Lincoln Laboratory are described in separate manuals provided by their manufacturers (see the list of references).

Figure 1.1 shows the overall block diagram of the ARIES System, and all interfaces to the DABS sensor.

1.2 Data General I/O Interface Conventions

ARIES employs a Data General 'Eclipse' computer and associated I/O devices and interfaces. Data General interfaces have two modes of data transfer. One is programmed I/O, where the transfer of each word is controlled by the software. The other is data channel I/O, where the software merely specifies to the device the address and length of a buffer area in memory (via programmed I/O). All transfers to or from that buffer are controlled by the device interface, independently of the software.

Programmed I/O is conducted between a CPU register and one of three "registers" on the device interface, the A, B, and C registers. These may or may not be implemented as unique hardware registers. It is better to regard A, B, and C as device addresses of particular components of the interface, rather than as actual registers. Output to these registers occurs via the DOA, DOB, and DOC instructions, respectively. The corresponding input instructions are DIA, DIB, DIC.

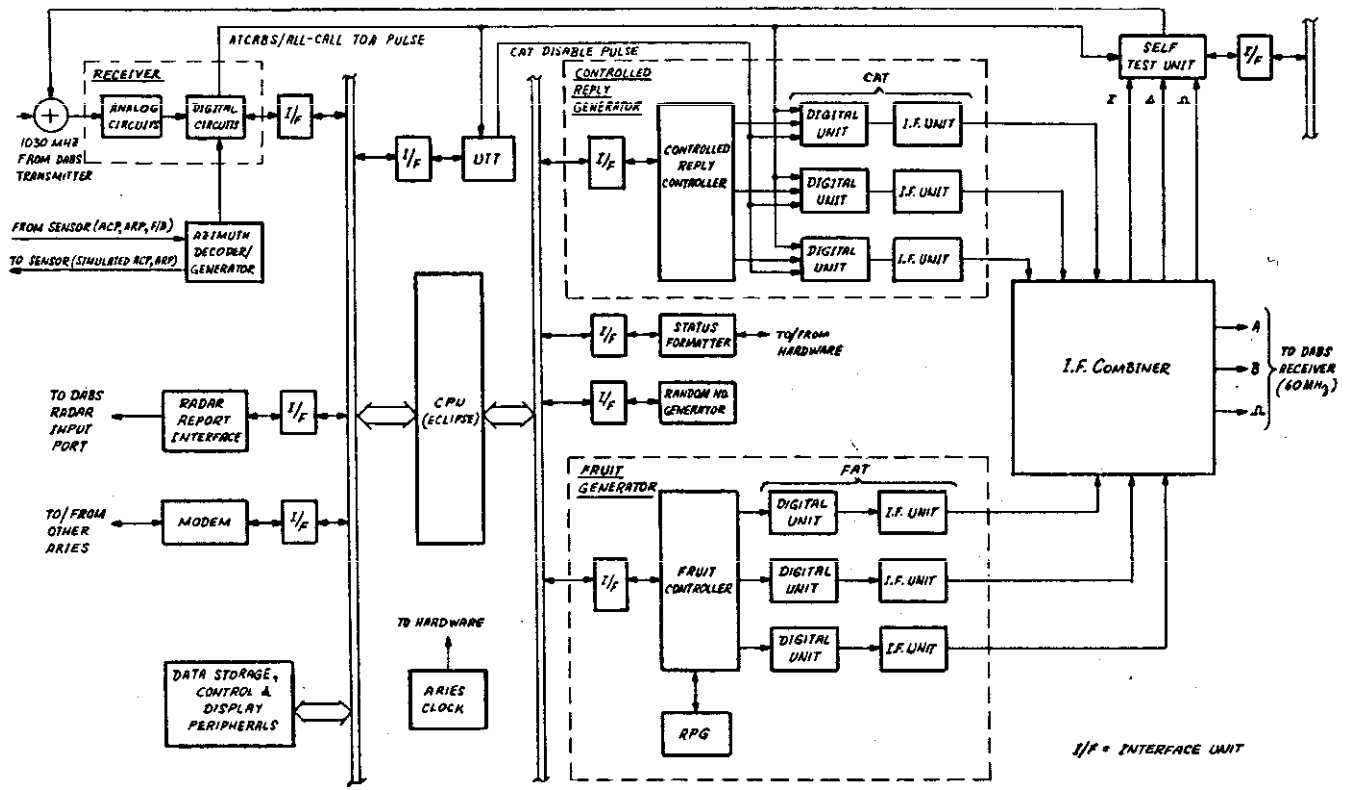


Fig.1.1. ARIES Block Diagram.

Each device interface has three status flip-flops which are controlled by the software, the BUSY, DONE, and INTERRUPT DISABLE flip-flops. If BUSY is set, the device is active. DONE is always zero in that circumstance. When the device completes its operation, it clears BUSY and sets DONE. This automatically causes an interrupt to be generated at the CPU, unless the INTERRUPT DISABLE flip-flop is set, in which case the interrupt will be inhibited until INTERRUPT DISABLE is cleared. If DONE is set when INTERRUPT DISABLE is zero, an interrupt will be generated immediately. A device is completely inactive when both BUSY and DONE are zero.

There are several signals available to control these status flip-flops. The START line, when pulsed, will set BUSY and clear DONE. This usually has the effect of activating the device. The CLEAR line, when pulsed, will set both of these to zero. The IORST line is similar to CLEAR, except that the INTERRUPT DISABLE flip-flop is also cleared.

To pulse the START and CLEAR lines the letters S and C respectively are appended to the programmed I/O instruction mnemonics (e.g., DOAS, DIBC), or to a NO I/O TRANSFER instruction (NIOS, NIOC). There is a third control line, called the P line, which is operated similarly by appending a P to the I/O commands. It has no standard usage, and is interpreted differently by each device.

The IORST line is pulsed by the I/O RESET instruction, or by toggling the RESET switch on the front panel. It is pulsed automatically by the CPU when power is first turned on. Note that the input and output instructions, and any START, CLEAR, or P pulse associated with them, affect only the addressed device, while an IORST affects all devices.

INTERRUPT DISABLE is normally set and cleared by a MASK OUT instruction. This instruction places the contents of a specified CPU register on the data lines, and then sends a special control pulse. Each device looks at only one of the 16 data bits, and loads the value of that bit into its INTERRUPT DISABLE flip-flop on receipt of the pulse.

For more information on the operation of the Data General I/O system, please see the Data General documentation in the references.

2.0 RECEIVER

The ARIES receiver consists of an analog section and a digital section. The analog section receives its input from the ARIES RF port of the DABS sensor at 1030 MHz and demodulates it, providing output levels compatible with digital logic. The digital section detects arriving interrogations, determines their mode, and in the case of discrete interrogations it assembles the data bits and removes the error detection encoding from the DABS address field. At each interrogation, an interrupt is generated to inform the computer of its arrival and a 10 word interrogation data block is created in a buffer area in the computer's memory. This block contains the time of arrival, the antenna boresight azimuth at arrival, the mode, and (for discrete interrogations only) the data bits. The format is shown in the Appendix.

The receiver uses a data channel interface to store interrogation blocks directly into the memory. Therefore, it can operate independently of the computer once an input buffer area is specified to it. A 640 word buffer is required, allowing 64 ten word interrogation blocks to be stored. The interface maintains a count of the number of interrogation blocks that have been completed. This can be read by the software to determine how many complete interrogation blocks are awaiting processing. The software can also decrement this counter once it has completely processed an interrogation.

The input buffer is treated as a circular buffer by the interface. As long as the interrogation counter does not overflow (as it will if there are 64 unprocessed interrogations) the interface will continue storing interrogation blocks. If it reaches the end of the buffer area, it will continue at the beginning of the buffer.

The interrupt generated with each interrogation occurs at the time of bracket detection for ATCRBS or ATCRBS/All-Call interrogations, and at the time of sync phase reversal detection for discrete interrogations. In the case of discrete interrogations an additional 14 to 28 μsec can elapse before the last word of the interrogation block is stored, depending on whether the interrogation is a surveillance or Comm-A interrogation respectively. Therefore, it should not be assumed that occurrance of an interrupt means that the data is available. The interrogation counter must be tested to determine if the data block is complete, as it will only be incremented upon storage of the 10th word of the block.

The interrupt logic for this interface is a modification of the Data General standard. Two DONE flip-flops are used to indicate different conditions. The standard DONE, which is tested by the I/O SKIP instruction, is set only upon interrogation counter overflow. As in the Data General standard, the BUSY flip-flop is simultaneously reset, disabling the interface. This occurrence should be treated as an error condition.

The second DONE flip-flop cannot be tested by the I/O SKIP, but does cause an interrupt to be generated. The BUSY flip-flop is not reset. This is used to indicate the arrival of an interrogation. When either of the DONE flip-flops is set, an interrupt is generated, and the INTA instruction will indicate that the interrupt is from the receiver. The I/O SKIP instruction can be used to distinguish the two cases by testing the standard DONE flip-flop.

The interface must be initialized by sending a CLEAR or IORST pulse to assure that BUSY and both DONE flip-flops are reset, and that the interrogation counter is zeroed. Then the address of the origin of the buffer area must be set via a DOA instruction. The buffer length is always assumed to be 640 words. Sending a START pulse will then activate the receiver.

Upon receipt of an interrupt from the receiver, the program must first check whether the interrupt indicates buffer overflow or the arrival of an interrogation. If the latter, it must first reset the second DONE flip-flop by means of the P pulse. Then it must repeatedly read the interrogation counter via a DIC instruction until a non-zero count is indicated. It can then process the interrogation.

In order to be able to locate the interrogation, the software must maintain a buffer pointer of its own. It is not correct to read the receiver's memory address register for this purpose. Every time BUSY is set, the interface's memory address register is set to the beginning of the buffer, and the first interrogation will appear there. Subsequent interrogations will appear in successive locations until the end of the buffer is reached (at the end of every 64th interrogation) at which time the address register will be set back to the beginning of the buffer.

When the program has completed processing the interrogation, it must decrement the interrogation counter via a DOC instruction. This DOC does not transmit any data, but merely provides a pulse to the interface which is used to decrement the count.

In processing interrogations, the programmer should note that the interrogation time field has different precision for DABS and ATCRBS/All-Call interrogations. The receiver has a 20 bit range counter that counts at a 16 MHz rate. The DABS interrogation time is used to calculate the precise reply time and therefore the low order 16 bits of this counter are used. This allows a maximum unambiguous round trip time of 4.096 msec. The ATCRBS/All-Call time is only used in obtaining the inter-interrogation times while ARIES is finding the interrogation pattern of the DABS sensor. Less precision and a longer unambiguous interval is required, and so the high order 16 bits of the 20 bit counter are returned as the ATCRBS/All-Call interrogation time.

Before exiting the interrogation interrupt routine, it is worth checking the interrogation count to determine if any more interrogations have arrived

during the processing interval. Processing these immediately will avoid the overhead of saving and restoring the machine state for each interrupt.

The current value of the receiver's memory address register can be read via a DIA instruction. This is useful primarily for diagnostic purposes, and points to the next location to be written into by the interface.

Note that, since the interrogation interrupts do not reset the BUSY flip-flop, the receiver will run continuously once started. It will be disabled only by an I/O RESET instruction (or a reset from the front panel), a CLEAR pulse, or a buffer overflow condition.

3.0 CONTROLLED REPLY GENERATOR

The Controlled Reply Generator (CRG) generates both DABS and ATCRBS replies under software control. All non-fruit replies are generated by this portion of ARIES. As shown in Fig. 3.1 the CRG consists of several components. The program creates reply data and transmits it to buffers in the interface. The microprocessor controller polls the Controlled ARIES Targets (CATs) to see if any are ready for new reply data. When new data can be accepted by a CAT, the controller obtains the next set of reply data from the interface buffers, if any is available, and places it into the CAT.

All programming for the CRG involves only the interface circuits, and the rest of this discussion focuses exclusively on the operation of the interface. The interface serves a dual purpose. First, it forms a link between the computer and the controller. Second, it provides a buffer space where the program can place replies as they are generated. The advantage of having replies stored in the interface rather than in the computer's memory is that the data transfer rate to the controller is increased. This makes it possible to handle bursts of replies that would not be transferred in time if the Data General direct memory access channel was used to obtain the data from the computer's memory. It also reduces the amount of interference between central processor and I/O memory access requests.

Two buffer memories are built into the interface. At any time, one is labeled as primary and the other as secondary, but the roles can be reversed under program control. Each buffer is 1024 words long (16 bit words). This allows the storage of 102 DABS discrete or all-call replies (10 words each) or 256 ATCRBS replies (4 words each). The microprocessor controller can read reply data only from the buffer designated as primary.

To understand the functioning of the primary and secondary buffers, it is necessary to understand how ARIES handles discrete and ATCRBS/All-Call interrogations. Discrete interrogations are handled as they are received. The ARIES receiver interrupts the computer, which then processes the interrogation data and generates a reply, which is immediately sent to the CRG. This can be done because the DABS transponder turn-around time of 128 μsec allows sufficient processing time.

In the case of ATCRBS interrogations, however, the specified turn-around time is 3 μsec. This does not allow sufficient time for the software to process these interrogations "in real time". Fortunately, the time and mode of ATCRBS/All-Call interrogations is predictable, as the sensor follows a fixed interrogation pattern. Therefore, the ARIES system can prepare the complete set of ATCRBS and all-call replies for a given interrogation in advance of that interrogation actually being sent. When the interrogation is received, these pre-computed replies are transmitted and ARIES begins generating the replies for the next ATCRBS/All-Call interrogation.

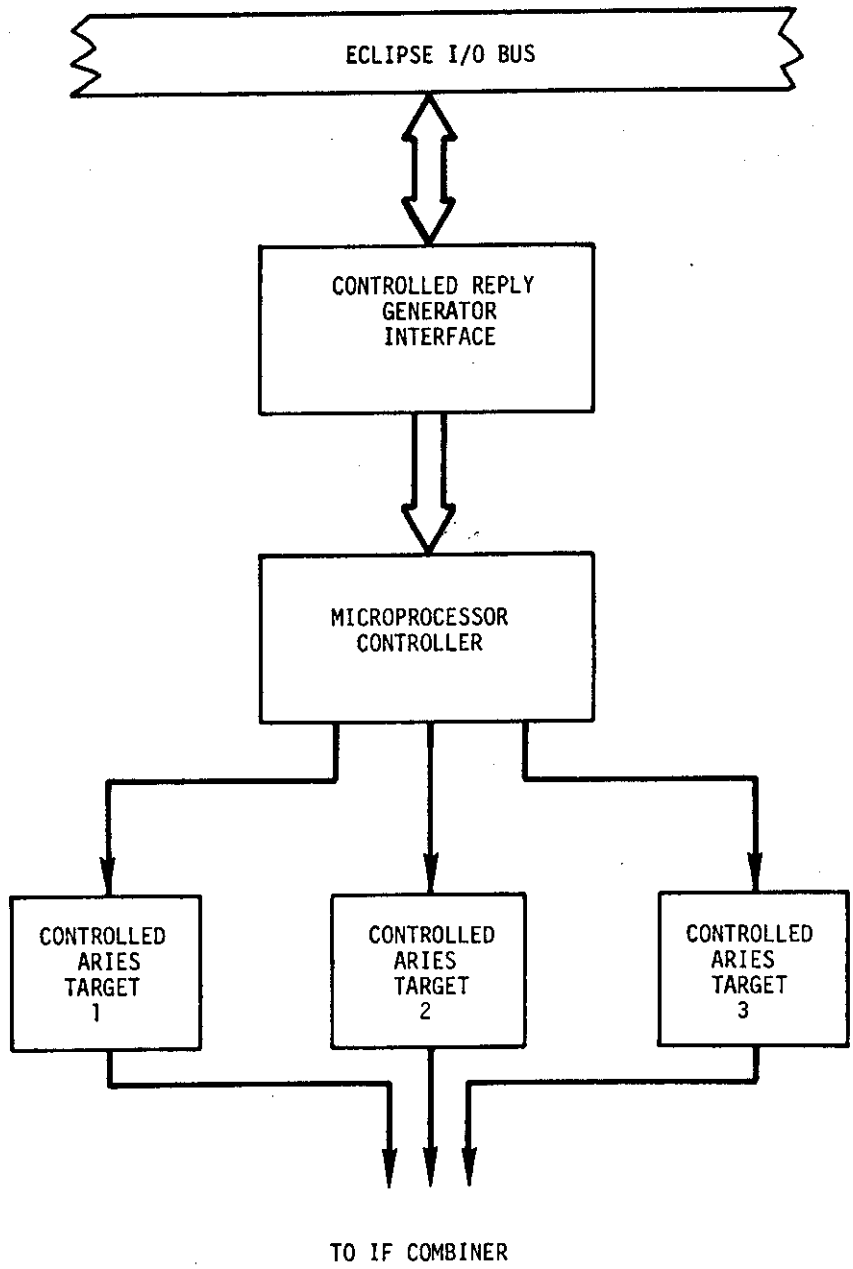


Fig.3.1. Controlled Reply Generator Components.

The secondary buffer is the storage area for these pre-computed ATCRBS and all-call replies. Since the controller can only read from the primary memory, these will not be transmitted. When the ATCRBS/All-Call interrogation is received, the software switches the buffer status. Since the ATCRBS and All-Call replies are then in the primary buffer the controller immediately begins sending them to the CATs.

DABS discrete replies are to be transmitted immediately, and so the CPU must store them directly into the primary buffer. This introduces the problem that this buffer may be simultaneously read from by the controller and written into by the CPU. Therefore, some control logic is needed so that it is always accurately known how many replies have yet to be read from the buffer. Each buffer therefore has associated with it a reply counter. This is incremented each time a complete reply is entered into the buffer by the software and decremented each time the controller reads a reply. Just as the controller can only look at the primary buffer, it can only access the primary reply counter. Figure 3.2 is a block diagram of the overall interface.

To write a word into the primary memory, the program executes a DOA instruction. Words must be written in the order shown in the Appendix, and are stored at successive locations in the buffer. Similarly, to store a word into the secondary memory, a DOB instruction is executed. To store the last word of a reply (word 4 for ATCRBS, word 10 for DABS All-Call or discrete replies) either a DOAP or DOBP instruction must be used, as this increments the reply counter for the buffer in addition to storing the last reply word. The result of issuing a pulse on the P line other than in conjunction with DOA or DOB is undefined.

The interface buffers are circular buffers. After word 1023 is written, word 0 will be the next to be written. Therefore, if more than 1024 words are written before any reading takes place, some locations will be overwritten. There is no hardware protection against this, nor any error indication. It is the responsibility of the software to keep track of the available memory. The size of the buffers is such, however, that they should never be more than 50% to 60% full.

It is acceptable to start a reply at the end of the buffer and finish it at the beginning, or in other words to split it between the end and beginning of the buffer.

The DOC instruction is used to control the interface operations. As shown in the Appendix, bits are provided to specify which buffer is primary, to select whether the primary or secondary reply counter is to be read by the next DIC instruction, to place the interface in a diagnostic mode, and to reset the microprocessor. The DIC instruction can be used to read back these control bits, as well as the primary or secondary reply counter, for test purposes.

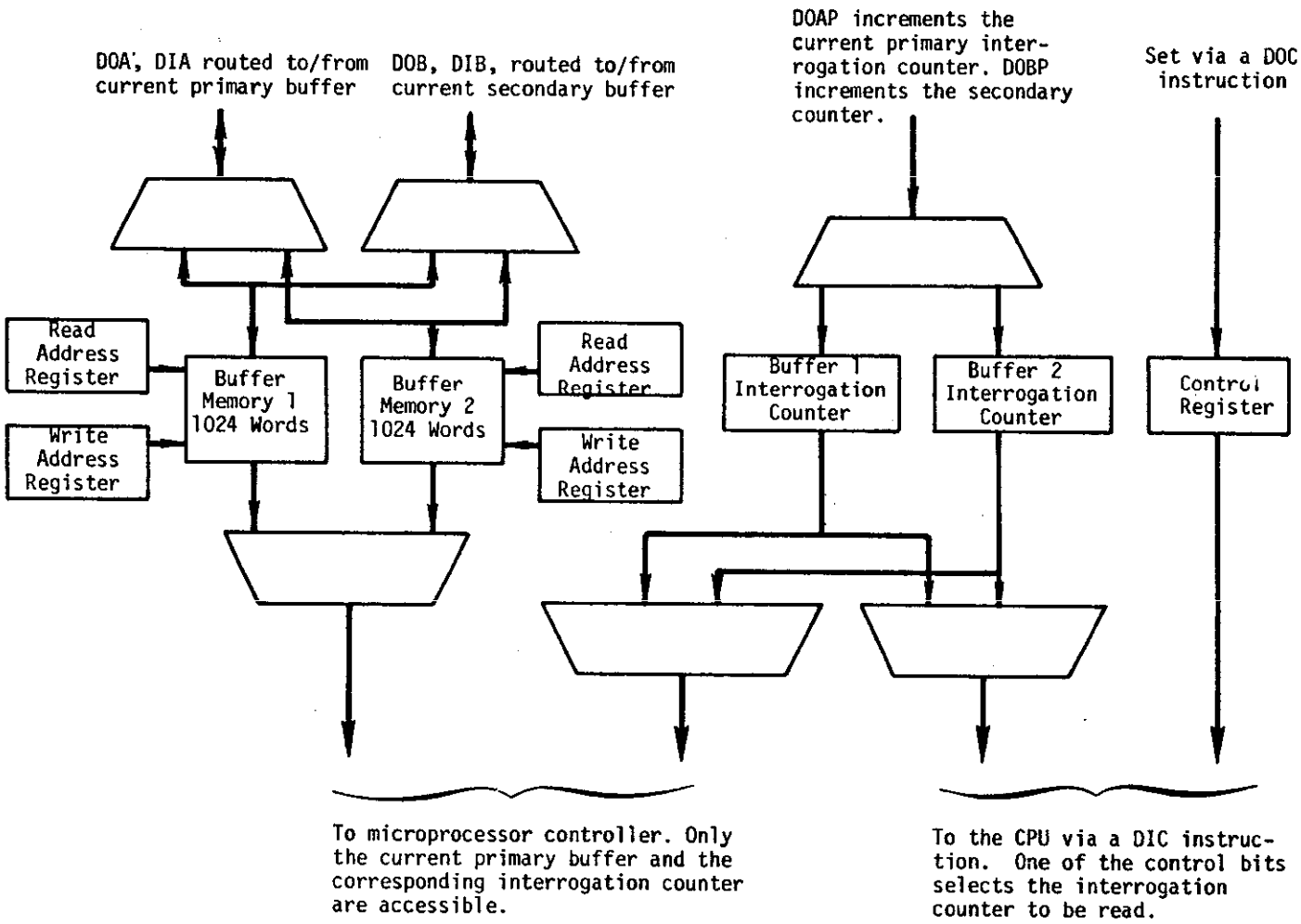


Fig.3.2. Block Diagram of the CRG Interface.

If the interface is placed in the diagnostic mode, the controller is inhibited from reading either buffer, and the program is allowed to read either buffer by means of DIA or DIB instructions for the primary and secondary buffer respectively. Successive DIAs or DIBs will read successive buffer locations, starting at whatever address the read address register was left indicating when diagnostic mode was entered. After location 1023, location 0 will be returned.

4.0 FRUIT REPLY GENERATOR

The Fruit Reply Generator (FRG) provides a means of inserting simulated fruit replies into the signal being sent to the sensor. These replies are randomly generated, with exponentially distributed inter-arrival times. The following parameters of the random reply generation process can be controlled by the programmer: average fruit rate, the fraction of replies in the main antenna beam (as opposed to being in the sidelobes), the fraction of replies that will have a fixed known value for their data bits (as opposed to having randomly generated data bits) and the specific fixed data bits to be used. Only ATCRBS replies are generated by the FRG.

The FRG consists of several components as shown in Fig. 4.1. The microprocessor controller is the central controlling element of the FRG. In normal operation, it polls the three Fruit ARIES Targets (FATs) to find one that can accept another reply block. At that point, it obtains the parameters for a fruit reply from the Random Process Generator (RPG), and sends it to the FAT.

The controller also periodically polls the interface to the computer. By this means it can obtain new fruit parameters from the computer and transmit them to the RPG. There are also diagnostic modes whereby the RPG reply parameters can be sent to the computer, or the reply parameters can be obtained from the computer rather than from the RPG.

Programming for the FRG is concerned primarily with the interaction between the program and the interface, and so the rest of this discussion focuses entirely on the interface.

Figure 4.2 is a diagram of the interface. There are two nearly independent channels, one for transferring data from the computer to the controller and the other for transfers in the opposite direction. Each such channel consists of a four word memory, a memory address register, and a bit to indicate whether the memory is in a read or write mode. In addition to the two data transfer channels, there is a two bit control register, which determines whether the FRG is in its normal operating mode or in one of three possible diagnostic modes.

All transfers over the two channels must be in groups of four words. The source of the data (i.e., the program or the controller) first must check the status bit to be sure that it is allowed to write into the memory. It then writes four words into the memory, causing the memory address register to wrap around and be left pointing at the first word stored. The status bit is then switched automatically by the interface, allowing the reader to access the data. When four words have been read, the status bit will switch back to its original state. A status bit value of 0 always means that the computer has access to the memory.

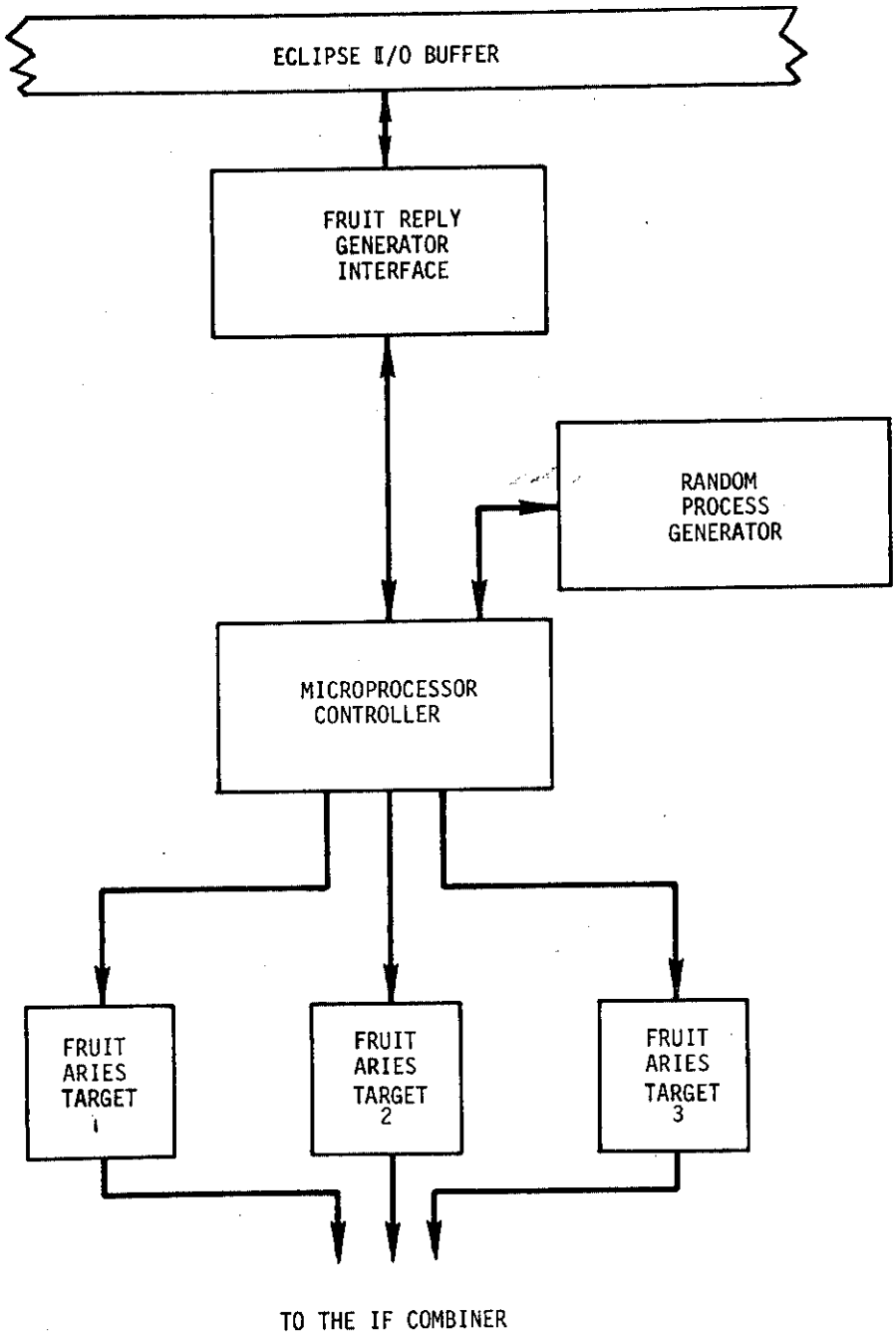


Fig.4.1. Fruit Reply Generator Components.

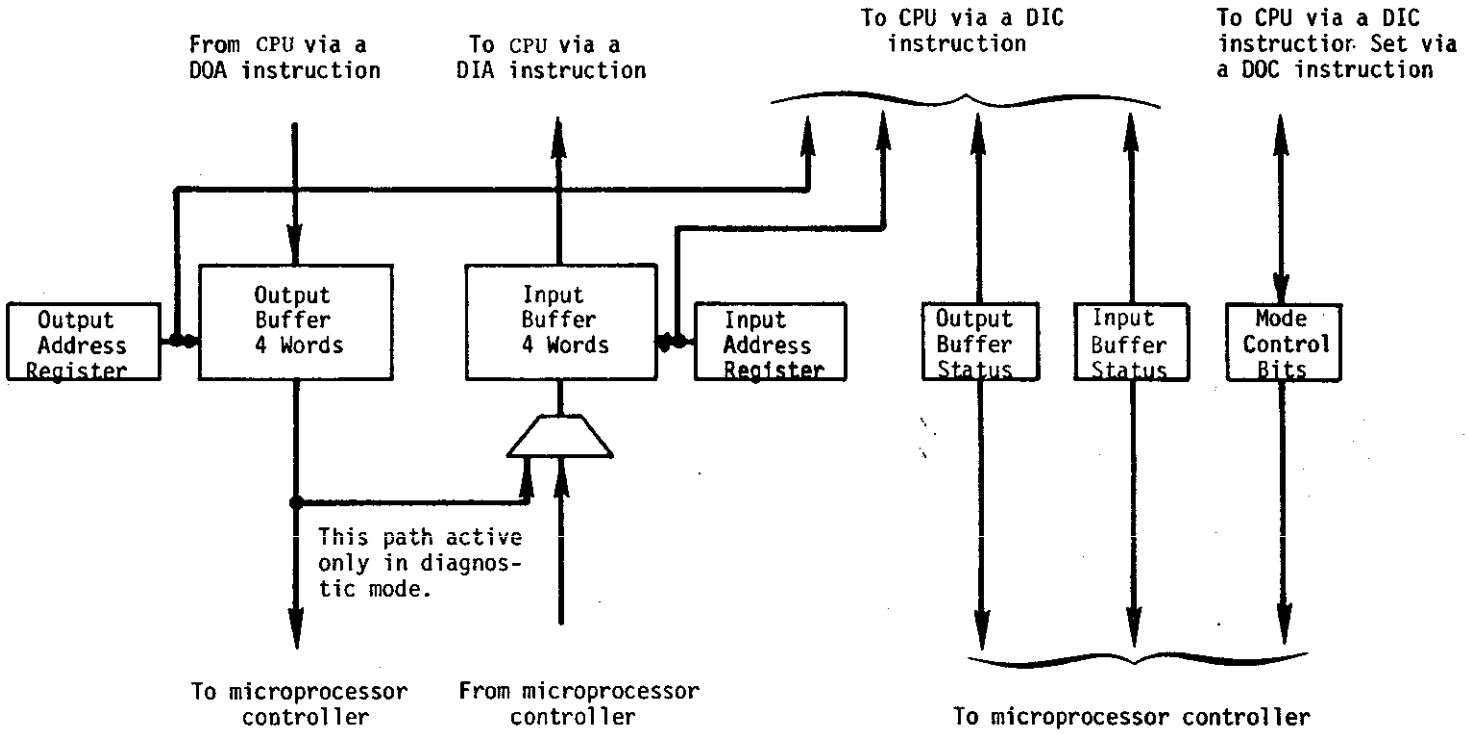


Fig.4.2. Block Diagram of Fruit Reply Generator Interface.

Note that both the input and output status bits will change state whenever the memory address for the corresponding buffer wraps around from the last word to the first. The value of the status bit does not interlock the memory to prevent either the microprocessor or the computer from accessing either buffer at any time. Therefore, for example, the program is perfectly free to output 8 successive words. This will cause the output status bit to change value twice, and leave it in its original state.

To send data to the microprocessor, the programmer follows the above protocol using the output channel. The status bits can be obtained by means of the DIC instruction. Data is transfered to the output memory by means of four DOA instructions. The format of the RPG control words and the order in which they are to be sent is shown in the Appendix. Similarly, four DIA instructions are used to read data from the input channel. The input data format is also shown in the Appendix.

Whenever the RPG parameters are changed (by sending 4 words to the controller over the output channel) the RPG is reset to its initial state.

Note that the DIC instruction also reads the current memory address register values for both channels. While only four words of memory are used in each channel, the memories are implemented using locations 4, 5, 6, and 7 of a 16 word memory. Four bits are provided to read the address register, although only the above four values should ever appear.

The mode control bits are set using a DOC instruction, as shown in the Appendix. Four modes are possible, as follows:

Control Bits	Mode
11	Normal
10	RPG diagnostic
01	FAT diagnostic
00	Interface loop test

The normal mode is the usual operational mode of the interface. Only the output channel is used. In running tests with a DABS sensor the ARIES software periodically (every sector of antenna rotation, or 11.25°) writes four words of RPG fruit parameters into the output memory. This data is then taken by the controller and loaded into the RPG. By this means the characteristics of the fruit replies generated by the RPG can be varied from sector to sector.

The RPG diagnostic mode provides a way of checking the RPG operation from the computer. Both the output and the input channels are used. To begin the operation, the program must initialize the RPG with some fruit parameters using the output channel. The controller will then request fruit reply data from the RPG and transfer it to the computer via the input channel. As each

reply is read by the program, a new one will be sent by the controller. This operation continues until enough data is gathered to check RPG operation. Since the random process generator is only pseudo-random, and therefore the sequence of values is repeatable, the received sequence can be compared against the expected sequence. The whole procedure may then be repeated for different fruit parameters to assure that the fruit characteristics change appropriately.

Normally the FATs receive fruit reply information from the RPG via the controller, and generate the appropriate analog reply signal at 60 MHz. To check the operation of the FATs one might consider looking at fruit replies with the ARIES Self Test Unit. However, there are problems with this in that (a) the reply parameters are random, making it difficult to determine if the results are correct and (b) even at low fruit rates replies will occasionally overlap and garble the results of the test.

To avoid these problems the FAT diagnostic mode of the FRG allows the software to insert known reply data into the FATs, bypassing the RPG. Only the output channel is used in this case. The data format is identical to the RPG diagnostic input data format, shown in the Appendix. The replies generated can then be observed using the Self Test Unit, without fear of garbled data.

All the above tests are meaningless if the interface itself is not working properly. To check this link between the computer and the microprocessor controller, the interface loop test mode is provided. This cascades the output memory and the input memory such that any data written into the output memory will be read from that memory and written into the input memory. A diagnostic program can verify the correct operation of both these memories by writing four words into the output channel, reading four words from the input channel, and verifying that they match.

The interface generates an interrupt only upon an error condition. If a FAT fails to request new data within 5 msec of the last time data was sent to it, it is considered to have failed and the controller will signal the interface to cause an interrupt. The BUSY bit must of course be set if this interrupt is to be seen.

5.0 SELF TEST UNIT

The purpose of the ARIES Self Test Unit (STU) is to allow for complete loop checks of most of the Lincoln Laboratory built equipment in ARIES, especially the analog equipment such as the receiver, the target generators, and the IF combiner. These tests can be conducted completely independently of the DABS sensor under test, and provide a means of verifying the correct operation of ARIES before any such test.

The STU is composed of two independent sections. The first of these is capable of generating a variety of interrogations at 1030 MHz which are entered into the receiver's input port. The typical mode of operation is for a program to specify a particular interrogation to be generated and to then look at the resulting input data block from the receiver and compare it against the expected result. This provides a complete loop check of the receiver, both the analog and digital portions.

The second section receives as inputs the Σ, Δ, and Ω signals from the IF combiner. One of these signals can be selected by the program as the signal to be sampled. When a reply is detected an amplitude sample is taken by an A/D converter and the data bits are also sampled. The program can then read the time of arrival, the amplitude, and the data bits. To perform a complete loop check of the reply generator circuitry, the diagnostic program must generate a series of replies. These should cover the entire range of amplitudes and off-boresight angles, all reply modes, and a variety of data content. The resulting signals are then sampled using the STU, and compared against the expected results.

The operation of both sections of the STU is controlled by two control registers. These can be altered under program control by executing two successive DOA instructions. Both words must be changed if either is to be changed. The STU will interpret every odd numbered DOA as a new transmission of control word 1. The control words remain in effect until two other words are sent. The format of these words is shown in the Appendix.

To generate a test interrogation, the program must specify an interrogation time and an interrogation type (one of up to 15 pre-stored interrogations, not all of which are currently implemented). Once the two control words containing this information have been transferred, the specified interrogation will be sent every time the STU clock equals the specified interrogation time. Since the STU clock is 16 bits wide, driven at 16 MHz, an interrogation will occur every 4.096 msec. If multiple interrogations are not desired, the program must disable the STU after receipt of the first interrogation by executing an NIOC instruction. The BUSY/DONE logic is not used for interrogation generation.

To listen to replies, the program must specify whether the Σ, Δ, or Ω channel is to be sampled, and whether the reply mode will be ATCRBS or DABS. Normally the interrogation generator should be turned off by zeroing the interrogation type field. Once the two control words have been transferred containing this information, a START pulse must be issued. At that point the STU begins looking for a reply. Next the program must cause a reply of the desired type to be generated via the Controlled Reply Generator or Fruit Reply Generator. When the STU has completely received this reply BUSY will be cleared, DONE will be set, and an interrupt generated.

At this point 11 words of information are available from the STU. The data includes the time of arrival, the amplitude, an indication of whether the reply was left or right of boresight (this is valid only when the Σ and Δ amplitudes are equal and near their maximum level), the data bits, an error bit which is set if the pulse position modulation (PPM) format of a DABS reply appears incorrect, and a copy of the STU control bits to verify that the appropriate data was sampled. The format of this data is shown in the Appendix.

To obtain this data the programmer executes successive DIA instructions. The words are returned in the order shown in the Appendix. It is not necessary to read all 11 words, or to read any of them. Issuing a START pulse will reset the STU and it will begin looking for another reply using the previous control words. Alternatively, the control words can be changed and a START pulse issued.

It is possible to set the STU up to simultaneously send an interrogation and listen for a reply. This could be useful in performing a complete check of the interrogation processing and reply generator portions of the system, including the real time software which receives the interrogation and generates the reply. Care must be exercised, however, to be sure that a START pulse is not sent in the middle of a reply, as this will result in a garbled input. The reply processing portion of the Self Test Unit does not check for preambles, or bracket pulses, but instead will start sampling reply data when triggered by the first pulse leading edge sensed after the START pulse is received.

It is also possible to listen to replies from the Fruit Reply Generator using the STU. This has diagnostic value in testing that the various IF signals are generated properly by that unit. However, the STU can only process one reply at a time, and overlapping fruit replies will give anomalous results. Therefore, the fruit generation must be controlled directly by the program, bypassing the hardware Random Process Generator (this is possible by means of one of the diagnostic modes of the Fruit Reply Generator).

It is sometimes useful in running tests to know approximately what value the ARIES range clock has. One way of controlling this is to send an ATCRBS

interrogation, which forces all the system range clocks to zero, including those of the receiver, Controlled Reply Generators, and the STU. Alternatively, sending a DABS interrogation will cause the receiver clock to be read and inserted into the interrogation data, providing the program with the current clock value.

6.0 RADAR REPORT INTERFACE

The purpose of this device is to generate radar target reports in Production Common Digitizer (PCD) format for serial transmission to the radar input port of the DABS sensor. It is a data channel device, and therefore can independently transmit an entire buffer of reports once initialized by the software.

To initialize the transmission, a DOA instruction is used to pass the address of the first word of the buffer and a DOB instruction is used to pass the two's complement of the word count. A START pulse will then begin the transmission. The DONE flip-flop will be set and an interrupt generated when the buffer transmission is completed. A DIA instruction can be used to read the current contents of the interface's memory address register.

Each word in the data buffer represents 12 bits of data, stored in bits 4-15. Bit 4 is transmitted first. Bit 0 controls whether even or odd parity will be generated by the interface for those bits (0 is odd, 1 is even parity). Including parity, 13 bits are serially transmitted to the sensor for each word taken from memory. Bits 1-3 of a memory word are ignored.

A surveillance report consists of 4 words, or 48 data bits, or 52 bits including parity. The format is shown in the Appendix. These words all must have odd parity. Reports, in turn, must be separated by at least one idle character. The data bits for this idle character are 000 111 111 111 with even parity. It is recommended that this idle character be considered the first or last word of each report, for a total of 5 words per report.

When no data is being transmitted, the interface continually sends idle characters over the serial link.

7.0 STATUS FORMATTER

This device is used to read various manual switch settings on the ARIES devices, and also receives error signals and status lines from several ARIES devices. In the normal mode of operation it sequentially polls devices for their current status. The new value of a device's status is compared against the old value. If they are not equal, polling is stopped at the end of the current polling cycle and an interrupt is generated to inform the computer.

There are two conditions under which an interrupt will not be generated. If the only bit that has changed is the low order bit of the 8 bits of status for some device, no interrupt will be generated. This bit is used only as a status indicator bit, never an error bit. The second condition which will inhibit interrupts is if the programmer has set the ERROR ENABLE bit (EE) in the status formatter control register to zero. This differs from simply masking the interrupt by means of the MSKO instruction in that if EE is zero polling will continue despite any mismatch.

There is also a mode in which the programmer can force the polling to stop at the end of the current cycle. This involves setting the UPDATE and ERROR ENABLE bits in the control register. When the polling cycle is complete, polling will stop and an interrupt will be generated.

The DOC instruction is used to set and clear the bits in the control register. This instruction can be executed at any time, independently of whether polling is in progress.

The DIC instruction is used to read various status lines in the interface, and is useful primarily for diagnostic purposes. The format and definition of these bits is given in the Appendix.

Whenever polling stops and an interrupt is generated, BUSY is zero and DONE is 1 as in the standard Data General I/O protocol. When the interface is in this condition, the 8 words of status information can be read by means of successive DIAs. It is incorrect to try to read words while polling is in progress (i.e., if BUSY is set). The first DIA retrieves word 1, the second word 2, etc. The programmer can read as many of the 8 words as are desired. There is no requirement to read them all or to read any. If reading continues beyond word 8, word 1 will be obtained on all subsequent DIAs.

Setting BUSY restarts the polling cycle, and resets the status formatter buffer address register so that the next DIA will retrieve word 1.

Note that because the status formatter compares successive status bytes to determine whether or not it should interrupt, interrupts may be generated when the status formatter is first activated or when one of the devices it

monitors is first turned on. Normally this is not desired, and the following sequence of commands will prevent interrupts until the status has stabilized.

```
DOCS          EE = 0, UPDATE = 0
Wait until the status has had time to stabilize
DOC           EE = 1, UPDATE = 0
```

Please see the Appendix for the format and definition of the status information.

The status formatter also has a self-diagnostic mode. By setting the Inhibit Polling bit (IP) in the control register by means of a DOC instruction, the status formatter is prevented from polling the devices. Instead it loads into the status words either all ones or all zeros. The choice is determined by the value of the Test Data (TD) bit, 0 giving zeros, and 1 giving ones. The status formatter memory and much of the data transmission circuits can be checked by reading this data back and checking that it matches the expected value.

8.0 UNIVERSAL INTERVAL TIMER

The Universal Interval Timer (UIT) provides a means to interrupt the computer at software controlled intervals. The UIT provides timing accurate to 1 μsec. Its timing is derived from the ARIES 16 MHz clock. The UIT counter counts from zero or a software specified preset value up to 65535. On the next count it wraps around to zero and an interrupt is generated by the carry out of the high order bit. Even though an interrupt is generated, the counter may continue running, depending on the contents of the control register.

Figure 8.1 shows the major UIT registers (with the exception of the control register) and their relationships. This is not a complete diagram of the UIT, and it intends to show the general data flow and not the exact electrical connections.

To provide an initial 16 bit count value for the UIT (called its preset value) a DOA instruction is used. This value is saved by the UIT in the preset register, allowing the counter to be repeatedly started at this value without requiring further DOAs.

The DOC instruction is used to set or reset the bits in the UIT control register. The current state of this register can be read by means of a DIC instruction. The bits in this register have the following functions when set (except where separate functions are shown for 0 and 1):

0-8: Unused
9: Load the counter on an external signal.
10: Load the counter on overflow.
11: Stop the counter on overflow.
12: Load (0) or read (1) the counter.
13: Load the counter.
14: Zero the counter.
15: Start (0) or stop (1) the counter.

} P line must also be pulsed for these to take effect.

All of these bits can be set or reset at any time, whether or not the counter is running. Bits 12-14 take effect whenever the P line is pulsed, whether or not the counter is running. To load the counter means to take the last preset value stored by a DOA instruction and load it into the counter. Overflow occurs when the counter wraps around from 65535 to zero, causing an interrupt. The external signal is an external electrical connection of the UIT. Pulses on that line can be used to trigger a load operation if bit 9 is set. In ARIES, this line is connected to the receiver and is pulsed whenever an ATCRBS/All-Call interrogation is received.

Bits 12 and 13 operate together to load the counter. By setting bit 12 to zero and bit 13 to 1, and pulsing the P line, the counter can be loaded with the preset value.

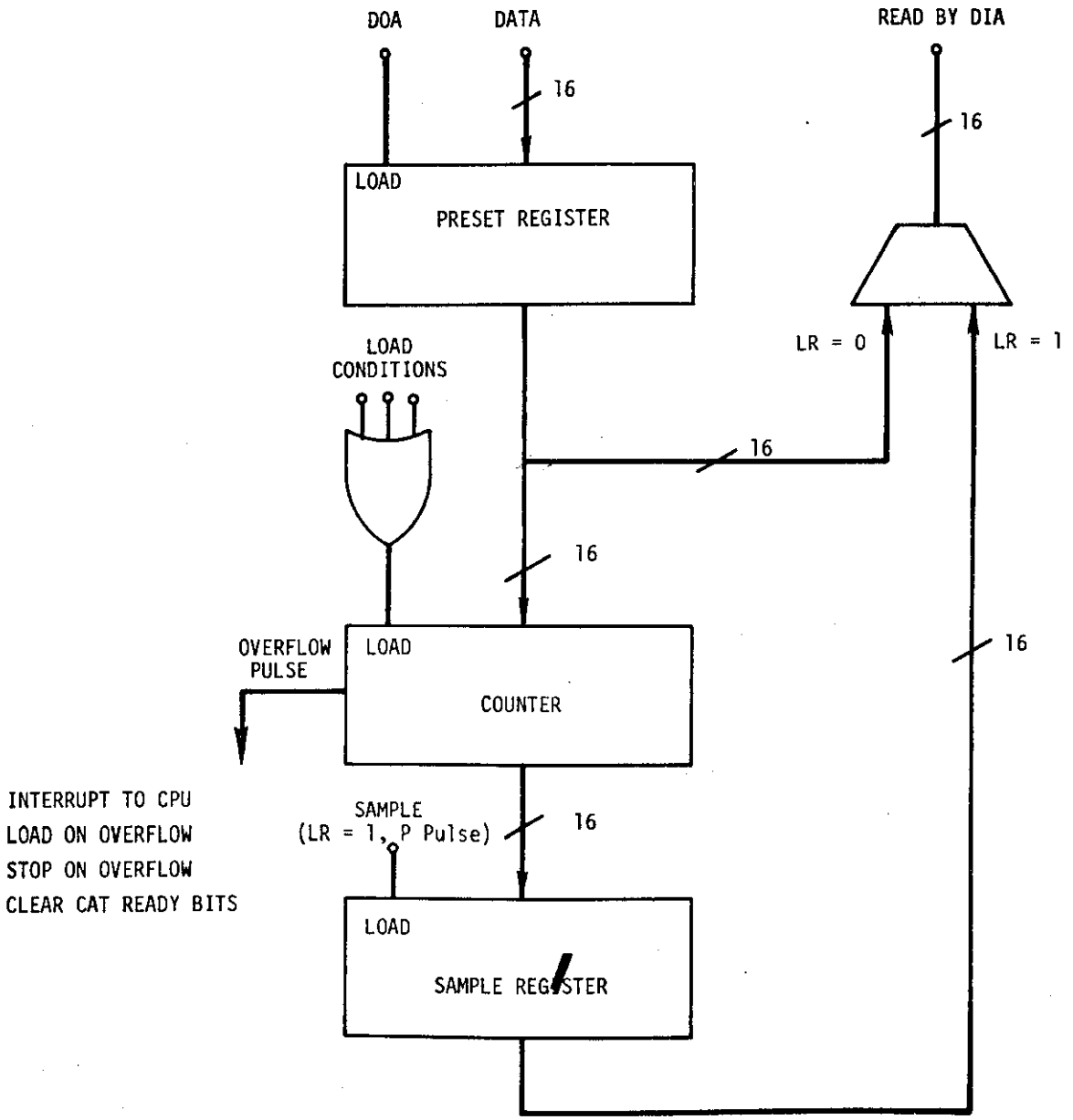


Fig.8.1. Major UIT Registers.

The current counter value can be read by setting bit 12 to 1, and pulsing the P line. This causes the current counter value to be sampled and saved in the sample register of the UIT. This action takes place regardless of the state of bit 13. This value can then be read by means of a DIA instruction. Bit 12 of the control register must remain set while this DIA is executed, or no valid data will be read. Whenever a DIA is executed with bit 12 set, the last counter value sampled will always be read. Reading the counter in this way does not stop it.

To generate an interrupt after a specific interval of T μsec, the programmer must preset the counter to 65536-T and start it running (if it is not already doing so). Since the Eclipse is a 16 bit machine using 2's complement arithmetic, this is equivalent to loading (- T). The BUSY bit must also be set in order to receive the interrupt, as the standard Data General BUSY/DONE logic is used for generating the interrupt. The BUSY bit has no effect on the operation of the counter itself.

To generate periodic interrupts at intervals of T μsec, the above procedure must be followed and in addition bit 10 of the control register must be set. Note that BUSY must be set again after each interrupt, or interrupts after the first one will be lost.

9.0 RANDOM NUMBER GENERATOR

The purpose of this device is to provide rapid generation of random numbers. It is extremely easy to use, successive DIA instructions returning successive 16 bit uniformly distributed random integers. The BUSY/DONE logic is not used, and no interrupts are generated.

Since the number generator is only pseudo-random, it can be made to repeat the same sequence of numbers by reinitializing it. This is accomplished by the I/O RESET pulse or by pulsing the P line.

References

1. M. Goon and D.A. Spencer, "The Aircraft Reply and Interference Environment Simulator (ARIES) Vol. 1: Principles of Operation", Project Report ATC-87, Volume 1, Lincoln Laboratory, M.I.T. (22 March 1979), FAA-RD-78-96.

2. D. Reiner and H.F. Vandevenne,"Provisional Message Formats for the DABS/ NAS Interface (Revision 1)", Project Report ATC-33, Revision 1, Lincoln Laboratory, M.I.T.(10 October 1974), DDC AD-A000257/6.

3. Programmer's Reference Manual, Eclipse Line Computers, Data General Corporation, 015-000024.

4. Programmer's Reference Manual, Peripherals, Data General Corporation, 015-000021.

5. Technical Reference, Programmable Synchronous Line Adapters, Data General Corporation, 014-000015.

6. Interface Designer's Reference, Nova and Eclipse Line Computers, Data General Corporation, 015-000031.

APPENDIX: DEVICE SUMMARIES AND DATA FORMATS

The following pages summarize the function of all the Lincoln Laboratory constructed I/O devices in the ARIES system. For a more complete description of device operation, please see the appropriate section in the main part of the manual, and also Ref. 1.

In the summaries, the functions START, CLEAR, P, and I/O RESET are represented by S, C, P, and IORST respectively. In describing the effect of pulsing these lines, those functions that are standard among all devices connected to the Eclipse I/O system have been omitted. These functions are as follows:

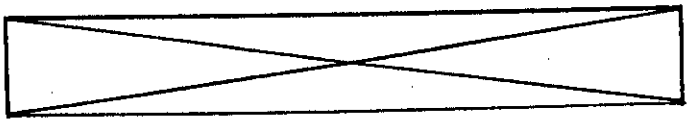
S: Sets BUSY, clears DONE, and clears any pending interrupt from the addressed device.

C: Clears BUSY, DONE, and any pending interrupt from the addressed device.

P: This line has no standard function.

IORST: Performs all the functions of CLEAR, and in addition clears the interrupt mask. This line affects all devices, and cannot be addressed to a particular device.

In the data format descriptions the following symbol is used to represent undefined, "don't care", fields:



Also, in several of the discussions, the term "set" is used in reference to flip-flops or bits to mean "set to 1", and "reset" to mean "set to 0".

In the descriptions of certain fields, additional information is included describing how the ARIES real time software uses these fields.

SUMMARY OF DEVICE NUMBER AND MASK BIT ASSIGNMENTS

Non-Lincoln Devices	Device Code (octal)	Mask Bit
TTY (Keyboard)	10	14
TTY (Printer)	11	15
Disk	33	7
Tape	22	10
Synchronous Line Adaptor	30	14
Line Printer	17	12
Real Time Clock	14	13
Lincoln Laboratory Devices		
Controlled Reply Generator	46	*
Fruit Reply Generator	50	2
Receiver	52	3
Universal Interval Timer	54	4
Status Formatter	56	5
Random Number Generator	60	*
Radar Report Interface	44	11
Self Test Unit	62	9

*These devices do not generate interrupts.

As is standard for all Data General and ARIES documentation, bit 0 is the high order bit, and bit 15 is the low order bit.

Device: Receiver
Device Number (octal): 52
Mask Bit: 3

S: Clears the second DONE flip-flop, and activates the receiver.

C: Clears the second DONE flip-flop, deactivates the receiver, and clears the interrogation counter.

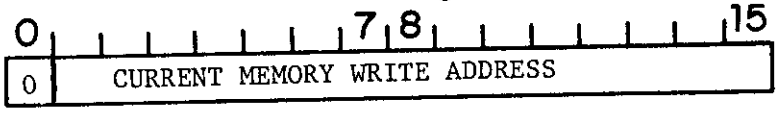
P: Clears the second DONE flip-flop, thereby clearing the interrogation interrupt.

IORST: The second DONE flip-flop is cleared and the interrogation counter is cleared. This signal has no effect on the buffer address pointer, or on the memory address register. These must be explicitly initialized by a DOA instruction.

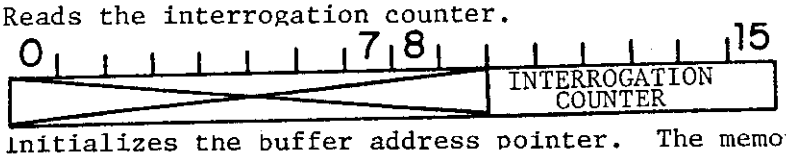
Note: The interrogation counter is zeroed whenever BUSY=0.

The second DONE flip-flop is set whenever an interrogation is received, causing an interrupt. The primary DONE flip-flop is set to indicate buffer overflow. The interrupts caused by these can be distinguished by using the I/O SKIP instruction to test the primary DONE flip-flop. (I/O skip will not skip if only the second DONE flip-flop is set).

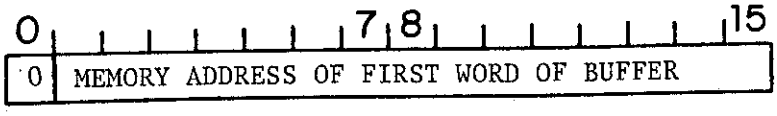
DIA: Reads the memory address register.



DIC: Reads the interrogation counter.

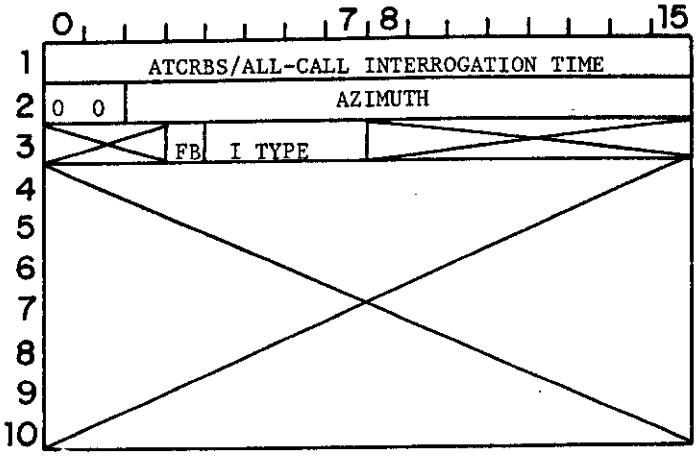


DOA: Initializes the buffer address pointer. The memory address register is also initialized to equal the buffer address pointer.

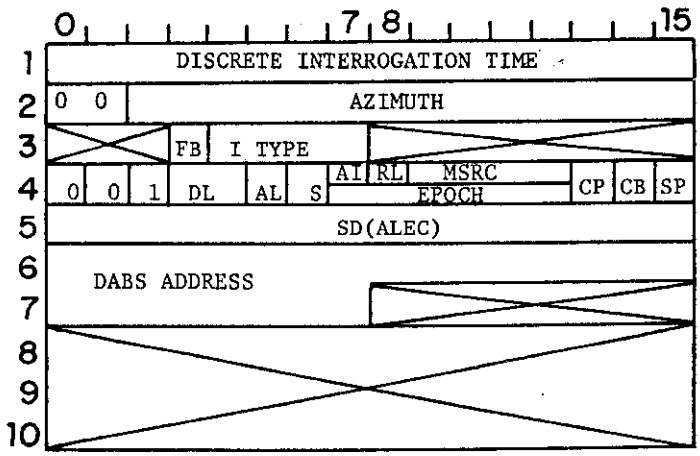


DOC: Decrements the interrogation counter. No data is transferred, and so the content of the register specified as the argument of the DOC does not matter.

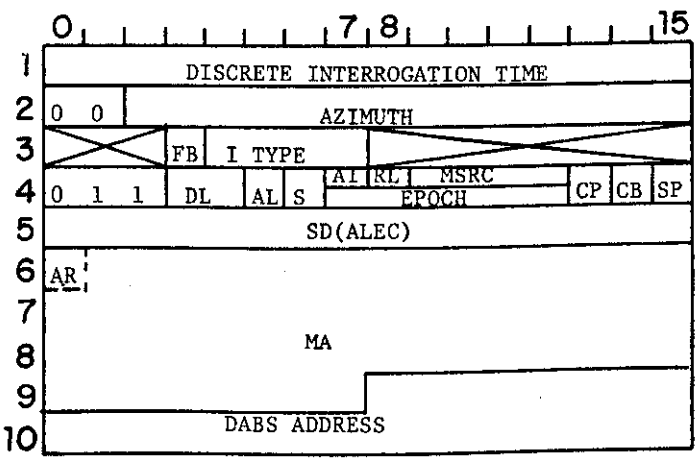
RECEIVER



ATCRBS/ALL-CALL
INTERROGATION



SURVEILLANCE
INTERROGATION (56 BITS)



COMM-A
INTERROGATION (112 BITS)

DEFINITION OF FIELDS

Field	Significance
ATCRBS/ALL-CALL INTERROGATION TIME	The time since the last ATCRBS/DABS All-Call interrogation; LSB = 1 μsec. Only used to measure the interrogation interval and therefore does not need range-clock resolution.
DISCRETE INTERROGATION TIME	The time since the last ATCRBS/DABS All-Call interrogation modulo 4.096 msec; LSB = 1/16 μsec. Used to calculate discrete reply times; therefore, range-clock resolution is required.
FB	Front/back bit. Indicates which antenna, front or back, transmitted the interrogation. 0 Front Antenna 1 Back Antenna
ITYPE	Interrogation type. Decimal Value — Significance 0 — Used to indicate an illegal uplink type. 1 — ATCRBS/DABS All-Call, Mode A. 2 — ATCRBS/DABS All-Call, Mode C. 3 — DABS-only All-Call. 4 — DABS surveillance (56 bits). 5 — ATCRBS Mode A (no P_4 pulse). 6 — ATCRBS Mode C (no P_4 pulse). 7 — ATCRBS Mode D (no P_4 pulse). 8 — DABS COMM-A (112 bits). 9-15 — Undefined.
AZIMUTH	LSB = $2\pi/2^{14}$ radian; measured clockwise from true north.

Note: The following fields are included in a DABS discrete interrogation. A detailed description of these fields and their use by ARIES appears in Ref. 1.

DL	DABS lockout. 00 Clear all DABS lockouts. 01 Lockout Mode A and Mode C All-Calls. 10 Lockout auxilliary interrogations (ignored by ARIES). 11 Lockout auxilliary interrogations and standard All-Calls (treated like 01 by ARIES).

DEFINITION OF FIELDS (continued)

Field	Significance
AL	ATCRBS lockout. Ignored by ARIES.
S	Synchronization indicator (synchro-DABS). 0 Unsynchronized interrogation. AI, RL, MSRC appear in the following bits. 1 Synchronized interrogation. EPOCH appears in the following bits.
AI	Altitude/identity bit. 0 Reply with Mode C altitude. 1 Reply with Mode A code.
RL	Reply length requested. 0 Surveillance reply (56 bits). 1 COMM-B reply (112 bits).
MSRC	Air-to-ground data link message source. Ignored by ARIES.
EPOCH	Synchro-DABS epoch. Merely copied into corresponding reply field.
CP	Clear PBUT. If set to 1, clears the transponder's pilot acknowledgment.
CB	Clear B bit. If set to 1, clears the transponder's downlink request.
SP	Spare bit, ignored by ARIES.
SD (ALEC)	Special data, or altitude echo field. Ignored by ARIES.
MA	COMM-A message field. Ignored by ARIES except for the bit marked AR, which initiates the acknowledgment request protocol if set to 1.
DABS ADDRESS	A 24-bit transponder identifier. The low order 10 bits are used by ARIES as a track number.

Device: Controlled Reply Generator
Device Number (octal): 46
Mask Bit: None (this device does not generate interrupts).

S,C: Not used. The BUSY/DONE logic is not used by this interface.

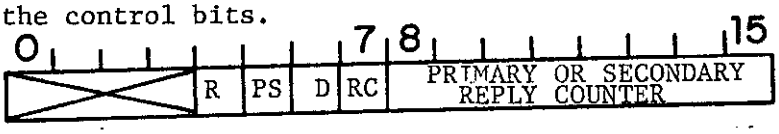
P: Used in conjunction with the DOA or DOB instruction which transfers the last word of a reply (word 4 for ATCRBS, 10 for DABS). This increments the reply counter for the current primary or secondary memory, depending on whether it is associated with DOA or DOB respectively. The result is undefined if P is used other than with a DOA or DOB instruction.

IORST: Zeros the read and write address register for both buffer memories, and zeroes both reply counters. The microprocessor controller reinitializes itself and all the target generators.

DIA: Reads one 16 bit word from the current primary buffer memory. The word is read from the location addressed by the current value of the read address register for that memory, and the read address register is incremented by 1. If its value is currently 1023, its incremented value will be 0. This can only be used if the interface is in diagnostic mode.

DIB: Identical to DIA, except that the word is read from the current secondary buffer.

DIC: Reads the current interface status, as shown. Only one of the two reply counters is read, the selection being based on the value of one of the control bits.



R: Setting this bit via a DOC causes the microprocessor controller to reset all the CAT's. This is useful in cases where the CAT's "lock up" for some reason, and stop processing replies. This bit is set to 0 by the microprocessor when the reset is complete. The CPU can check this via a DIC.

PS: Primary/secondary select. Selects which of the two buffer memories is to be the current primary buffer and which is to be the secondary buffer.

D: Diagnostic mode control.

0: Normal mode. DIA, DIB do not read buffer data.
1: Diagnostic mode. DIA and DIB can be used to read buffer data.

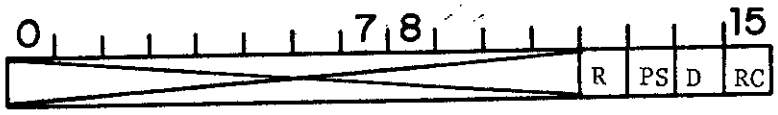
RC: Primary/secondary reply counter select. This bit determines which of the two reply counters will be read by a DIC instruction.

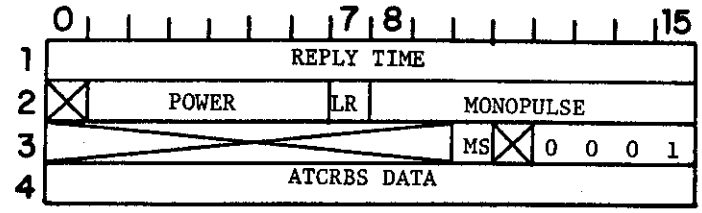
0: Primary buffer reply counter.
1: Secondary buffer reply counter.

DOA: Writes one word of data to the current primary buffer memory. The word will be stored at the location indicated by the current value of the write address register for that memory, and the register will then be incremented by 1. If the current write address is 1023, the incremented value will be 0. The formats of the various reply types are shown below.

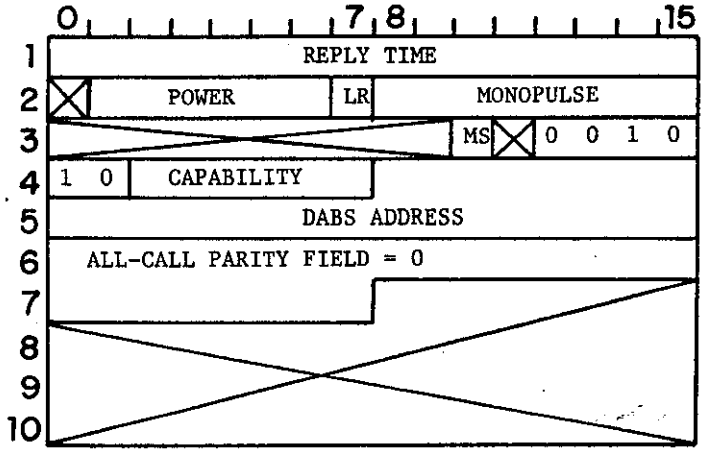
DOB: Identical to DOA, except that the word is stored in the current secondary buffer memory.

DOC: Transmits the control bits to the interface. See the data format for the DIC instruction for the bit definitions.

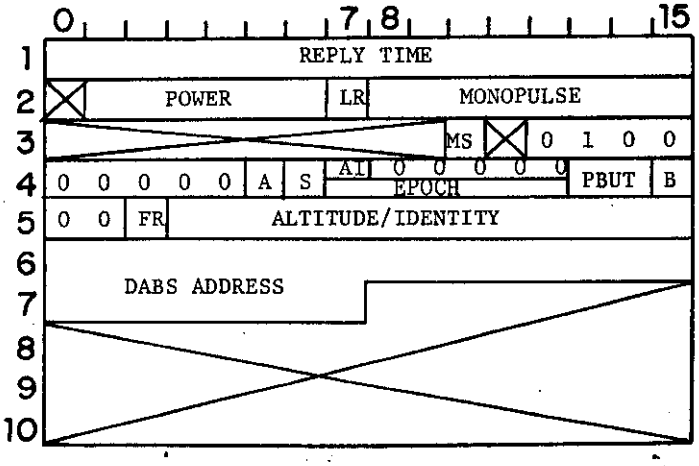




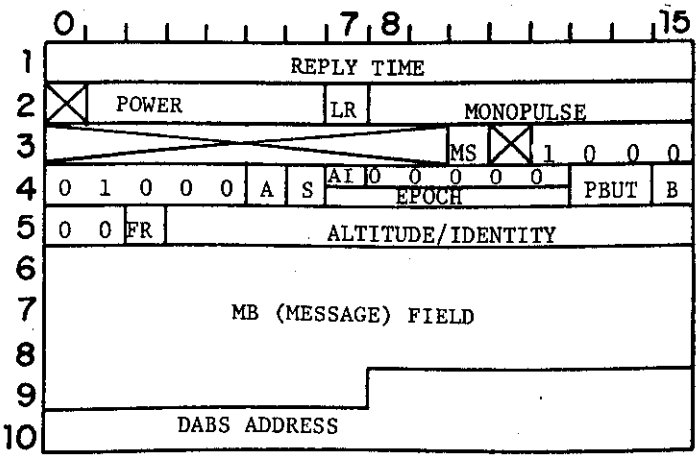
ATCRBS REPLY



ALL-CALL REPLY (56 BITS)



SURVEILLANCE REPLY (56 BITS)



COMM-B REPLY (112 BITS)

DEFINITION OF FIELDS:

Field	Significance
REPLY TIME	The time that the reply is to be generated; LSB = 1/16 μsec. Referenced to the time of the last ATCRBS/DABS All-Call interrogation (i.e., the reply time counter is set to zero at that time).
POWER	Reply power level; LSB increment = 1 dB. 0 -20 dBm 63 -83 dBm referred to the sensor's RF port (i.e., the reply will appear to the sensor as if it had these levels)
MONOPULSE	The off-boresight angle of the reply. Values (and therefore units) are determined by the calibration procedure. This value is calculated by table lookup based on off-boresight angle. The table is derived during the calibration procedure. In terms of amplitude, each step represents a .125 dB attenuation of Δ relative to Σ. A value of 0 gives $\Delta=\Sigma$.
MS	Mainbeam/Sidelobe. Determines whether the reply will appear in the mainbeam (MS=0) or in the sidelobe (MS=1). Normally, this value will be zero. A sidelobe reply is attenuated by an additional amount specified on front panel switches.
LR	Monopulse sign. Determines whether the monopulse angle is to be measured to the left (LR=0) or to the right (LR=1) of boresight.
ATCRBS DATA	The 13 data bits of a standard ATCRBS reply, plus F_1, F_2 (always 1) and SPI. The ordering is: $1\ C_1A_1C_2A_2C_4A_4OB_1D_1B_2D_2B_4D_4\ 1\ SPI$ where the standard ATCRBS pulse nomenclature is used.

DEFINITION OF FIELDS (continued)

The following fields are included in a DABS reply. A detailed description of these fields and their use by ARIES appears in Ref. 1.

Fields	Significance
CAPABILITY	Bits indicating the on-board devices with which the transponder is equipped. In ARIES, this information is obtained from the traffic model file.
DABS ADDRESS	A 24-bit transponder identifier. The low order 10 bits are used by ARIES as a track number.
ALL-CALL PARITY FIELD	Must always be 0.
A	Pilot alert bit. If set to 1, it indicates an on-board emergency condition whose nature is indicated by the value of the Mode A code. Set from the model file.
S	Synchronization indicator. Copied from the same bit in the interrogation which caused this reply. 0 Unsynchronized. AI bit follows. 1 Synchronized. EPOCH field follows.
AI	Altitude/Identity. Copied from the same bit in the interrogation which caused this reply. 0 Reply contains Mode C altitude. 1 Reply contains Mode A code.
EPOCH	Synchro-DABS epoch time. Copied from the interrogation which caused this reply.
PBUT	Pilot acknowledgment bits. Set from the model file whenever a pilot acknowledgment is requested. 00 No acknowledgment. 01 Cannot comply. 10 Will comply. 11 Request test transmission (not used by ARIES).
B	Air-to-ground downlink request (B=1). The ground is requested to allocate channel time for a COMM-B downlink. Set from the model file.

DEFINITION OF FIELDS (continued)

Fields	Significance
FR	Flight rules. Set from the model file. 0=VFR; 1=IFR.
ALTITUDE/IDENTITY	If AI=0, this field contains the Mode C altitude. If AI=1, this field contains the Mode A code. The bit order, using the standard ATCRBS pulse nomenclature is: $C_1A_1C_2A_2C_4A_4{}^{OB}{}_1{}^{D}{}_1{}^{B}{}_2{}^{D}{}_2{}^{B}{}_4{}^{D}{}_4$
MB	A fixed format downlink message field. The same MB is returned by ARIES in all COMM-B downlinks.

Device: Fruit Reply Generator
Device Number (octal): 50
Mask Bit: 2

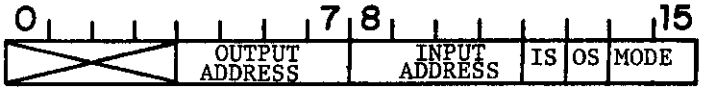
S,C: Only normal functions. An interrupt is generated if a target does not request data from the controller within 5 msec of the last load (error condition).

P: Identical to IORST, but only affects this device.

IORST: Both buffer address registers are set to 4 (the first address used in the memory), the mode is set to interface loop test mode, and the status of both buffers is set to write (0 for the output buffer, 1 for the input buffer). The microprocessor controller reinitializes itself and the reply generators.

DIA: Reads one word from the input channel. After four words are read, the input buffer status will switch state. Input formats are shown below. Note: The interface must be in RPG diagnostic or loop test mode for the DIA to read meaningful data.

DIC: Reads the interface status.



Output Address: The address of the next output buffer memory address to be read or written. Only addresses 4, 5, 6, and 7 occur.

Input Address: The address of the next input buffer memory address to be read or written. Only addresses 4, 5, 6, and 7 occur.

IS: Input buffer status

- 0: CPU can read the buffer.
- 1: Microprocessor controller can write into the buffer.

OS: Output buffer status.

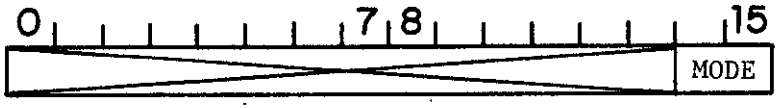
- 0: CPU can write into the buffer.
- 1: Microprocessor controller can read from the buffer.

Mode: Interface mode.

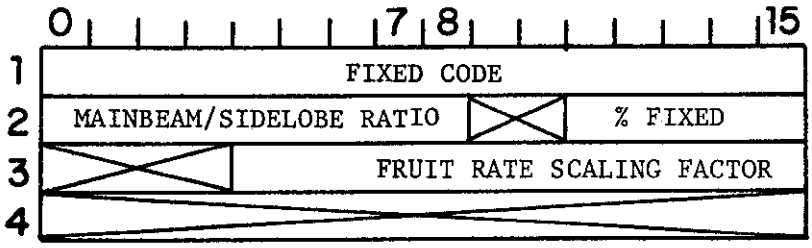
- 11: Normal
- 10: RPG Diagnostic
- 01: FAT Diagnostic
- 00: Interface Loop Test (note that in this mode OS is not controlled by the microprocessor and will only change value after each group of 4 DOA's).

DOA: Transfers one word to the output buffer memory. After four words are written, the output buffer status will switch state. Output formats are shown below. Output of words should normally be done only if OS=0, the sole exception being when the interface is in loop test mode. Note: Whenever the RPG parameters are changed, the RPG is reset to its initial state.

DOC: Interface mode control.



The Mode field is as defined for the DIC instruction.



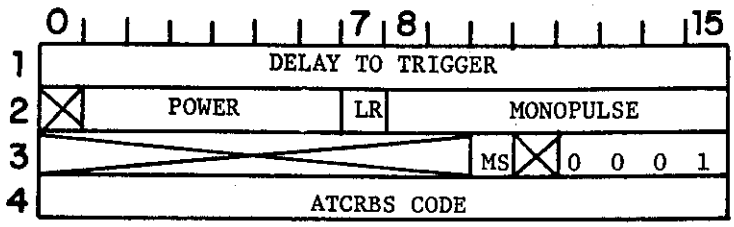
Output Format for Normal and RPG Diagnostic Modes (Note: Whenever these parameters are output, the RPG is reset to its initial state).

DEFINITION OF FIELDS:

Field	Significance
FIXED CODE	This is the fixed code to be used for that fraction of replies specified as being fixed code replies. Bit order: 1 $C_1A_1C_2A_2C_4A_4$0 $B_1D_1B_2D_2B_4D_4$ 1 0
MAINBEAM/SIDELOBE RATIO	This field determines the fraction of replies in the mainbeam, LSB = 100/256 percent. 0 All replies in sidelobe. 256 All of the replies are in the mainbeam. Values greater than 256 are treated as equal to 256.
% FIXED	The percentage of fruit replies that will have the prespecified fixed reply code (all other replies having randomly generated codes); LSB = 100/16 percent. 0 No fixed replies. 16 All fixed replies. Values greater than 16 are treated as being equal to 16.
FRUIT RATE SCALING FACTOR	If the desired average fruit rate in thousands of fruit per second is called F, then the fruit rate scaling factor should have the value 4096/F. The legal range of values for the fruit rate scaling factor is 64 to 4095, corresponding to average fruit rates of 64,000 to slightly more than 1,000 fruit per second, respectively. Values in the range 1 to 63 are illegal. (Note: to stop fruit reply generation, the interface should be set in loop test mode. Also, at the higher fruit rates the actual rate will be lower than the

DEFINITION OF FIELDS:

Field	Significance
FRUIT RATE SCALING FACTOR (Continued)	specified rate due to hardware limitations. A requested rate of 64000 fruit/sec will actually result in about 50000 fruit/sec. The effect is not linear and if precision is required the actual fruit rate should be measured. This is done by placing a counter on the FTOA output line of one of the FAT boards (see Vol. 1 of this document)).



Input Format, RPG Diagnostic Mode.
Output Format, FAT Diagnostic Mode.

DEFINITION OF FIELDS:

Field	Significance
DELAY TO TRIGGER	This is the delay between the beginning of the previous fruit reply and the beginning of this fruit reply. LSB=1/16 μsec.
POWER	This field is identical to the power field of a non-fruit reply; LSB increment = 1 dB. 0 = -20 dBm 63 = -83 dBm } referred to the sensor's RF port (i.e., the reply will appear to the sensor as if it had these levels).
LR	Monopulse sign. This field determines whether the monopulse angle is to be measured to the left (LR=0) or to the right (LR=1) of boresight.
MONOPULSE	The units of this field depend on the particular sensor's monopulse calibration. For fruit replies, this value is determined by a random number generator. In terms of amplitudes, each increment attenuates Δ relative to Σ by .125 dB. A value of 0 gives Δ = Σ.
MS	Mainbeam (MS=0) or sidelobe (MS=1) bit. This field determines whether the fruit reply will appear in the mainbeam or the sidelobe. Sidelobe replies are attenuated relative to mainbeam replies by an amount specified by front panel switches.
ATCRBS CODE	The ATCRBS data bits of the fruit reply. The bit order, using the standard ATCRBS pulse designation, is: $1\ C_1A_1C_2A_2C_4A_4\ 0\ B_1D_1B_2D_2B_4D_4\ 1\ 0$ A code of all 1's in RPG diagnostic mode indicates that the microprocessor controller will generate a reply using the specified fixed code. This does not apply to FAT diagnostic mode.

Device: Self Test Unit
Device Number (octal): 62
Mask Bit: 9

S: Starts the reply processing portion of the STU listening for a new reply.

C: Inhibits reply processing by the STU, and clears the second of the two STU control registers. This is the preferred method of clearing this word, as it avoids possible timing errors that can arise if the interrogation time is cleared while the uplink type field UPSEL contains a non-zero value. For a similar reason, this register should always be cleared before changing the interrogation time via a DOA instruction.

P: Not used.

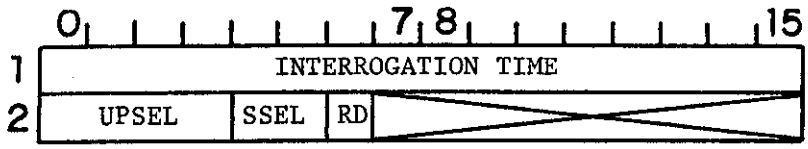
IORST: Stops any reply processing and interrogation generation, if either is active. Sets the second of the two control registers to all zeros.

DIA: Used to sequentially read up to 11 input words provided by the reply processing portion of the STU when a reply has been detected. The result of executing this instruction when BUSY=1 may be to lock up the STU data transfer, preventing interrupts until BUSY is cleared. The format of the 11 words is shown below.

DIB: Reads back from the control registers the first of the two control words transferred by the last DOA's. This is the interrogation time word.

DIC: Reads back from the control registers the second of the two control words last transferred to the interface by the last DOA's. This is the mode selection word.

DOA: Two sequential DOA instructions are used to transmit the two STU control words. The format of these words is shown below. To change any control field, both words must be sent, and the change does not take effect until the second word is received.



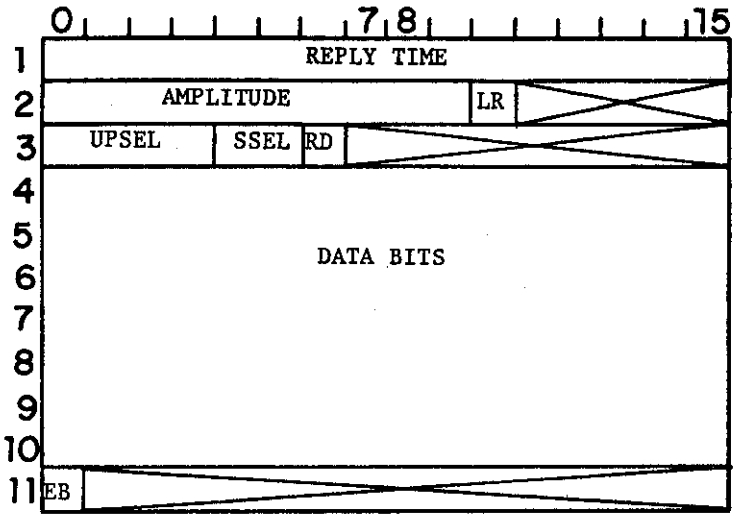
Output Format, Control Words (DOA)

DEFINITION OF FIELDS:

Field	Significance
INTERROGATION TIME	Every time the system range clock reaches this value, the selected interrogation will be sent. Until further control words are sent, this interrogation will therefore be sent every 4.096 msec. LSB=1/16 μsec.
UPSEL	Interrogation type selection. 0: Do not generate an uplink 1: ATCRBS/DABS All-Call Mode A 2: ATCRBS/DABS All-Call Mode C 3: DABS-only All-Call 4: DABS surveillance (56 bits: $200...00_{16}$) 5: ATCRBS Mode A (No P_4 pulse) 6: ATCRBS Mode C (No P_4 pulse) 7: ATCRBS Mode D (No P_4 pulse) 8: DABS COMM-A (112 bits: $7FF...FF_{16}$) 9: DABS COMM-A (112 bits: $718400 ... 00555555_{16}$) 10: DABS surveillance (56 bits: $2CFFAA ... AA_{16}$) 11: 12: 13: currently undefined 14: 15: DABS interrogation defined by front panel switches. The bit pattern is assumed to be that resulting <u>after</u> the error detection coding has been performed. No encoding is performed by the Self Test Unit.
SSEL	Selects which IF signal the reply processing portion of the STU will sample. 0: Σ channel 1: Δ channel 2: Ω channel 3: Unused

DEFINITION OF FIELDS (continued)

Field	Significance
RD	Selects the reply mode that will be expected. 0: ATCRBS 1: DABS



Input Format,
Reply Data (DIA)

DEFINITION OF FIELDS:

Field	Significance
Reply Time	The range clock time at which this reply was detected. LSB=1/16 μsec. Reply detection occurs at the leading edge of the first reply pulse.
Amplitude	An amplitude sample from the channel specified by SSEL. LSB = .080 dB (this is approximate, and varies with amplifier gain adjustments). 1023 = 0 dBm at the input to the A/D log amplifier. The following correspondences exist (approximately) between power levels at the A/D log amplifier input and power levels at the test points shown. The corrections should be added to the measured value to get the test point value. These are based on design information. For greater accuracy, a calibration chart should be consulted. Σ,Δ input to the $\frac{\pi}{2}$ hybrid: +3 dBm Σ,Δ monitor port: -10 dBm Ω output to sensor: +0 dBm Ω monitor port: -10 dBm
LR	Specifies whether the relative phase of Σ and Δ is such that the target appears to the right (1) or left (0) of boresight. This is generated independently of the value of SSEL. This bit is not valid except when the Σ and Δ amplitudes are equal, and near their maximum level.
RD, UPSEL, SSEL	Defined as in the control word output format.

DEFINITION OF FIELDS (continued)

Field	Significance
Data Bits	These are the sampled reply data bits. The format depends on the reply type. If RD=0 (ATCRBS reply mode) only the first 16 bits contain useful data, and the bit order is: $F_1C_1A_1C_2A_2C_4A_4XB_1D_1B_2D_2B_4D_4F_2S_{PI}$ If RD=1 (DABS reply mode) there are either 56 bits (Surveillance, All-Call) or 112 bits (COMM-B) of useful data. The format is identical to words 4-10 of the Controlled Reply Generator reply formats, except that the DABS address field is combined with a parity field in a 24 bit address/parity field. The STU does not contain the required circuitry for parity removal. This must be done by the software before the address field can be compared against the address actually sent.
EB	If set when a DABS reply has been processed (RD=1) this indicates that an error was detected in the pulse position modulation format of the reply. Further diagnostic action requires observing the IF signals with an oscilloscope.

Device: Radar Report Interface
Device Number (octal): 44
Mask Bit: 11

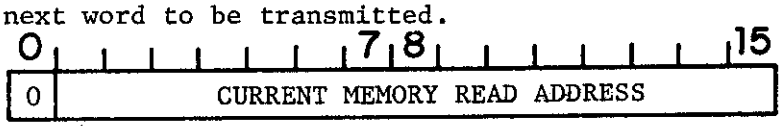
S: Starts transmission of the buffer defined by the current buffer address and word count values.

C: Stops transmission of the buffer, if any is in progress. Idle characters will be sent over the serial link.

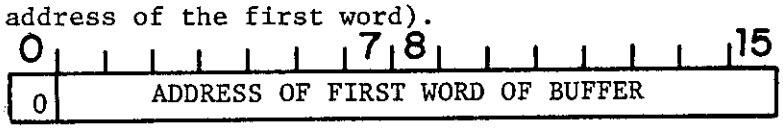
P: Not used.

IORST: Same as a CLEAR pulse.

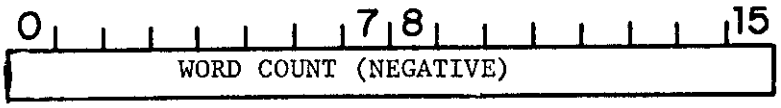
DIA: Reads the interface's memory address register, which points to the next word to be transmitted.



DOA: Transmits the output buffer starting address to the interface (the address of the first word).



DOB: Transmits the number of words in the output buffer to the interface.



The word count is expressed as the two's complement of the number of words to be transmitted.

The radar report formats in the buffer are shown below. In the interests of eliminating unnecessary detail, the only fields of these reports that have been labeled are the ones which ARIES may change from report to report. On the search report the constant bits indicate

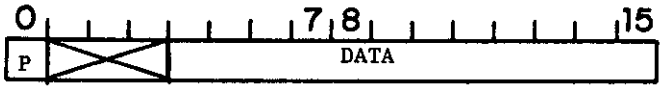
Test = 0, FAA=1, AF=1, AIMS Present = 0,

using the nomenclature of Reference 2. In the status report, all alarm bits are set to zero, standby CD available = 1, Sens. Det. On = 0, R.L. Discr. On = 0, Normal Sectors 1, 2, 3 = 1, Outer Contour = 0, Inner Contour = 0, Fixed Map On = 0, Sensitive Sectors 1, 2, 3 = 0. The general intent is that this message cause no alarm or unusual action when received by a NAS site. In the Real Time Quality Control report, the fields shown will actually contain fixed values adapted to the expectations of the NAS site receiving the data.

DEFINITION OF FIELDS:

FIELD	SIGNIFICANCE
Range, RTQC Range	Target range from the radar, LSB = .125 nm.
Azimuth, RTQC Azimuth	Target azimuth, clockwise from true north, LSB = $2\pi/4096$ radian = 1 ACP.
Run Length, RTQC Run Length	LSB = 4 ACP. ARIES sets this to some nominal constant value.
Time in Storage, RTQC Time In Storage	LSB = 0.125 sec. ARIES sets this to some nominal constant value.

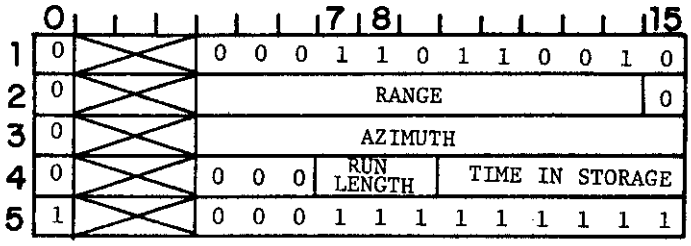
The format of individual words in the buffer is as follows:



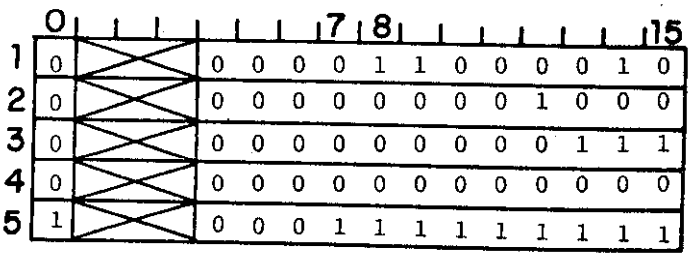
where

Data is the 12 data bits.
P determines whether odd (0) or even (1) parity is generated for this word.

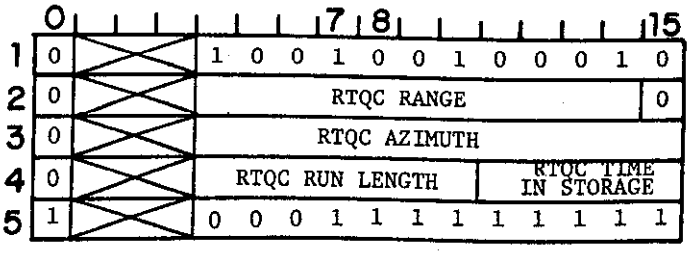
The interface is not concerned with the data content of words or with the message structure beyond the single word level. The higher level formats are entirely the concern of the transmitting and receiving software. However, for reference purposes, the three types of report transmitted by ARIES are shown below. Note that the required idle character is always included as the last word.



Radar Search Report



Status Report



Real Time Quality Control (RTQC) Report

Device: Status Formatter
Device Number (octal): 56
Mask Bit: 5

S: Starts the device polling cycle.

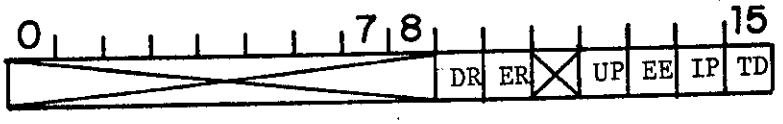
C: Sets ERROR ENABLE and UPDATE = 0 in the control register. The effect on polling is indeterminate, i.e., depending on the hardware state polling may continue or may be stopped.

P: Has no effect.

IORST: Starts the polling cycle, if polling is stopped. However, it sets ERROR ENABLE, UPDATE, TEST DATA and INHIBIT POLLING to zero in the control register, preventing interrupts. Sets DR=0, ER=0 (see the DIC instruction below).

DIA: Reads successive status words up to the maximum of 8. (Further DIA instructions will retrieve word 1 only). It is incorrect to execute a DIA instruction for this device if BUSY = 1. The format of the status words is shown below.

DIC: Reads various status bits, as shown.



DR: Data Ready. This indicates that the status formatter has a word to transfer to the computer. It will normally be 0 during polling, and 1 if polling stops due to a status change or an UPDATE request and all 8 words have not yet been read. It is intended to be used only for hardware diagnostic purposes. After each DIA instruction DR = 0 until the interface obtains the next word from the status formatter. Normally this word will arrive too quickly for the software to notice that DR = 0, but in the event of hardware failure this may not be the case.

ER: Error Report. This reads the state of the flip-flop which indicates if a status change has been detected during the current polling cycle (ER = 1). Again, this is useful primarily for hardware diagnostic purposes. However, in the case where polling has stopped due to an UPDATE request, this can be used to determine if a status change was also detected on the last polling cycle.

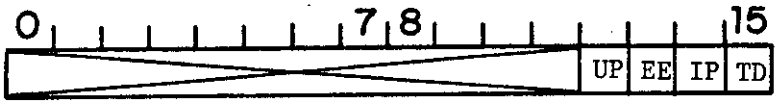
UP: The current value of the UPDATE bit in the interface control register. Setting this bit and the EE bit to 1 via a DOC instruction causes polling to stop at the end of the next complete polling cycle and an interrupt to be generated. If EE is not set, UP has no effect.

EE: The current value of the ERROR ENABLE bit in the interface control register. If set to 0 via a DOC instruction this bit prevents polling from being stopped and an interrupt generated even though the status bits change or an update is requested. This is useful when the Status Formatter or one of the devices it monitors is first started up or stopped, as this will likely cause status changes that are not of interest.

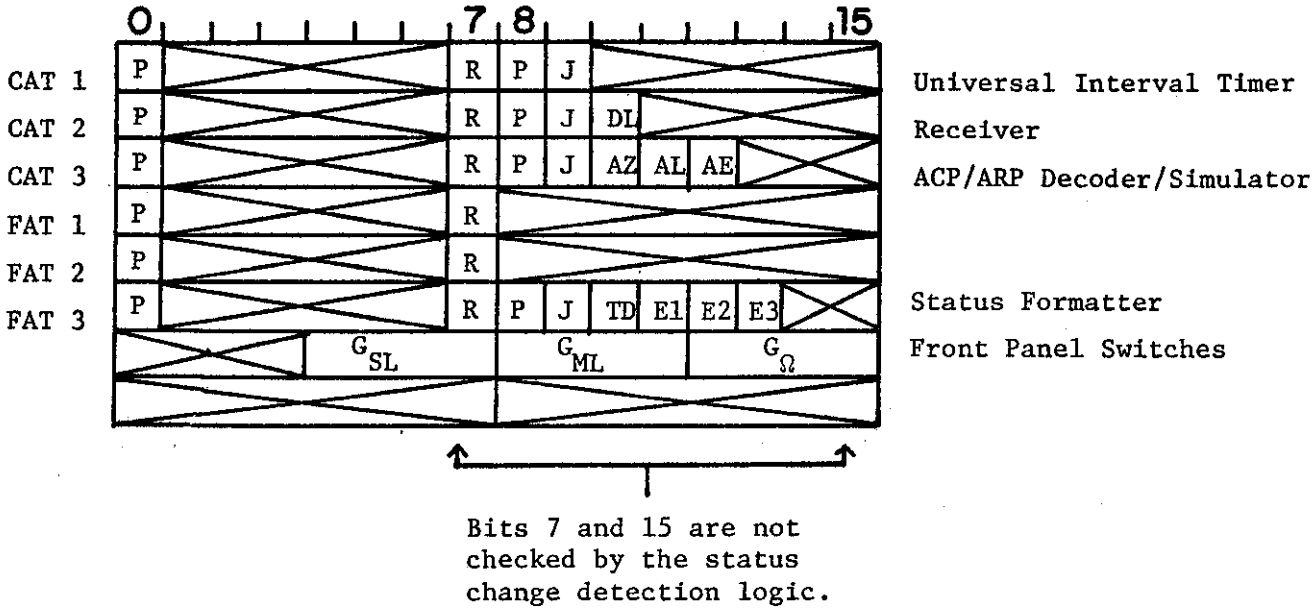
IP: The current value of the INHIBIT POLLING bit in the interface control register. If set to 1, this bit prevents device polling from taking place. Instead, the value of the TEST DATA bit is placed on all the input lines to the status formatter, and that value should appear in all 128 bit positions of the status words. This is a status formatter diagnostic mode.

TD: TEST DATA. The test value to be placed on the status formatter inputs when INHIBIT POLLING is set. Used for diagnostic purposes.

DOC: Used to transfer the control bits to the interface. The bit definitions are as for the DIC instruction.



Input block format read by DIA instructions:



Definitions of fields:

Field	Significance
P	Power on. A 1 indicates that the device is connected and powered up.
R	Ready to reply. If this bit is 0, the corresponding CAT or FAT is disabled. Normally only one FAT should have this bit set. After each FAT replies, its R bit goes to 0 and the next FAT's R bit goes to 1. Normally all CAT's are ready (R=1). For CAT's, this bit is turned off by a signal which occurs every time the Universal Interval Timer overflows, and turned on by a signal which occurs whenever an ATCRBS/All-Call interrogation is detected.
J	This is a manual jumper connection on several of the devices which can be used to indicate that a modification has been made or that some other special condition applies.

Definition of fields (continued)

Field	Significance
DL	Data Lost. This is an error condition indicating that data was not transferred to the computer from the Receiver quickly enough to prevent overwriting by the arrival of subsequent data.
AZ	0: The ACP/ARP Decoder/Simulator is generating simulated ACP's and ARP's. 1: ACP's and ARP's are being received from the sensor's antenna.
AL	ARP Late. More than 16384 ACP's were received between two ARP's.
AE	ARP Early. Fewer than 16384 ACP's were received between two ARP's.
TD	Test Data. The current value of the Test Data bit in the Status Formatter control register.
E1, E2, E3	Status Formatter error conditions, which should be referred to a hardware engineer. E1 indicates that the Transfer Acknowledge signal is present even though Data Ready was not raised (these are signals between the Status Formatter and its interface board). E2 and E3 indicate different circumstances under which Transfer Acknowledge remained up too long.
G_{SL}	Sidelobe gain. This reads the corresponding front panel switch. This indicates the amount of additional attenuation placed in the Σ and Δ lines when a reply is outside the mainbeam. LSB = 1 dB, 0 = 27 dB attenuation, 15 = 42 dB attenuation.
G_{ML}	Mainlobe gain. The amount of attenuation indicated is placed in the Σ and Δ lines for all replies, both controlled replies and fruit replies. This serves to adjust the output levels to match the sensor's desired input levels, and in conjunction with G_{Ω} is used to set the relative levels of the main and omni antennas. LSB = 1 dB, 0 = 0 dB attenuation, 15 = 15 dB attenuation.
G_{Ω}	This performs a similar function to G_{ML}, but for the Ω signal. LSB = 1 dB, 0 = 0 dB attenuation, 15 = 15 dB attenuation.

Device: Universal Interval Timer
Device Number (octal): 54
Mask Bit: 4

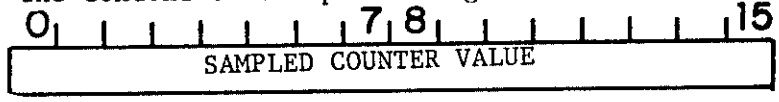
S: Enables one clock interrupt (i.e., by setting BUSY and clearing DONE, the logic is set so that the next clock overflow will clear BUSY, set DONE and cause an interrupt if interrupts are not masked).

C: Will clear BUSY and DONE, preventing further timer interrupts.

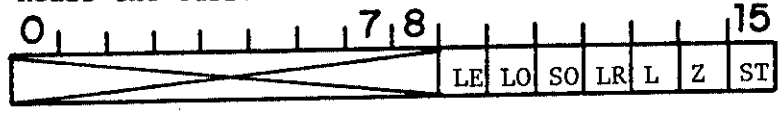
P: Causes actions specified by the LR, L, and Z control bits (see below) to take place. They will not occur until this pulse is generated.

IORST: Inhibits timer interrupts. Does not affect control bits. Note: This implies that if the counter is running, it will continue to do so. If it overflows, the signal will be sent to the CAT target cards, disabling their reply generation logic until an ATCRBS interrogation or an IORST occurs.

DIA: When the LR bit of the control register is set, this will read the last sampled counter value. (The counter is sampled when the LR bit is set and the P line is pulsed). If the LR bit is not set, the content of the preset register is returned by the DIA instruction.



DIC: Reads the current status bit values.



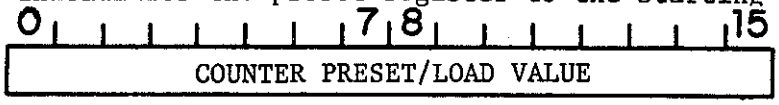
LE: Load the counter from the preset register on an external signal*.
LO: Load the counter from the preset register on overflow*.
SO: Stop the counter on overflow.
LR: Load (0) or Read (1) the counter*.
L: Load the counter from the preset register*.
Z: Zero the counter.
ST: Start (0) or stop (1) the counter.

The P line must be pulsed for LR, L, or Z to take effect.

*Note: None of the counter loading operations will work properly if LR=1 at the time of the load. For safety, LR should normally be left at 0. This also makes it unsafe to read the counter if either LE or LO is in effect, as the timing might be such as to prevent proper loading.

To load the counter directly with the preset register value, set LR=0, L=1, and pulse the P line. (The preset register is loaded by a DOA instruction). To sample the current counter state and store the value in the sample register set LR=1 and pulse the P line. (This value can then be read by a DIA instruction if LR=1).

DOA: Initializes the preset register to the starting time for the counter.



DOC: Initializes the control bits The format and definitions are as for the DIC instruction.

Device: Random Number Generator
Device Number (octal): 60
Mask Bit: This device generates no interrupts.

S,C: Have no effect.

IORST, P: Reset the generator to the beginning of its sequence.

DIA: Obtains successive 16 bit uniformly distributed random numbers.