Project Report ATC-89

The DABS Calibration Performance Monitoring Equipment

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(CPME) is a special DABS to				
more DABS beacon sensors.				
and for calibration of the se	nsor off-boresite a	zimuth look-up table	. In addition, the CPME	
provides tests for DABS link	c integrity, by stori	ng an up link messag	e and parroting it back u	pon
command from the sensor.				
This document contains	all information neo	cessary to obtain a g	eneral understanding of	the
CPME system and its opera	tion. Detailed infor	mation necessary fo	r repair of the equipmen	tis
not contained in this docume	ent, but is supplied	with each CPME sys	tem.	
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CONTENTS

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1.0	INTRODUCTION		1
		General Overview of CPME Operation	1 1
		<pre>1.2.1 Reception 1.2.2 Transmission 1.2.3 Transponder Interfaces</pre>	1 4 5
		Diagnostic and Repair Features Physical Features	5 7
2.0	2.0 FUNCTIONAL DESIGN		
	2.1 2.2	High-Power Transmitter External Logic	9 9
		2.2.1 ELR1 Card 2.2.2 ELR2 Card 2.2.3 ELR3 Card	10 14 19
3.0	ENVI	RONMENTAL SYSTEM	23
4.0	4.0 POWER DISTRIBUTION		
	4.2	Over-Voltage Protection Circuit Breakers Power Consumption	26 26 26
ACKN	OWLED	GMENTS	27
APPE	NDIX	A CPME Operating Procedures	A-1
APPE	NDIX	B Exceptions and Clarifications to Calibration and Performance Monitor Equipment (CPME) Engineering Requirement, FAA-ER-240-29	B-1

LIST OF ILLUSTRATIONS

•

1	DABS Calibration Performance Monitoring Equipment (CPME), External View	2
2	DABS Calibration Performance Monitoring Equipment (CPME), System Block Diagram	3
3	CPME with Front Door Open	6
4	CPME, As Installed	8
5	CPME Lockout Logic	11
6	Transmitter Duty Cycle Limiter, Modulator Delay Equalizer	13
7	High Power Transmitter Control Logic	15
8	Power-Up/Power-Fail Circuitry	16
9	Selectable Turn-Around Delay Circuitry	17
10	Standard Message Interface Processor	21
11	Standard Message Interface Processor Flowchart	22
12	Environmental Controls	24
13	Thermal Operating Characteristic	25

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1.0 INTRODUCTION

1.1 General

The DABS Calibration and Performance Monitor Equipment (CPME) is a special purpose test set required to verify DABS sensor monopulse azimuth accuracy, to calibrate the sensor off-boresight azimuth look-up table* at a given sensor site, and for checking DABS datalink integrity. CPMEs are permanently installed at surveyed sites within the coverage patterns of one or more DABS sensors, and each is assigned its own DABS discrete address (wiredin ID number). The weatherproof enclosure, which permits the CPME to be operated unattended over a wide range of environmental conditions, contains:

- 1) A modified DABS transponder,
- 2) A phase-locked 1090 MHz oscillator,
- 3) A special high duty cycle RF amplifier for providing the high level test signals needed at the DABS sensor, even at ranges up to 20 miles,
- 4) Special logic to permit the CPME to send status messages and to parrot uplink messages to the sensor,
- 5) Self-test and diagnostic circuitry, and
- 6) Power supplies and control circuits to permit all of the above to operate from AC power mains.

This document describes the CPME hardware and provides information necessary to understand its operation. It does not provide information sufficiently detailed to repair the CPME.

A detailed operating guide is provided as Appendix A and clarifications and exceptions to the CPME specification (FAA-ER-240-29 Amendment 1, Spec. Change 1) are included as Appendix B.

Each CPME is provided with a weather protected horn antenna intended for installation atop a tall tower, 150 feet of antenna cable, and a power cable. (See Figure 1).

1.2 Overview of CPME Operation

1.2.1 Reception

DABS interrogation signals (see Figure 2) pass through a circulator, a filter (to eliminate out-of-band signals), a power limiter (for front-end

As specified in FAA ER-240-26, Section 3.4.11 and 4.5.4.3.



Fig. 1. DABS Calibration Performance Monitoring Equipment (CPME), external view

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Fig. 2. DABS Calibration Performance Monitoring Equipment (CPME), system block diagram

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protection), and a variable attenuator (used to set the receiver sensitivity) before reaching the DABS transponder. The DABS transponder receiver is employed, but only one channel is used (i.e., the transponder's diversity capability is not used). Mode decoding and reply encoding are performed by unaltered transponder circuitry.

The TTL reply leaves the transponder and is delayed for 0, 128, or 256 microseconds as desired (causing the CPME to appear as though it is 0, 10, or 20 miles further away from the sensor than it actually is). After this additional turnaround delay, the TTL signal necessary to generate a reply is sent to one of two modulators: either high-power or low-power.

1.2.2 Transmission

The RF transmitter section is driven either by an ultra-stable 1090 MHz oscillator, which is isolator protected, or by an external variable frequency signal source (during DABS sensor acceptance testing). The CW signal is fed into a variable attenuator. This attenuator sets the RF reply level if the CPME is operating in the low-power mode, or sets the drive level to the power amplifier if the CPME is operating in the high-power mode.

The transponder's transmitter section is not used, and the original power supply has been removed from the transponder. An additional front panel connector has been added to the transponder to allow external power input and to communicate with the external logic rack.

In the low-power mode, the CW signal is modulated by a PIN diode switch and then filtered to eliminate out-of-band signals. The modulated signal is sampled by a built-in power monitoring system consisting of a directional coupler, pads, and a calibrated crystal detector. Output from the sampling detector can be viewed on an oscilloscope, and the power output of the CPME can be determined using calibration information provided with each CPME. The power monitor system is most useful when the CPME is operated in the high-power mode, as low-power signals are typically too small to be measured accurately. Modulated reply signals exit through the circulator and are fed to the antenna. The maximum output in the low-power mode, +20 dBm at the CPME RF port, allows the CPME to be placed up to 2000 feet away from the sensor.

The high-power mode allows the CPME to be placed up to 20 miles from the sensor, as it provides output power as high as +45 dBm at the CPME RF port. The high-power mode is necessary in cases where the CPME is to be shared with more than one sensor (in this case more than one directional horn antenna would be fed from one CPME).

Operation in the high-power mode is similar to that in the low-power mode, except that a separate modulation, amplification, and attenuation system is used. The CW signal from the low-power variable attenuator is further attenuated (to protect the amplifier's RF input), and then fed to the RF power amplifier. Here, the CW is both modulated and amplified, and the reply power level is then set by a high-power variable attenuator.

The amplifier unit itself is a 4-stage triode tube amplifier. Other components of the high-power amplifier system are: power supplies (+6V, +28V, and +1000V), switches for re-routing the RF when changing from low to highpower mode (see Fig. 3), a high-power variable attenuator, and a modulator for the tube amplifier. In the event that any of these items should fail, the CPME will still function correctly when switched to the low-power mode.

1.2.3 Transponder Interfaces

The transponder also interfaces with the external logic rack via the Standard Message Interface (SMI). Data interchange between the transponder and external logic rack via the SMI allows the CPME to operate in a test mode wherein the CPME "parrots" uplink messages. The SMI data capability also allows the CPME to report its status to the sensor. Thus a "remote diagnostics" function is provided.

Status reporting provisions are included to transmit (as a Comm-B downlink message): enclosure over-and-under temperature, 1090-MHz oscillator out-of-phase-lock condition, power failure condition, miscellaneous hardware faults and interrogation lockout states. The entire status reporting system can be inhibited if desired.

1.3 Diagnostic and Repair Features

In addition to the dual transmitter feature and status reporting to sensor features the CPME includes other built-in test and diagnostic aids. Extensive built-in diagnostic logic circuits exist to detect hardware failures and thereby facilitate repair. The results of these built-in test circuits are displayed on a main CPME control panel, along with various other indicators and controls for the system. Another built-in diagnostic tool is a digital voltmeter. This feature allows a repairman to quickly check all seven of the CPME's power supplies by setting a single control.

Finally, the Bendix transponder is equipped with a test jack on its front panel. Various internal signals are brought out to this connector so that they can be viewed with an oscilloscope and faults isolated.



Fig. 3. CPME with front door open

1.4 Physical Features

The CPME unit features a lockable weather-tight enclosure for outdoor stand-alone operation, an air-to-air heat exchanger for cooling, a 500 watt heater, a sun shade, mounting legs, highly visible external "power on" and "fault" indicator lamps, and an external electrical convenience outlet so that oscilloscopes and other test equipment can be powered at the CPME if desired. Overall dimensions of the CPME unit, exclusive of sunshield and mounting legs, are 30" wide, 35" high, and 16" deep. Legs raise the enclosure 12" above the mounting pad. Its weight is approximately 200 pounds.

Figure 3 illustrates the unit as it would be seen by service personnel. A flush door ($30'' \times 35''$) permits access to all components. In addition to the front door, a small lockable rear door allows easy access to the wire-wrap backplane of the logic rack.

The CPME antenna consists of an environmentally protected horn antenna, a coax-to-waveguide adapter, and a mount. The mount features 360° azimuth adjustment for "aiming" the antenna (no elevation adjustment is necessary). A typical installation is illustrated in Figure 4.



Fig. 4. CPME, as installed

2.0 FUNCTIONAL DESIGN

2.1 High-power Transmitter

A high-power, high duty cycle transmitter was developed for the DABS CPME to satisfy a requirement dictated by (1) the possibility of sharing one CPME between two or more sensors and (2) the high-power level (-24 dBm) required at the sensor during monopulse accuracy tests*. The high duty cycle requirement is based on the Texas Instruments DABS monopulse calibration and accuracy test algorithm in which 80 interrogations are transmitted during a 44 msec beam dwell time interval (PRF = 1800 replies per second required from CPME).

Tests on the high-power transmitter have verified that it is able to support this high PRF required during monopulse calibration. The capability of producing pulse repetition frequencies of 2000 replies/sec for DABS short and 1000 replies/sec for DABS long simulated replies has also been established. Simulated DABS short replies are 60 μ sec transmissions of a 50% duty cycle 1 MHz signal. Simulated DABS long replies are 116 μ sec transmissions of a 50% duty cycle 1 MHz signal. Note that the overall duty cycle should not exceed 0.005, when averaged over a 1 second interval.

The RF power amplifier tube used is a General Electric model C-2173 microwave triode amplifier. The C-2173 is a 4 stage amplifier operating at 1090 MHz center frequency capable of providing an output of at least 300 watts peak at 0.01 duty, with an input of 10 milliwatts.

The RF input is a CW signal to the first stage with the cathodes of the first two stages modulated to generate the required RF pulses. The last two stages are self-biased using a 22 volt zener on the cathodes and are RF keyed by the pulses of RF generated by the first two stages.

The output vs. input characteristic for the C-2173 shows that the amplifier has considerable compression. This is desirable for stability with input and with life. However, it may be possible to overdrive one of the intermediate stages without obtaining excessive output power if the input is allowed to go beyond the 10 milliwatt level.

Normal power output is 400 watts at 1000 volts B+. The power output may vary considerably with B+. It is not recommended that the B+ level be raised over 1000 volts.

2.2 External Logic

Logic not contained in the transponder is termed external logic. This logic is contained on three wire-wrap boards, ELR1, ELR2 and ELR3, located in

See FAA-ER-240-26, p. 534, paragraph 4.5.4.3.1.

the External Logic Rack* (see Fig. 3).

- ELR1 contains the CPME lockout logic, the transmitter duty cycle limiter, the modulator delay equalizer, the high-power transmitter control logic, and the power-up/power-fail circuitry.
- ELR2 contains the logic necessary to delay CPME replies by 0, 128, or 256 microseconds (in addition to those delays specified for DABS and ATCRBS replies.)
- $\underline{\text{ELR3}}$ contains logic which allows the CPME to communicate with the DABS sensor via the DABS data link.

When referring to logic signal names on the diagrams shown in the following sections, note that the following nomenclature has been standardized:

Logic Signal Name	Meaning
NAME.A NAME.F	Inverter (amplifier) output Flip-flop
NAME.G	Gate
NAME . L	Latch
NAME.M	Multiplexer
NAME*	Open collector signal
NAME	Active low signal

2.2.1 ELR1 Card

2.2.1.1 CPME Lockout Logic

2.2.1.1.1 The ATCRBS lockout function in the Bendix transponder is consistent with CPME requirements, and no modification was necessary.

2.2.1.1.2 The ATCRBS/DABS All-Call, Auxiliary (DABS-only) All-Call and Auxiliary Discrete Reply lockout system in the transponder was replaced with the system shown in Figure 5. When an interrogation is received, it is held in the transponder's uplink register. If the uplink is valid and is of a type which has not previously been locked out, then three uplink bits (IT and the two DL bits) are taken together with the present lockout states to address a PROM which will determine the next lockout state. The next lockout state is determined as in paragraph 4.4.3.1 of FAA-RD-74-62 (ATC-30).

2.2.1.1.3 The standard timeout is initiated each time the CPME replies to a discrete address interrogation from a standard DABS sensor. When the standard timer times out, only the ATCRBS/DABS All-Call lockout flip-flop is cleared.

The External Logic Rack has three unused slots for future expansion. Available power supplies (+5V, +12V and -12V) can provide ample additional current.



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Fig. 5. CPME lockout logic

2.2.1.1.4 The auxiliary timeout is initiated each time the CPME replies to a discrete address interrogation from any DABS sensor, either standard or auxiliary. When the auxiliary timer times out, all four lockout flip-flops are reset.

2.2.1.1.5 When an ATCRBS/DABS All-Call interrogation is received, the ATCRBS/DABS All-Call flip-flop is set. If the CPME is locked out to ATCRBS/DABS All-Calls and not to ATCRBS, then the ATCRBS/DABS all-call signal is gated to zero, regardless of whether the received interrogation is an ATCRBS/DABS all-call or not. When this condition occurs, the CPME replies to ATCRBS/DABS all-calls with the proper type of ATCRBS replies (either mode A or mode C). This allows the CPME to "look like" an ATCRBS transponder for purposes of testing the sensor with ATCRBS replies.

2.2.1.2 Transmitter Duty Cycle Limiter

The CPME must be capable of replying to all combinations of ATCRBS and DABS interrogations for which the resulting transmitter duty cycle is not greater than 0.005, averaged over a 1-second period. This means that the transmitter must be able to provide RF output for a total of 5 milliseconds each second.

A simple numerical integration scheme can be used to determine the overall duty cycle, as illustrated in Fig. 6. The TTL reply, which has gone through the selectable 0, 128, or 256 usec delay (DELAYED REPLY), is used to enable a high-speed counter. Every ATCRBS reply pulse gates the counter on long enough to increase the count by four, and each DABS pulse increases the count by either five or ten, depending upon the bit pattern in the reply. When the count reaches 50,176, corresponding to a minimum of 5 milliseconds of RF "on" time, a flip-flop is set which indicates that a duty cycle fault has occurred. This signal is displayed on the CPME control panel, and a bit is set in further CPME replies to indicate that a fault has occurred. The CPME continues to operate normally until the counter reaches 57,344, corresponding to 5.7 milliseconds of RF "on" time. At this point a flip-flop is set to indicate that the duty cycle has been exceeded, and further replies are inhibited by gating them off. At the end of every second, a pulse comes from a pulse generator to clear the fault conditions, if any, and reset the counter. Note that the maximum duty cycle of the tube amplifier is 0.01, so safe operation is assured.

2.2.1.3 Modulator Delay Equalizer

Figure 6 shows a 120 nsec delay difference between replies to the PIN diode switch and the power amplifier. This delay line compensates for the fact that the PIN diode switch has a very fast turn-on characteristic, while the tube amplifier does not. Thus the delay between the TTL signal and RF turn-on is the same in both high- and low-power modes. Typical total delay between the TTL signal on the ELRl card and the RF output (in either high- or low-power mode) is 220 nsec.



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Fig. 6. Transmitter duty cycle limiter, modulator delay equalizer

2.2.1.4 High-power Transmitter Control Logic

When initially turning the high-power transmitter on, it is necessary to provide several interlocks and detection of fault conditions to avoid damaging the tube unit. The system is illustrated in Fig. 7. When power is first turned on or when the CPME is in the INITIALIZE mode, a RESET signal is generated which allows the state of the HIGH-POWER/LOW-POWER MODE select switch to be latched. The HIMODE.L signal state is displayed on the CPME front panel as "HI-PWR XMTR SEL" for high-power mode selected. The presence of this signal does not indicate that the high-power transmitter is in fact active; it merely indicates that we wish it to be active. The HIMODE.L signal is used to switch in the appropriate elements for either high-or low-power operation by controlling a DPDT (double pole, double throw) switch. When the DPDT switch's built-in indicator circuits show that the switch is in the high-power position, the HIPWR signal goes true. This signal activates the power supplies for the tube amplifier, and gives a visual indication (the 1KV, 6V ACTIVE LED on the control panel) that the high-power transmitter section is ready.

2.2.1.5 Power-up/Power-fail Circuitry

Refer to Figure 8. When the CPME is powered-up or initialized, the POWER-FAIL signal goes true and the ENABXMIT (enable transmission) goes false. After 64 seconds, the ENABXMIT signal goes true, which allows the CPME to reply to interrogations. The 64-second timeout is to allow the tube amplifier ample time to warm up, as well as to allow various transponder and CPME timers to time out. When another 64 seconds have elapsed (i.e., 128 sec after the CPME has been in the RUN mode with power on) the POWER-FAIL flag is cleared, and the CPME runs normally. The POWER-FAIL flag, when active, simply indicates that power to the CPME has been off for a while or that the CPME has recently been initialized. This feature is useful in performing remote diagnostics from the sensor, as it verifies that a CPME failure has occurred rather than a sensor failure and also indicates that someone may have changed CPME control settings. The POWER-FAIL flag is sent in reply transmissions, as a fault bit, during the first 64 seconds that the CPME is able to reply (i.e., 64 to 128 sec after power-up or initialization).

2.2.2 ELR2 Card

Figure 9 shows the logic needed to delay CPME replies by 0, 128, or 256 microseconds.

2.2.2.1 Delay Selection Logic

A switch on the CPME control panel is used to select the desired turnaround delay. The state of this switch is latched after power-up or initialization, and cannot be changed unless the CPME is re-initialized.



Fig. 7. High power transmitter control logic



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Fig. 8. Power-up/power-fail circuitry



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Fig. 9. Selectable turn-around delay circuitry

2.2.2.2 Zero Delay Selected

If zero delay is desired, the "DØ" signal goes true, which in turn generates a signal "NODEL" (no delay). The "NODEL" signal true condition holds all the delay circuitry in a reset condition, and also resets all fault conditions associated with the turn-around delay circuitry. When "DØ" is active, it gates the "REPLY" signal through to form "DELREP" (delayed reply) with only a few gate delays.

2.2.2.3 Fault Detection Circuitry

A design philosophy was followed which increases reliability and reduces field repair time. Wherever possible, invalid conditions are detected and displayed. For example, the "D-FLT" (delay fault) signal is generated when more than one turn-around delay time has been selected. This occurrence is logically impossible, but has in fact occurred due to bad chips, connector problems, and so forth. Another example shown is "C-FLT" (counter fault). The 13-bit counter should never overflow, but if it does an error is indicated. Two other fault detectors are located on the ELR2 card, but are not shown in Fig. 9 for simplicity. These are "REP-FLT" (reply fault), which is generated when any combination of "DAREP" (delayed ATCRBS reply), "DDABREP" (delayed DABS reply) and an undelayed reply are present simultaneously, and "MODE-FLT" (reply mode fault), which is generated when any combination of Mode A ATCRBS, Mode C ATCRBS, and DABS flip-flops are set simultaneously. The "MODE-FLT" signal true can indicate a failure in the transponder or a failure in the "MUTUAL SUPPRESSION DRIVER CIRCUITRY" shown in Fig. 9.

2.2.2.4 ATCRBS Turnaround Delay

2.2.2.4.1 128 Microsecond Delay Selected

The "REPLY" and "DIG SUP" (digital suppression) signals become active, which in turn set the "START" signal at the next rising edge of the "2MHz CLOCK". The "START" signal drives the "MUT SUP" (mutual suppression) line to the transponder, thereby inhibiting further decoding of interrogations while the delay is taking place.

The state of the "MODE-A" and "MODE-C" signals is then latched at the next rising edge of the 2MHz clock. No more than one of these signals should be true. Meanwhile, the "REPLY" signal from the transponder is simply gated out, and no delayed reply is generated as yet. 125 microseconds later, the "END125" signal is generated and gated with the true "D128" signal to produce a signal called "SET". The "SET" signal sends the "SET-A" and SET-C" signals to the transponder, causing the transponder to give an appropriate Mode A or Mode C ATCRBS reply 3 microseconds later. This reply is gated through the system to form "DAREP" (delayed ATCRBS reply), because the "SET" signal sets a flip-flop which allows this to occur. Thus the transponder has actually generated two ATCRBS replies: the first is lost, and the second one (which comes 128 microseconds after the first reply) is transmitted as the delayed reply. A short while later (157 microseconds after "START" goes true), the "END 157" signal becomes active, which returns the circuitry to its initial state by generating the "DONE" signal.

2.2.2.4.2 256 Microsecond Delay Selected

The same sequence of events occurs as occurred with the 128 microsecond ATCRBS delay, except that "END 253" is used to elicit the second ATCRBS reply from the transponder and "END 285" is used to reset the delay circuitry.

2.2.2.5 DABS Turnaround Delay

The DABS turnaround delay is handled in an entirely different manner from the ATCRBS delay. This is due to the different timing schemes involved (690 KHz clock for ATCRBS vs. 1 MHz clock for DABS replies). Note that ATCRBS/ DABS all-call replies are considered to be "DABS"-type replies insofar as the timing is concerned.

2.2.2.5.1 128 Microsecond Delay Selected

The first reply pulse and digital suppression signals are used to generate "START", as was the case with ATCRBS. 256 microseconds later, "END 256" is used to generate the "DONE" signal which resets the delay circuitry. The "DABS XMIT" (DABS transmission) signal goes true prior to the "REPLY" signal.

"DABS XMIT" is latched, and "DABS.L" is used to gate the DABS reply into a CMOS shift register chain where it is delayed for 128 microseconds. When the DABS reply emerges from the shift register delay, it becomes "DDABREP" (delayed DABS reply) and is sent out to the transmitter as the delayed reply.

2.2.2.5.2 256 Microsecond Delay Selected

Operation is similar to that described in the preceding paragraph, except that more shift registers are used to obtain a longer delay and "END 384" is used to reset the delay logic after completion of the DABS reply.

2.2.3 ELR3 Card

The logic contained on this card allows a message turn-around test to be performed between the sensor and CPME. It also allows the CPME to report its operating status to the sensor for remote diagnosis of CPME problems.

2.2.3.1 Initialization

The "RESET" signal completely clears the SM processor, and all fault conditions associated with it. After every SM interface transaction, the system is cleared (with the exception of PBUT, B-bit, and fault conditions) by the "SMCLR" (standard message clear) signal. The "SMCLR" signal becomes active 220 microseconds after the first leading edge of "SMC" (standard message clock), and so occurs after all SM interactions have taken place. Refer to the simplified schematic presented in Fig. 10.

2.2.3.2 Operation

The transponder has a uni-directional clock line output, "SMC", which provides the required timing for the interface. The transponder also provides a 1-bit bi-directional data bus, "SMD" (standard message data), on which uplink data is transferred from the transponder to the SMI processor, and downlink data is sent to the transponder from the SMI processor. The operation of the SMI processor is summarized in the flowchart of Fig. 11.



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Fig. 10. Standard message interface processor



Fig. 11. Standard message interface processor flowchart

3.0 ENVIRONMENTAL SYSTEM

The environmental system shown in Fig. 12 enables the CPME to operate satisfactorily outdoors. All temperature switches are located on a single heat sink, which senses the CPME's internal air temperature. The safe operating limits on this internal air temperature are shown in Fig. 13.

Each CPME system has been tested and shown to be completely functional over outside air temperatures ranging from $-10^{\circ}F$ to $+105^{\circ}F$. When operated in the high-power mode, the CPME's internal air temperature is typically $80^{\circ}F$ when the outside ambient is $-10^{\circ}F$.

Operation in the high temperature range is limited by the transponder (maximum transponder operating temperature is $+130^{\circ}F$) and by the efficiency of the heat exchanger. The heat exchanger limits the transponder's temperature to a rise of 25°F above outside ambient when the CPME is in the high-power mode, and 18°F in the low-power mode. Thus the CPME can safely operate outdoors in temperatures of 105°F for the high-power mode and 112°F for the low-power mode.



Fig. 12. Environmental controls

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Fig. 13. Thermal operating characteristic

4.0 POWER DISTRIBUTION

4.1 Over-voltage Protection

All CPME supplies with the exception of the 1000V supply are equipped with over-voltage protection. Additionally, the CPME is protected from power line transients.

All supplies have accessible voltage adjustments, except for the +12V and -12V supplies which are non-adjustable. The +5V and +28V have been fitted with knobs for ease of adjustment. The +6V, -20V, and +1000V supplies are screwdriver adjustable. The plexiglass high voltage protection plate must be removed before the voltage adjustment trimpot on the +1000V supply can be reached, so care should be taken when making this adjustment.

4.2 Circuit Breakers

Three circuit breaker switches are provided. A 2.5 amp breaker controls the "convenience outlet"; a 10 amp breaker controls the power to the 500 watt heater and to all fans, and a special 7.5 amp breaker controls power to the logic and RF components. The 7.5 amp breaker features immunity to current spikes which are often encountered during system power-up. This feature was required so that if, during normal field operation, AC power to the CPME is interrupted, when power is restored the CPME will power-up again normally without the need to reset the breaker by human intervention. Notice that the total current which could be drawn from the AC power line is 2.5 + 7.5+ 10 = 20 amperes, thus standard service can be used.

4.3 Power Consumption

Actual power taken by the CPME from the AC line is as follows.

a. Environmental System:

The heater uses 500 watts, and the heat exchanger's cooling fans use 50 watts.

b. RF, Logic, and Circulating Fans:

The low-power mode uses 240 watts, while the high-power mode uses 325 watts. Note that these figures are the "heat load" which the heat exchanger is required to dissipate.

c. Worst Combination:

The worst case power consumption occurs on cold days when the CPME is in the high-power mode, requiring 325 watts (electronics and circulating fans) plus 500 watts (heater) or a total of 825 watts drawn from the AC power lines.

Acknowledgments

The development of the DABS CPME took place under the guidance of R.R. LaFrey and J.D. Welch, MIT/Lincoln Assistant Group Leaders, <u>System</u> <u>Design and Evaluation</u>. Significant contributions to the design, construction, and checkout of the CPME were made by E.A. Crocker, J.L. Cataldo, A. Augustine, W.J. Grabowski, B.F. Adams, and B. Hutchings. The helpful suggestions regarding construction and thermal design given by R.G. Nelson and D.M. Nathanson are also gratefully acknowledged.

APPENDIX A

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TABLE OF CONTENTS

		Page
1.0	NORMAL OPERATION	A-1
	1.1 Set Call Sign	A-1 A-3 A-3 A-3 A-3
	1.6Set AT51.7Powerup1.8Check Supplies1.9Check CPME Control Panel Indicators1.10Adjust AT11.11Turn On Environmental System1.12Set PAM/PPM Switch	A-5 A-5 A-6 A-6 A-8 A-8 A-8
2.0	USE OF CPME DURING MONOPULSE ACCURACY TESTS	A-9 A-9 A-9 A-9

APPENDIX A

CPME OPERATING PROCEDURES

1.0 NORMAL OPERATION

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It is assumed that the CPME has been set up so that ample space is available all around the unit (to facilitate ventilation and repairs) and that if the unit is located outdoors, the sun shield has been attached. It is also assumed that the CPME unit has been connected to 120 VAC 20 ampere service.

1.1 Set Call Sign

The CPME will transmit a Comm-B reply with a dummy call sign contained in the extended capability MB field in response to a correctly addressed interrogation with RL=1 and MSRC=0001. The call sign consists of 42 bits which are transmitted in bit positions 47 through 88 of the Comm-B data field inclusive (see FAA-RD-74-62, paragraph 4.4.3.6). Set the 42-bit call sign as follows:

1.1.1 Remove board #3 (ELR3) from the "External Logic Rack" (see Fig. A-1).

1.1.2 Set call-sign switches as follows (switch set "ON" transmits a "ZERO", "OFF" transmits a "ONE"):

<u>Bit #</u>	Pack Location	<u>Switch #</u>	Bit #	Pack Location	Switch #
47	U58	1	70	U36	6
48	U12	2	71	U36	7
49	U12	1	72	U36	8
51	U12	3	73	U48	1
52	U12	4	74	U48	2
53	U12	5	75	U48	3
54	U12	6	76	U48	4
55	U12	7	77	U48	5
56	U12	8	78	U48	6
57	U24	1	79	U48	7
58	U24	2	80	U48	8
59	U24	3	81	U60	1
60	U24	4	82	U60	2
61	U24	5	83	U60	3
62	U24	6	84	U60	4
63	U24	7	85	U60	5
64	U24	8	86	U60	6
65	U36	1	87	U60	7
66	U36	2	88	U60	8
67	U36	3			
68	U36	4			



Fig. A-1. DABS CPME: Internal view

1.1.3 Carefully replace ELR3 board in the proper slot (slot #3) of the External Logic Rack.

1.2 Set ATCRBS Mode C Code (altitude simulator)

On the CPME CONTROL PANEL locate the two sets of switches marked "ALTIMETER". The transmitter bits are set as follows (see Fig. A-2):

Bit	Switch Bank	Switch #
A1	Left	1
A2	Left	2
A4	Left	3
B1	Left	4
в2	Left	5
В4	Left	6
C1	Left	7
C2	Right	1
C4	Right	2
D2	Right	3
D4	Right	4

Note: Switch set "ON" transmits the bit, switch set "OFF" does not. Bit Dl is not used (always zero). The zero feet altitude code is obtained by setting B2, B4, and C2 "ON", all others "OFF".

1.3 <u>Set ATCRBS Mode A Code</u> on thumbwheel switches provided on CPME CONTROL PANEL.

1.4 Set Receiver Threshold

Adjust variable attenuator AT2 for the desired threshold level. A setting of 26 dB results in an input sensitivity of approximately -40 dBm as referenced to the CPME RF port. Similarly, a setting of 66 dB results in a sensitivity of approximately \emptyset dBm. It is recommended that attenuator AT2 should always be set at some value greater than 8 dB for the purpose of protecting the receiver. See calibration information on each CPME for more accurate setting.

1.5 Select Operating Modes

1.5.1 Select \emptyset , 128, or 256 µsec additional turn-around delay time by setting the TURNAROUND DELAY control (see Fig. A-2).

1.5.2 Set the INITIALIZE/RUN switch to the RUN position. Note: after powerup, if it is necessary to change the Turnaround Delay setting or Transmitter Power switch, then put the INITIALIZE/RUN switch into the INITIALIZE position and then back to the RUN position.


Fig. A-2. CPME control panel diagram

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1.5.3 Set the TRANSMITTER POWER (XMTR PWR) switch to either HIGH or LOW power, as desired. At the CPME RF port, the output power in the low-power mode can be varied from -80 dBm to +21 dBm in 1 dB steps, whereas output power in the high-power mode can be varied from -9 dBm to +51 dBm continuously. For greatest accuracy in power level setting, it is recommended that the high-power mode output should be used only in the range from +11 dBm to +51 dBm. It is also recommended that the low-power mode be used whenever possible, especially during hot weather.

1.5.4 Set the status REPORTING TO SENSOR switches as desired for status reports. In response to a correctly addressed interrogation with RL=1 and MSRC=0001, the CPME shall transmit a Comm-B reply with bits 38 through 46 defined as follows:

1.5.4.1 All zeroes if the ALL STATUS switch is in the INHIBIT position.

1.5.4.2 With the ALL STATUS switch in the ENABLE position and the LOCKOUT STATE switch in the INHIBIT position, the CPME fault bits (defined in paragraph 1.9.5.2) are transmitted in bits 38 through 42 inclusive. Bits 43 through 46 inclusive are transmitted as zeroes.

1.5.4.3 With the ALL STATUS switch in the ENABLE position and the LOCKOUT STATE switch in the ENABLE position, the CPME fault bits are transmitted in bits 38 through 42, and the CPME lockout state status (defined in paragraph 1.9.4) is reported in bits 43 through 46.

1.5.4.4 Whenever the ALL STATUS switch is in the ENABLE position, the FR bit (bit 19 of <u>any</u> surveillance or Comm-B reply) is transmitted as a "one" if any of the fault bits are set (logical "OR") and "zero" otherwise. When the ALL STATUS switch is in the INHIBIT position, the FR bit is a "zero".

1.6 <u>Set AT5</u>

Attenuator AT5 directly controls the output power in the low-power mode. Set to 11 dB for normal low-power mode operation, thus giving approximately +10 dBm output at the CPME RF port. See calibration information on each CPME for more accurate setting. In the high-power mode, AT5 sets the drive level to the RF power amp. Set AT5 to 6 dB for normal high-power mode operation, thus giving +10 dBm input to the GE RF power amp.

1.7 Powerup

1.7.1 Make sure all circuit breakers are in the OFF position.

1.7.2 Connect antenna system cable to the type N connector on the outside of the CPME.

1.7.3 Connect AC power (110 VAC, 20 A) to the CPME through the Bendix connector, on the outside of the enclosure, using the power cord provided.

1.7.4 Turn the circuit breaker marked "RF/LOGIC" to the ON position. The handle should light up red.

1.7.5 The green lamp on the outside of the CPME enclosure should light up.

1.8 Check Supplies

Turn the ON/OFF switch of the DVM to the ON position. Check the supplies by setting the DVM's selector switch to the desired supply and reading the value on the Digital Volt Meter (DVM). The DVM is accurate to about 2%. Note that the 6V and 1000V supplies are active only when the high-power transmitter has been selected. Also note that the 6V supply has been set to about 5.8V. This lower filament voltage increases the life expectancy of the GE RF power amp, and the voltage can be increased as the tube ages. Turn off the DVM.

1.9 Check CPME Control Panel Indicators

1.9.1 Turnaround delay indicator should correspond to selected turn-around delay. If not, then re-initialize the system using the INITIALIZE/RUN switch.

1.9.2 If the high-power mode is selected, then the "1KV, 6V ACTIVE" and "HI-PWR XMTR SEL" indicators should be lit. If the low-power mode is selected, neither of these should be lit. Re-initialize the system if necessary.

1.9.3 The ATCRBS INTERROGATIONS indicator flashes momentarily (.1 sec) when an ATCRBS interrogation is detected. The DABS INTERROGATIONS indicator is activated when a DABS interrogation is detected, and remains lit for approximately 16 seconds thereafter. No visual indication is given for ATCRBS/DABS or DABS-only All-Calls.

1.9.4 The "LOCKOUTS" indicators reflect the state of the CPME lockouts at all times. Indicator lit implies "locked out". When the ALL STATUS and LOCKOUT STATE switches are both in the ENABLE position, then the lockout state as indicated is transmitted in a Comm-B reply as follows (in response to a correctly addressed interrogation with RL=1 and MSRC=0001):

Bit 43: ATCRBS lockout state
Bit 44: ATCRBS/DABS All-Call lockout state
Bit 45: auxiliary (DABS-only) All-Call lockout state
Bit 46: auxiliary discrete address interrogation lockout state

1.9.5 Fault Bits

1.9.5.1 If a CPME fault exists, the LED marked "FAULT" will light up and so will the red "fault lamp" on the outside of the CPME enclosure. This main "fault bit" is a logical OR of the fault bits listed below. It is the state of this main fault bit which is transmitted as the FR bit in replies, as noted in paragraph 1.5.4.4. The fault lights are lit regardless of the state of the "Reporting to Sensor" switches.

1.9.5.2 Five LEDS (#1-#5) on the CPME Control Panel always display the state of the CPME fault detection system. If the "Reporting to Sensor: All Status" switch is in the ENABLE position, then the condition of these LEDS is transmitted in the Comm-B reply bits shown (see also paragraph 1.5.4.2) in response to a correctly addressed interrogation with RL=1 and MSRC=0001.

LED #	<u>Reply Bit</u>	Fault
1	38	Oscillator out of phase-lock.
2	39	Power fail/initialize (a 128 sec
		timer which is activated at powerup
		or when system is initialized).
3	40	Inside of enclosure under-temperature.
4	41	Inside of enclosure over-temperature.
5	42	Miscellaneous fault (a logical OR of
		the fault conditions described in
		paragraph 1.9.5.3).

1.9.5.3 Miscellaneous fault conditions are detected and displayed as follows (these bits are not individually transmitted in any replies):

LED #	Fault
6	Transmitter duty cycle exceeded.
7	Multiple turn-around delays selected.
8	Multiple reply types detected.
9	Multiple re _l ly modes requested (a transponder fault condition)
10	Turnaround delay state counter failure.
11	SMI state counter failure.
12	SPARE (unused).

1.10 Adjust AT1

If the high-power mode is selected, the CPME RF power output level is adjusted by attenuator AT1. To adjust this, monitor the replies by connecting an oscilloscope to the "OUTPUT MONITOR TO SCOPE" jack provided. Convert the peak voltage readings of the reply pulses to "dBm" readings by using the crystal calibration charts provided with each CPME. Add this power reading (in dBm) to the "bias value" (see calibration information for each CPME), which is about +38.5 dB, to obtain the actual RF output power at the CPME RF port. A calibration chart which converts the dial reading of AT1 into the attenuation value is also provided, so that relative power levels can be easily set.

1.11 Turn On Environmental System

Turn on the circuit breaker marked "HEAT/COOL". All five of the internal fans should run continuously.

1.12 Set PAM/PPM Switch

A screwdriver-adjust switch is located on the front of the transponder for the purpose of changing reply modulation formats. The CPME is shipped with the switch in the PPM position, and the control should normally remain in this position.

2.0 USE OF CPME DURING MONOPULSE ACCURACY TESTS

2.1 External Signal Source

A high-accuracy CW signal source, such as an HP8640B signal generator, is required.

2.2 Connecting the External Source

Connect the external source as follows:

2.2.1 If the power available from the signal generator is +20 dBm, then set it to this value. With the CPME power OFF, remove the "External XMTR Source Patch" semi-rigid coaxial jumper. Care must be taken in removing this jumper so as not to damage it. To remove, unscrew each side by one turn, then repeat (alternating sides) until jumper comes off. To replace it, a torque wrench is recommended. Attach the signal generator to the side of the patch input marked "XMTR Source Input". Terminate the patch jack marked "Internal Source Output" in a 50 ohm impedance. The CPME can now operate as before, in either high or low power mode, but with a variable frequency output. Set attenuator AT5 to zero dB if the high-power mode is used.

2.2.2 If the power available from the signal generator is only +10 dBm, then set it to this value. With the CPME power OFF, remove the flexible coaxial cable from pad AT3, leaving the other end of this cable attached to the tube amplifier unit. Attach the signal generator to the cable. The CPME can now operate as before, but only in the high-power mode.

2.3 Example of CPME Use for Calibration

Assume that a CPME is located 7000 feet from a sensor. A 200 foot cable (with 6 dB loss) is used between the CPME and the 14 dB gain horn antenna, giving an effective CPME antenna system gain of +8 dB. Also assume a sensor with a +28 dB gain antenna (ASR-7) and 5 dB elevation loss due to antenna beam shaping, thus giving an effective sensor antenna gain of +23 dB.

2.3.1 Link Calculation

An estimate of the power levels involved is made in the following example (see also section 3.5.6.1.3 of the DABS CPME Performance Specification). A maximum power input of -24 dBm is required at the sensor RF port (see FAA-ER-240-26, paragraph 4.5.4.3.1). We wish to know the RF power output at the CPME RF port needed to accomplish this. This is given by:

 $P_{out, CPME} = P_{in, sensor} + \underbrace{[97 + 20 \log (Range x Freq)]}_{FREE SPACE LOSS} - G_{HORN} - G_{ASR7}$

Substituting:

 $P_{out, CPME} = -24 \text{ dBm} + 97 + 20 \log \left[\left(\frac{7000}{5280} \right) (1.090) \right] - 8 - 23 = +45 \text{ dBm}.$

Thus a maximum power output of +45 dBm is required at the CPME RF port to produce a signal level of -24 dBm at the sensor RF input port, under the stated conditions. The minimum CPME power setting required is 40 dB less, or +5 dBm output at the CPME RF port.

2.3.2 CPME Use

Assume the conditions described in paragraph 2.3.1 still hold. Also assume that an HP8640B signal generator, which has +10 dBm output, is used. Connect this source as described in section 2.2.2, and turn the CPME on in high-power mode. To take the first set of readings, set the frequency of the generator to 1090 MHz and monitor replies on the CPME's "Output Monitor to Scope" (built-in crystal detector*). Adjust the high-power attenuator, AT1, until the power output at the CPME RF port is +35 dBm (which should result in a -24 dBm signal at the sensor). To determine the CPME RF port output from the crystal detector reading, first subtract the "Power Bias Value" (typically 38.5 dB) from the desired RF power output. In this example, a power level of +45 dBm - 38.5 dB = +6.5 dBm must occur at the crystal detector. Use the crystal calibration chart to convert this dBm reading to a voltage reading. For example, CPME #1 (which contains crystal #4 and AT1 serial #13) would be giving replies at a +45 dBm level if the peak voltage measured at the output monitor was 190 mV. (which corresponds to a +6.5 dBm signal to the crystal). The setting of AT1 should be about 5 dB at this point (which is a dial reading of 28 on the turnscounting dial of AT1). For further information, refer to the DABS CPME System Block Diagram.

Once the sensor is calibrated at this setting, change the HP8640B frequency +3 MHz, as specified in the test procedures. Now dial in 5 dB additional attenuation on AT1 and repeat (you can again monitor the RF power output on the crystal detector to make sure the level went down by 5 dB). Continue the procedure until the lowest required power setting has been reached, changing the frequency nine times at each of the nine power settings, for a total of 81 sensor runs.

Note: To use the built-in calibrated crystal detector, run a short BNC cable from the "Output Monitor to Scope" jack to a 1-Megohm scope input. Do not terminate the cable, as the detector is already terminated inside the CPME.

APPENDIX B

EXCEPTIONS AND CLARIFICATIONS TO CALIBRATION AND PERFORMANCE MONITOR EQUIPMENT (CPME) ENGINEERING REQUIREMENT, FAA-ER-240-29*

This Appendix provides a paragraph-by-paragraph listing of ways in which the Calibration and Performance Monitor Equipment described in this project report deviate from FAA Engineering Requirement FAA-ER-240-29*. Items are also included to clarify the intended meaning of a requirement or the manner in which the requirement was met in the MIT/Lincoln Laboratory CPME design.

Many of the listed deviations derive from the following agreed-upon ER exceptions upon which the design of the MIT/Lincoln Laboratory-provided CPMEs was based:

- (1) The LL CPME shall have no Comm-C/Comm-D capability, hence no ELM capability. Also, any reply bits which, when "true", indicate ELM capability shall be set "false".
- (2) The LL CPME shall not respond to Mode 2 interrogations.
- (3) The LL CPME shall have a high power mode.
- (4) Specification FAA-G-2100 shall be considered to be a design goal.

As amended by Amendment 1 and Specification Change 1 dated 20 May 1976.

Page	Para. No.	Reason for Change	Change
4	3.4.1	No ELM or Mode 2	In second sentence delete "plus military Mode 2 capability" and the word "full".
			In last sentence delete "and extended length uplink (Comm-C) and downlink (Comm-D) communications transactions.
4	3.4.2	No ELM or Mode 2	Delete sentence beginning "It shall also include the functional".
5	3.5.1.1	No ELM or Mode 2	Delete "Mode 2", in second line.
5	3.5.1.2	Clarification	In second sentence delete "or when inhibited by an ATCRBS/DABS All-Call lockout condition".
			Delete the third, fourth and fifth sentences and substitute:
			When locked out to ATCRBS/DABS All-Calls but not to ATCRBS interro- gations, the CPME shall respond to ATCRBS/DABS All-Calls with ATCRBS replies (Mode A or C appropriately, depending on the P ₁ - P ₃ spacing). The CPME shall not produce a DABS All-Call reply in response to a CW transmission or a single pulse of long duration whose received amplitude variations do not approximate an All-Call interrogation. The CPME shall not produce a DABS All-Call reply in response to P ₁ - P ₃ pair alone. In order to elicit an All-Call reply, the P ₁ - P ₃ transmission must be followed by a distinct P ₄ pulse. In particular, there shall be no All-Call reply to a "filled-in" P ₃ - P ₄ pulse, i.e., a long P ₃ pulse.
6	3.5.1.3	Clarification	Delete (c) and substitute:
			"(c) The interrogation content indicates that the interrogation is a DABS broadcast transmission (for which no reply is requested.)
6	3.5.1.3	Clarification	Delete (d) and reletter (e) to (d).

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Page	Para. No.	Reason for Change	Change
6	3.5.1.4	Revised and Reworded	Delete first sentence and substitute: "The CPME shall not reply to DABS uplink transmissions in which a sync phase reversal is not detected in the assigned interval, as specified in paragraph 2.4.5 of FAA-RD-74-62."
			In second sentence change "95 percent" to "90 percent".
7	3.5.1.8	Correction	In third line delete "(squitter)".
8	Table 3.5.2-1	Correction	In table caption change "DABS" to "ATCRBS/DABS".
8	3.5.2.2	Added require- ment	Add, after "as described in FAA-RD-74-62," Section 4.4.3.1, which is summarized in Table 3.5.2-2. The commands shown in the table are bits 3,4, and 5 of an uplink surveillance or Comm-A interro- gation. "X" indicates a "don't care" condition. Command Oll is unassigned. The IT bit (Bit 3) is 1 if the interrogation comes from a standard interrogator and 0 if the interrogation comes from an auxiliary interrogator. The lockout states are given as 1 = locked out, 0 = not locked out. "Standard" All-Calls are ATCRBS/DABS All-Calls. Auxiliary All-Calls are DABS-only All-Calls with IT=0. DABS-only All-Calls with IT=1 cannot be locked out. For example, if the CPME is locked out to Auxiliary All-Calls but not to standard All-Calls nor Auxiliary Discrete interrogations (lockout state 010), and an interrogation with bits 3, 4, and 5 equal to 1, 1, and 0, respectively (command 110 in the table), is received, the CPME becomes locked out to all subsequent Auxiliary Discrete and Auxiliary All-Call interrogations, but not to Standard All-Calls (lockout state 011).
9	-	Added require- ment	Add new Table 3.5.2-2 (and renumber existing Table) as attached.

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TABLE 3.5.2-2

DABS LOCKOUT STATE TRANSITION DIAGRAM

		AUX.	All-Ca All-Ca Discre			state after		()-
Lockout	000	001	010	011	100	101	110	111
State Prior AUX. Discrete To Interrogation AUX. All-Call STD. All-Call 0000	000 010 100		001	110	101			111
001	100	OXX		110		101		111
010	000 100		001 010	110		```	101	111
011	100			0XX 110				101 111
100	100			110	000 010 101		001	111
101	100			110		0XX 101		111
110	10 0			110	000		001 010 101	111
111	100			110				0XX 101 111
		DL4,	Bit 4	of Int of Int of Int	errog	ation		

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Page	Para. No.	Reason for Change	Change
10	3.5.5	Explanation of turn-around delay operations	In first sentence add after ATCRBS "and DABS". Add at end of paragraph: "When the additional delay of 128 or 256 microseconds is selected, the CPME shall be inactive for the selected delay time (except for asynchronous timers, e.g., lockout timers) and will not decode further interrogations until the delayed response has been given. This is in accord with paragraph 3.5.1.7 (Dead time)."
11	3.5.6.1	Requirement for low and high power modes added	Delete present paragraph 3.5.6.1 and substitute: <u>3.5.6.1 Power Output</u> The CPME shall operate in one or two modes: low power (+10 dBm maximum output at RF port) and high power (+45 dBm output at RF port). The high power/low power select switch shall be located on the CPME front panel.
			<u>3.5.6.1.1 Low Power Mode</u> When using the internal transmitter source or an external transmitter source (see 3.7.4) set at a fixed level of +16 dBm, the CPME power output in low power mode, measured at the CPME RF port shall be variable (continuously or in 1 -db steps) over a range of -47 dBm to +10 dBm. The power setting shall be accurate to within ± 2.0 dB for all settings and for all pulses of all replies. Note: when equipped with a single horn antenna, a CPME RF output of ± 10 dBm should be sufficient to produce a ± 50 dBm signal at the RF port of a sensor 2000 feet away (see 3.5.6.1.3.4).
			<u>3.5.6.1.2 High Power Mode</u> When using the internal transmitter source or an external transmitter source (see 3.7.4) set at a fixed level of +10 dBm, the CPME power output in high power mode, measured at the CPME RF port shall be variable (continuously or in 1 -dB steps) over a range of 0 dBm to +45 dBm. The power setting shall be accurate to within ± 2.0 dB for all settings and for all pulses of all replies. Note: when equipped with a single horn antenna, a CPME RF output of ± 45 dBm should be sufficient to produce a -50 dBm signal at the RF port of a sensor 20 miles away (see 3.5.6.1.3.4).

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Page	Para. No.	Reason for Change	Change
11	3.5.6.1	Change continued	3.5.6.1.3 Notes on CPME-to-Sensor Radio Link Calculations To determine the signal levels produced at a sensor RF port by a CPME, the following equations are used:
			$P_0 + G_1 - L + G_2 = P_i$, where
			P_0 is the power output from the CPME RF port
			${}^{ m G}_{1}$ is the gain of the CPME antenna system
			L is the free space loss
			G ₂ is the gain of the sensor's antenna system
			P_{i} is the resulting power at the sensor's RF port.
			<u>3.5.6.1.3.1</u> CPME Antenna System Gain The CPME uses a 14 dB gain horn antenna (see 3.7.2) and has a loss of 6 dB in the cable which connects the antenna to the CPME RF port (see 3.7.3), which results in $G_1 = +8$ dB.
			3.5.6.1.3.2 Free Space Loss
			$L = 97 + 20 \log (Range \times Freq)$, where
			L is the free space (no atmospheric attenuation) loss in dB.
			Range is the distance from the CPME to the sensor in statute miles.
			Freq is the operating frequency in GHz. The CPME uses a frequency of approx. 1 GHz (see 3.5.6.3).
			3.5.6.1.3.3 Sensor Antenna System For purposes of calculation, a sensor with a +28 dB gain antenna, 5 dB elevation loss due to antenna beam shaping, and 2 dB cable loss has been assumed, giving $G_2 = +21$ dB.

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Page	Para. No.	<u>Reason for Change</u>	Change
11	3.5.6.1	Change continued	<u>3.5.6.1.3.4 Graph.</u> The CPME-to-sensor link power budget is summarized in Figure 3.5.6-1. For example, if $P_0 = \pm 10$ dBm for the CPME, a level of -50 dBm is produced at the RF input port of a sensor which is .4 miles (2100 feet) away. Similarly, $P_0 = \pm 45$ dBm should give $P_1 = -50$ dBm for a range of 22 miles. Note that since reciprocity holds, the same graph can be used to determine the signal level produced by a sensor at the CPME RF port. For example, if $P_0 = 800$ watts = ± 59 dBm is the sensor output, a level of 0 dBm is produced at the RF port of a CPME located .35 miles (1800 feet) away.
11	3.5.6.1	Change continued	Add new Figure 3.5.6-1.
11	3.5.6.5	No ELM; changes to reflect required CPME capabilities	 3.5.6.5 CPME Transmitter Duty Cycle 3.5.6.5.1 Low Power Mode Within a single 30-ms period, corresponding to a typical interrogator antenna dwell time, the CPME shall be capable of transmitting a minimum of forty 112-bit replies, arbitrarily spaced in the 30-ms period, except that no more than twenty replies shall be required to be transmitted within any 4-ms sub-period. Overall variation in peak power output shall not exceed 1 dB from the first pulse of the first reply to the last pulse of the last reply within the 30 msec period. 3.5.6.5.2 High Power Mode Within a single 30-ms period, corresponding to a typical interrogator antenna dwell time, the CPME shall be capable of transmitting a minimum of sixty 56-bit replies or thirty 112-bit replies, equally spaced in the 30-ms period. Overall variation in peak power output shall not exceed 1 dB from the first reply to the
12	3.5.7.2	No ELM; reworded for clarity	last pulse of the last reply within the 30 msec period. Change parenthetical statement to read "(Surveillance, All-Call, and Comm-B)".

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Fig. 3.5.6-1. CPME output vs range for various sensor inputs

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Page	Para. No.	Reason for Change	Change
12	3.5.7.2.2	No ELM; reworded for clarity	Delete entire paragraph and substitute: <u>3.5.7.2.2 Extended Capability Code</u> In response to a correctly addressed interrogation with RL=1 and MSRC=0001, the CPME shall transmit a Comm-B reply with an MSRC code of 0001 in the leading four bit positions of the MB field and a zero in the first bit position of the extended capability field (bit position 37 of the Comm-B data field) to indicate lack of ELM capability.
12	3.5.7.2.3 3.5.7.2.4	To make room for added paragraphs	Renumber as paragraphs 3.5.7.2.4 and 3.5.7.2.5.
12	3.5.7.2.3	Added require- ment for status indication	<pre>Add new paragraph as follows: 3.5.7.2.3 CPME Status In response to a correctly addressed interrogation with RL=1 and MSRC=0001, the CPME shall transmit a Comm-B reply with bits 38 through 46 defined as follows: Bit 38: oscillator out of phase-lock. Bit 39: power fail (two minute timer which is activated</pre>
			completed). The four status bits indicating the state of the lockout latches shall all be set either to zeros or to reflect the proper lockout state (1 = locked out, 0 = not locked out) under control of a switch (lockout status switch). The five "fault bits" (38-42 above) shall be OR'ed together and this bit shall be transmitted as the FR bit (bit 19 of surveillance or

shall be transmitted as the FR bit (bit 19 of surveillance or Comm-B reply). This FR bit, and all the other status bits, shall be transmitted either as all zeros or as the CPME status dictates under control of a switch (Inhibit Status Switch).

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Page	Para. No.	Reason for Change	Change
13	3.5.7.2.5	Add explanatory information	Delete old paragraph 3.5.7.2.5 and substitute new paragraph renumbered 3.5.7.2.6.
			3.5.7.2.6 Alert and Flight Rule Bits Bit No. 6 (Alert) in downlink Surveillance and Comm-B transmission shall always be transmitted as a zero by the CPME. Bit No. 19 (Flight rule) in downlink surveillance and Comm-B transmissions shall be transmitted as defined in paragraph 3.5.7.2.3 (CPME status).
13	3.6	No ELM	In second line delete "and ELM".
14	3.6.2	No ELM	Delete entire paragraph.
14	3.6.3	-	Remember as 3.6.2.
14	3.7.1.1(c)	No Mode 2	Delete sub-paragraph.
14	3.7.1.1(d), (e), (f)	-	Renumber as (c), (d) and (e).
15	3.7.1.1(g)	Consistency with two output levels	Delete and substitute (f): "Controls for varying the transmitter output power (see 3.5.6.1)."
15	3.7.1.1(h), (i), (j)	-	Renumber as (g), (h) and (i).
15	3.7.1.1(k)	No switch is required	Renumber as (j) and change to read: "Transmitter source, (see 3.7.4)."
15	3.7.2	To reflect items actually required	In second line change <u>"+0.5</u> dB" to <u>"+1.0</u> dB". Add at end of paragraph: "A low-loss mylar radome and suitable mounting hardware for the horn shall also be provided."

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	16	3.7.4	To describe items required more fully	Delete paragraph and substitute: <u>3.7.4 Connectors and Adaptors</u> Sufficient cable connectors and adaptors shall be provided for connecting hte CPME to the horn antenna via the antenna cable. A port shall be provided for the insertion of an external CW signal to be used for test purposes in place of the internally generated transmitter carrier. The frequency of the external signal will be varied as part of the sensor monopulse accuracy tests specified in FAA-ER-240-26, paragraph 4.5.4.3. (The frequency of the external signal will be varied between 1087 and 1093 MHz. The power level of the external source shall be set at a fixed value of +10 dBm. The CPME peak RF power output can then be varied from +45 dBm to 0 dBm in the high power mode and from 0 dBm to -53 dBm in the low power mode). A coax "patch cord" shall be used on the front panel to switch between internal and external transmitter sources.
B-11	16	3.7.5	To describe items required more fully	Add at end of paragraph: "Suitable mounting hardware and a lock shall also be provided."
	16	3.7.7	To describe items required more fully	Add at end of paragraph: "A suitable power cord shall be provided."
	16	3.7.8	To reflect actual CPME design	Delete and substitute: <u>3.7.8 Environmental Service Conditions</u> The enclosed CPME shall be designed for outdoor operation in the continental U.S.
	17	3.7.10(d)	To add require- ment for warm-up period required in high-power mode.	In second line change "within 30 seconds" to "within one minute".
	17	3.7.11	Not applicable	Delete and substitute "Not applicable".

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