



# High Performance Embedded Computing Workshop

19 – 21 September 2006

## PRELIMINARY AGENDA

### 19 September

#### Auditorium

- 0730 **Check-in / Poster Setup / Continental Breakfast**
- 0830 **Welcome**  
Eric Evans / MIT Lincoln Laboratory
- 0835 **Keynote Address**  
Anita Jones / University of Virginia
- 0905 **Opening Remarks**  
Robert Bond / MIT Lincoln Laboratory
- 0915 **Session 1: Novel Hardware and Device Technologies**  
Richard Linderman / AFRL
- 0925 **Invited**  
William Dally / Stanford University
- 0955 **Invited**  
Craig Keast / MIT Lincoln Laboratory
- 1025 **Break (View Posters)**

#### Auditorium

- 1040 **MONARCH: A First Generation Polymorphic Computing Processor**  
Michael Vahey / Raytheon  
Lloyd Lewins / Raytheon  
Drew Davidoff / Raytheon  
Gillian Groves / Raytheon  
Kenneth Prager / Raytheon  
Charles Channell / Raytheon  
Matt Kramer / Raytheon  
John Granacki / University of Southern California-ISI  
Jeff Draper / University of Southern California-ISI  
Jeff LaCoss / University of Southern California-ISI  
Craig Steele / Exogi  
Jim Kulp / Mercury Computer Systems, Inc.
- 1110 **Probabilistic CMOS Technology for Cognitive Information Processing**  
Krishna Palem / Georgia Institute of Technology  
Bilge Akgul / Georgia Institute of Technology  
Lakshmi Chakrapani / Georgia Institute of Technology

#### Room S2-180

- 1040 **Focus 1: FPGA/ASIC Systems Technologies**  
David Cousins / BBN
- 1050 **Exploiting Reconfigurability for Text Search**  
Roger Chamberlain / Exegy & Washington University  
Mark Franklin / Exegy & Washington University  
Ronald Indeck / Exegy & Washington University
- 1120 **Heterogeneous Processing Element Support for VSIPL++**  
Miriam Leeser / Northeastern University  
Albert Conti / Northeastern University  
Nicholas Moore / Northeastern University  
Laurie Smith King / College of the Holy Cross
- 1150 **RFIC Beamforming for Agile, Low-Cost Overlapped Subarrays**  
Sean Duffy / MIT Lincoln Laboratory  
Daniel Santiago / MIT Lincoln Laboratory  
Christopher Olson / MIT Lincoln Laboratory  
Jeffrey Herd / MIT Lincoln Laboratory
- 1235 **Lunch (View Posters)**

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## PRELIMINARY AGENDA

### 19 September (*Continued*)

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#### Auditorium

- 1140 **Poster Précis A: Advanced Algorithms and Hardware**  
Rich Linderman / AFRL
- 1150 **Poster Précis A**
- Poster A.1 Nonlinear Equalization of RF Receivers**  
Benjamin Miller / MIT Lincoln Laboratory  
Brandon Kam / MIT Lincoln Laboratory  
Joel Goodman / MIT Lincoln Laboratory  
Gil Raz / GMR Research and Technology, Inc.
- Poster A.2 Parallelizing Exact Inference in Bayesian Networks**  
Viktor Prasanna / USC  
Vasanth Krishna Namasivayam / USC
- Poster A.3 Discrete Fourier Transform Compiler for FPGA and CPU/FPGA Partitioned Implementations**  
Markus Püschel / Carnegie Mellon University  
Paolo D'Alberto / Carnegie Mellon University  
Peter Milder / Carnegie Mellon University  
Franz Franchetti / Carnegie Mellon University  
James Hoe / Carnegie Mellon University  
José Moura / Carnegie Mellon University
- Poster A.4 Benchmark Results for Ultra-High Performance Scalable Processing Architecture for Embedded Defense Signal and Image Processing Applications**  
Stewart Reddaway / WorldScape  
Nigel Bond / WorldScape  
Rick Pancoast / Lockheed Martin  
Justin Kidman / WorldScape  
Pete Rogina / WorldScape
- Poster A.5 Petascale Computing in a Cubic Meter by 2015**  
James C. Anderson / MIT Lincoln Laboratory
- 1235 **Lunch (View Posters)**

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#### Posters on View at Burlington Marriott

- Poster A.6 (Marriott) Taking the HPEC Challenge with VSIPL++**  
Jules Bergmann / CodeSourcery  
Don McCoy / CodeSourcery  
Stefan Seefeld / CodeSourcery  
Mark Mitchell / CodeSourcery
- Poster A.7 (Marriott) HPCS Scalable Synthetic Compact Application #3 Reference Implementation**  
Brian Sroka / The MITRE Corporation
- Poster A.8 (Marriott) Runtime Verification of Cognitive Applications**  
Jonathan Springer / Reservoir Laboratories  
Donald Nguyen / Reservoir Laboratories  
Richard Lethin / Reservoir Laboratories
- Poster A.9 (Marriott) Implementations of FIR for MONARCH Processor**  
Jinwoo Suh / University of Southern California–Information Sciences Institute  
Janice McMahon / University of Southern California–Information Sciences Institute

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## PRELIMINARY AGENDA

### 19 September (Continued)

Auditorium	Room S2-180
1345 <b>Session 2: Applications on New Architectures</b> Jeremy Kepner / MIT Lincoln Laboratory	1345 <b>Focus 2: Intelligent Software Technologies</b> Robert Bond / MIT Lincoln Laboratory
1355 <b>Successive Rank-Revealing Cholesky Factorizations on GPUs</b> Xiaobai Sun / Duke University Ty Fridrich / Duke University Nikos Pitsianis / Duke University	1355 <b>SAT Solvers for Investigation of Architectures for Cognitive Information Processing</b> Rich Lethin / Reservoir Laboratories James Ezick / Reservoir Laboratories Samuel Luckenbill / Reservoir Laboratories Donald Nguyen / Reservoir Laboratories Peter Szilagyi / Reservoir Laboratories
1425 <b>Field Programmable Multi-Cores: A New Class of Semiconductors</b> Gail Walters / CPU Technologies Edward King / CPU Technologies	1425 <b>Automatic Mapping of the HPEC Challenge Benchmarks</b> Nadya Bliss / MIT Lincoln Laboratory Jason Dahlstrom / MIT Lincoln Laboratory Daniel Jennings / MIT Lincoln Laboratory Sanjeev Mohindra / MIT Lincoln Laboratory
1455 <b>Using VSIP as an Embedded DoD Application Programming Interface (API) on DARPA Polymorphous Computing Architectures (PCA)</b> Kristin Daly / Lockheed Martin Joseph Cook / Lockheed Martin Rick Pancoast / Lockheed Martin Steve Crago / University of Southern California-ISI Matthew French / University of Southern California-ISI Karandeep Singh / University of Southern California-ISI Jinwoo Suh / University of Southern California-ISI	1455 <b>Program Analysis Tools for Application Specific Architectures</b> Maya Gokhale / Los Alamos National Laboratory Matt Sottile / Los Alamos National Laboratory
1525 <b>Break (View Posters)</b>	1525 <b>Break (View Posters)</b>
1540 <b>Travel to Marriott</b>	

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## PRELIMINARY AGENDA

### 19 September (*Continued*) at Burlington Marriott

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#### Session 2: Applications on New Architectures

Jeremy Kepner / MIT Lincoln Laboratory

- 1630 **The Past, Present, and Future of High Performance Embedded Computing in Reconnaissance Applications**  
James Broesch / General Atomics
- 1700 **Advanced VLSI for Sensor Array Signal Processing**  
William Song / MIT Lincoln Laboratory
- 1730 **2005 Awards**  
Jeremy Kepner / MIT Lincoln Laboratory
- 1740 **Reception**
- 1840 **Banquet Speaker (Title TBA)**  
Rodney Brooks / MIT CSAIL
- 1910 **Banquet**

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### Posters on View at Burlington Marriott

#### Poster Demonstration: Advanced Algorithms and Hardware

Rich Linderman / AFRL

- Poster A.6 (Marriott)** **Taking the HPEC Challenge with VSIPL++**  
Jules Bergmann / CodeSourcery  
Don McCoy / CodeSourcery  
Stefan Seefeld / CodeSourcery  
Mark Mitchell / CodeSourcery
- Poster A.7 (Marriott)** **HPCS Scalable Synthetic Compact Application #3 Reference Implementation**  
Brian Sroka / The MITRE Corporation
- Poster A.8 (Marriott)** **Runtime Verification of Cognitive Applications**  
Jonathan Springer / Reservoir Laboratories  
Donald Nguyen / Reservoir Laboratories  
Richard Lethin / Reservoir Laboratories
- Poster A.9 (Marriott)** **Implementations of FIR for MONARCH Processor**  
Jinwoo Suh / University of Southern California–Information Sciences Institute  
Janice McMahon / University of Southern California–Information Sciences Institute



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## PRELIMINARY AGENDA

### 20 September

#### Auditorium

- 0730 **Check-in / Poster Setup / Continental Breakfast**
- 0830 **Announcements**  
Robert Bond / MIT Lincoln Laboratory
- 0835 **Keynote Address – HPEC: Looking Back, Projecting Forward**  
David Martinez / MIT Lincoln Laboratory
- 0905 

**Session 3: Challenging Computing Environments**  
Rick Pancoast / Lockheed Martin
- 0915 **Invited**  
Charles Holland / DARPA/IPTO
- 0945 **Leveraging Carbon Nanotube to Develop a Fourth-Generation Radiation Hardened Microprocessor for Space**  
Rick Ridgley / NRO
- 1015 **Break (View Posters)**

#### Auditorium

- 1030 **Invited**  
Col Stephen "Scotty" Fairbairn / SIAP
- 1100 **Dependable Multiprocessing (DM)**  
John Samson, Jr. / Honeywell  
Gary Gardner / Honeywell  
David Lupia / Honeywell  
Alan George / University of Florida  
Minesh Patel / Tandel Systems, Inc.  
Paul Davis / Tandel Systems, Inc.  
Vikas Aggarwal / Tandel Systems, Inc.  
Zbigniew Kalbarczyk / University of Illinois  
Raphael Some / Jet Propulsion Laboratory

#### Room S2-180

- 1030 

**Focus 3: High Performance Systems**  
David Cousins / BBN
- 1040 **Real-Time Adaptive Signal Processing Development for US Navy Torpedoes**  
Matthew Alexander / MIT Lincoln Laboratory  
James C. Anderson / MIT Lincoln Laboratory  
Nigel Lee / MIT Lincoln Laboratory  
Francine Rayson / MIT Lincoln Laboratory  
William Payne / MIT Lincoln Laboratory
- 1110 **Impact of CMP Design on High-Performance Embedded Computing**  
Patrick Crowley / Washington University  
Mark Franklin / Washington University  
Jeremy Buhler / Washington University  
Roger Chamberlain / Washington University
- 1140 **Break (View Posters)**
- 1155 **Filesystems for Embedded Stream-Oriented Applications**  
Bradley Kuszmaul / MIT CSAIL
- 1235 **Lunch (View Posters)**

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## PRELIMINARY AGENDA

### 20 September (Continued)

#### Auditorium

- 1130 **Poster Précis B: High Performance FPGA Technologies and Applications**  
Rick Pancoast / Lockheed Martin
- 1140 **Poster Précis B**
- Poster B.1** **Experimental Analysis of Multi-FPGA Architectures over RapidIO for Space-Based Radar Processing**  
Chris Conger / University of Florida  
David Bueno / University of Florida  
Alan George / University of Florida
- Poster B.2** **Radar Digital Beam-Former Utilizing FPGA Based COTS Processors**  
John Fontana / Lockheed Martin  
Edward Monastra / Lockheed Martin
- Poster B.3** **An FPGA-Based Dynamic Load-Balancing Processor Architecture for Solving N-body Problems**  
Jonathan Phillips / Utah State University  
Matthew Arenó / Utah State University  
Brandon Eames / Utah State University  
Aravind Dasu / Utah State University
- Poster B.4** **Hybrid Floating Point Technique Yields 1.2 Gigasample per Second 32 to 2048 point Floating Point FFT in a Single FPGA**  
Raymond Andracka / Andracka Consulting Group
- Poster B.5** **FPGA Technology Meets the Multicomputer Environment – Improving Processing Performance and Bandwidth in Advanced Naval Radar Missions**  
Sarah Leeper / Mercury Computer Systems, Inc.  
Mike Iaquinto / Lockheed Martin  
Richard Brooks / Mercury Computer Systems, Inc.  
Joseph Finnivan / Mercury Computer Systems, Inc.
- Poster B.6** **Design of Path Optimization Algorithm Using COTS Field Programmable Gate Array Hardware and Software Platforms**  
Neil Harold / Nallatech  
John Ostapovich / Nallatech  
Rick Pancoast / Lockheed Martin  
Jon Russo / Lockheed Martin
- Poster B.7** **Multi-FPGA Based High Performance LU Decomposition**  
Arvind Sudarsanam / Utah State University  
Seth Young / Utah State University  
Thomas Hauser / Utah State University  
Aravind Dasu / Utah State University
- Poster B.8** **Improving the Performance of Parallel Backprojection on a Reconfigurable Supercomputer**  
Benjamin Cordes / Northeastern University  
Miriam Leeser / Northeastern University  
Eric Miller / Northeastern University  
Richard Linderman / AFRL
- Poster B.9** **A New Class of High Performance FFTs**  
Greg Nash / Centar
- Poster B.10** **Running Simulink-Based Designs on SRC-6**  
David Meixner / National Center for Supercomputing Applications at Univ. of Illinois–Urbana-Champaign  
Volodymyr Kindratenko / National Center for Supercomputing Applications at Univ. of Illinois–Urbana-Champaign  
David Pointer / National Center for Supercomputing Applications at Univ. of Illinois–Urbana-Champaign
- Poster B.11** **High Performance Low Density Parity Check and Turbo Decoding FPGA Implementation**  
Ryan Shoup / MIT Lincoln Laboratory
- Poster B.12** **Close-to-Concept Coding for Configurable Computing**  
Henk Spaanenburg / Advanced Principles Group  
Joe Thompson / Advanced Principles Group
- 1235 **Lunch (View Posters)**

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### 20 September (Continued)

Auditorium	Room S2-180
1335 <b>Session 4: Cognitive Computing</b> William Harrod / DARPA / IPTO	1335 <b>Focus 4: High Performance Rapid Prototyping</b> Albert Reuther / MIT Lincoln Laboratory
1345 <b>CEARCH: Cognition Enabled Architecture</b> Stephen Crago / University of Southern California–ISI Janice McMahon / University of Southern California–ISI	1345 <b>HPEC Challenge SAR Benchmark pMatlab Implementation and Performance</b> Julia Mullen / MIT Lincoln Laboratory Theresa Meuse / MIT Lincoln Laboratory Jeremy Kepner / MIT Lincoln Laboratory
1415 <b>R-Stream: A Parametric High Level Compiler</b> Eric Schweitz / Reservoir Laboratories Rich Lethin / Reservoir Laboratories Allen Leung / Reservoir Laboratories Benoit Meister / Reservoir Laboratories	1415 <b>Applying Advanced Computing to Improve High-Fidelity Radar Data Simulations</b> Christopher Hulbert / Information Systems Laboratory Jameson Bergin / Information Systems Laboratory Paul Techau / Information Systems Laboratory
1445 <b>COGENT: An Innovative Architecture for Cognitive Processing</b> Julius Bogdanowicz / Raytheon John Granacki / University of Southern California–ISI	1445 <b>Interactive Supercomputing's Star-P Platform: Parallel MATLAB and MPI Homework Classroom Study on High Level Language Productivity</b> Alan Edelman / MIT & Interactive Supercomputing Parry Husbands / Interactive Supercomputing & Lawrence Berkeley National Laboratory Steve Leibman / Interactive Supercomputing
1515 <b>Break (View Posters)</b>	1515 <b>Break (View Posters)</b>
1540 <b>Panel: Looking Forward, Looking Back</b> Moderator: James C. Anderson / MIT Lincoln Laboratory Distinguished Panelists: Jerry Oosterheld / SimVentions, Inc. Stephen Poole / Los Alamos National Laboratory Richard Ridgley / National Reconnaissance Office Gary Shaw / MIT Lincoln Laboratory	
1730 <b>Adjourn</b>	



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### 21 September

#### Auditorium

- 0730 **Check-in / Poster Setup / Continental Breakfast**
- 0830 **Announcements**  
Robert Bond / MIT Lincoln Laboratory
- 0835 **Session 5: Standards and Metrics**  
Craig Lund / Mercury Computer Systems
- 0850 **HPC Challenge**  
Jeremy Kepner / MIT Lincoln Laboratory
- 0920 **Performance Complexity: A New Execution Time Metric**  
Erich Strohmaier / Lawrence Berkeley National Laboratory
- 0955 **Keynote Address**  
Robert Kahn / Corporation for National Research Initiatives
- 1025 **Break (View Posters)**

#### Auditorium

- 1040 **The HPEC Challenge Benchmark Suite**  
Ryan Haney / MIT Lincoln Laboratory  
Theresa Meuse / MIT Lincoln Laboratory  
Jeremy Kepner / MIT Lincoln Laboratory
- 1055 **Data Reorganization Interface (DRI): Past Perspective, Future Vision, New Results, and Increased Availability**  
Kenneth Cain, Jr. / Mercury Computer Systems, Inc.
- 1110 **VITA-49: Digital Intermediate Frequency (IF) Interface Standardizing Data Flow for Tomorrow's Embedded Systems**  
Dean Holman / Mercury Computer Systems, Inc.

#### Room S2-180

- 1040 **Focus 5: Harnessing the Cell Processor**  
Sharon Sacco / MIT Lincoln Laboratory
- 1050 **Performance Benchmarks and Programmability of the IBM/Sony/Toshiba Cell Broadband Engine Processor**  
Luke Cico / Mercury Computer Systems, Inc.  
Robert Cooper / Mercury Computer Systems, Inc.  
Jon Greene / Mercury Computer Systems, Inc.  
Michael Pepe / Mercury Computer Systems, Inc.
- 1120 **Leveraging Multicomputer Frameworks for Use in Multi-Core Processors**  
Yael Steinsaltz / Mercury Computer Systems, Inc.  
Scott Geaghan / Mercury Computer Systems, Inc.  
Myra Jean Prella / Mercury Computer Systems, Inc.  
Brian Bouzas / Mercury Computer Systems, Inc.
- 1150 **Speech Recognition on Cell Broadband Engine**  
Holger Jones / Lawrence Livermore National Laboratory  
Michael Perrone / IBM Watson Research Center  
\* Yang Liu / Lawrence Livermore National Laboratory

\* Denotes presenter other than first author.



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## PRELIMINARY AGENDA

### 21 September (Continued)

#### Auditorium

- 1115 **Poster Précis C: Software Standards**  
Craig Lund / Mercury Computer Systems
- 1125 **Poster Précis C**
- Poster C.1 Computational Requirements of a Non-combinatorial Detection of Multiple Targets in High GMTI Clutter**  
Simon Streltsov / LongShortWay, Inc.  
Ilya Muchnik / LongShortWay, Inc.  
Sergey Petrov / LongShortWay, Inc.  
Leonid Perlovsky / AFRL  
Ross Deming / Anteon Corporation
- Poster C.2 Extending the VSIPL Standard to Other Precisions: Gaining the Full Performance of Current Processors**  
Albert Garrett / Verari Systems  
Anthony Skjellum / Verari Systems
- Poster C.3 A Comparison of VSIPL++ Performance to VSIPL and Mercury SAL**  
Thomas Steck / Lockheed Martin
- Poster C.4 Reusing Verification Components in System-Level Modeling Environments**  
Ambar Sarkar / Paradigm Works  
Jim Crocker / Paradigm Works  
Bob Ionta / The MathWorks, Inc.
- Poster C.5 Abstract Machines for RASCs and Signal/Image Processing**  
Lenore Mullin / College of Computing and Information at SUNY–Albany  
James Reynolds / College of Nanoscale Science and Engineering at SUNY–Albany  
Ian Grout / University of Limerick  
Qiang Li / College of Computing and Information at SUNY–Albany  
Jeffrey Ryan / University of Limerick
- Poster C.6 The Measure Polytope: Rapid Context Switching within a Universal Network Architecture**  
Kurt Keville / MIT  
Dan Vickery / MIT
- Poster C.7 DIFdoc: A Standard Format for Visualizing Hierarchical Dataflow Representations**  
Ivan Corretjer / University of Maryland  
Shuvra Bhattacharyya / University of Maryland
- Poster C.8 The Impact of Programming Difficulty on Hardware Obsolescence**  
James Steed / Gedae  
William Lundgren / Gedae  
Kerry Barnes / Gedae
- Poster C.9 X-Sim: A Federated Heterogeneous Simulation Environment**  
Roger Chamberlain / Washington University  
Saurabh Gayen / Washington University  
Eric Tyson / Washington University  
Mark Franklin / Washington University  
Patrick Crowley / Washington University
- Poster C.10 System Overhead Management with Virtual Power Centers for Biometric Applications**  
Kevin Howard / Massively Parallel Technologies  
James Lupo / Massively Parallel Technologies
- Poster C.11 Modeling Concurrency in NOC for Embedded Systems**  
Ankur Agarwal / Florida Atlantic University  
Ravi Shankar / Florida Atlantic University
- Poster C.12 Algorithm Development for Future High Performance Systems**  
**Jigsaw: An Early Case Study**  
Imran Khan / SoftServ International
- Poster C.13 Software Decomposition for Multicore Architectures**  
Ankit Jain / Florida Atlantic University  
Ravi Shankar / Florida Atlantic University
- 1220 **Lunch (View Posters)**

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## PRELIMINARY AGENDA

### 21 September (*Continued*)

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#### Auditorium

- 1330 **Session 6: Awards Session**  
Jeremy Kepner / MIT Lincoln Laboratory
- 1340 **Invited**  
Jerry Oesterheld / SimVentions, Inc.
- ★1410 **VSIPL++ Acceleration Using Commodity Graphics Processors**  
Daniel Campbell / Georgia Institute of Technology
- ★1440 **Enabling Cognitive Architectures for UAV Mission Planning**  
Jon Russo / Lockheed Martin  
Mohammed Amduka / Lockheed Martin  
Keith Pedersen / Lockheed Martin  
Richard Lethin / Reservoir Laboratories  
Jonathan Springer / Reservoir Laboratories  
Rajit Manohar / Cornell University  
Rami Melhem / University of Pittsburgh
- 1510 **Break (View Posters)**
- ★1535 **Spaceborne Processor Array in Multifunctional Structure (SPAMS)**  
Edward Chow / Jet Propulsion Laboratory  
Don Schatzel / Jet Propulsion Laboratory  
Bill Whitaker / Jet Propulsion Laboratory  
Thomas Sterling / Louisiana State University
- ★1605 **Exploring the Cell with HPEC Challenge Benchmarks**  
Sharon Sacco / MIT Lincoln Laboratory  
Glenn Schrader / MIT Lincoln Laboratory  
Jeremy Kepner / MIT Lincoln Laboratory
- 1635 **Invited**  
Andre van Tilborg / Office of the Secretary of Defense
- 1700 **Adjourn / Awards**  
Jeremy Kepner / MIT Lincoln Laboratory