High Performance Embedded Computing Workshop 2000

PRELIMINARY AGENDA
20 – 22 September 2000

20 September

0730 **Check-In & Continental Breakfast**

AUDITORIUM

0830 **Welcome**
David Briggs (MIT Lincoln Laboratory)
0835 **Keynote Address**
Charles Holland (DDR&E)
0905 **Opening Remarks**
Robert Bond/Jeremy Kepner (MIT Lincoln Laboratory)

0915 **Session 1: Enabling Hardware Technologies**
Michael Lucas (Northrop Grumman ESSD)

0925 **Applying Reconfigurable Hardware to Segmentation for Multispectral Imagery**
Miriam Leeser (Northeastern University)

0955 **Break**

1010 **Parallel C Programming of Reconfigurable Computers: The Streams-C Approach**
Maya Gokhale (Los Alamos National Laboratory)

1040 **Implementing QR-Decomposition on the Imagine Stream Processor**
Brian Towles (Stanford University)

1110 **A 225 Billion Operations Per Second Polyphase Channelizer Processor Chip-Set for Wideband Channelized Adaptive Sensor Array Signal Processing**
William Song (MIT Lincoln Laboratory)

1140 **Poster Session A: Advanced Hardware Systems**
Michael Vai (MIT Lincoln Laboratory)

Poster Session A Précis

Poster A.1
An Economical 40 MHz Universal Software Radio Using a Hybrid Approach
Joseph Arrowood (Los Alamos National Laboratory)

Poster A.2
Task-Level Energy Minimization for Reconfigurable Embedded Systems
Hakan Aydin (University of Pittsburgh)

Poster A.3
Implementation and Optimization of a Distributed Memory FFT Processor
Robert Johnson (MathStar, Inc.)

Poster A.4
A FPGA Implementation of an Adaptive Reconfigurable Image Encoder
Sarin Mathen (ITTC)

Poster A.5
SCALIP: Scalable IP for Systolic Applications
Matthew Moe (Carnegie Mellon University)

Poster A.6
Reconfigurable Video Processor
Scott Morris (Raytheon Electronic Systems)

Poster A.7
A Processor-In-Memory (PIM) Computing Architecture for Critical Navy Phased Array Radar Applications
Stephen Shank (Lockheed Martin)

Poster A.8
A Dynamically Reconfigurable Vision (DRV) System
David Stack (Comptek Amherst Systems, Inc.)

Poster A.9
A Hybrid FPGA/DSP/GPP Prototype Architecture for SAR and STAP
Jack West (University of Oklahoma)

1220 **Lunch**

1305 **Session 2: High Performance Interconnects**
Robert Hoenig (SKY Computers, Inc.)

1315 **Performance Evaluation of Opto-Electronic Interconnects for High-Performance Computing**
Janice McMahon (MIT Lincoln Laboratory)

1345 **A Low-Cost 10 Gb/s Optical Link for Embedded Computing Applications**
Warren Rosen (Drexel University)

1415 **Fairness Issues in an Embedded Photonic Ring Interconnect**
Abhijit Mahajan (Washington University)

1445 **Distributed Corner Turn on a PIM-Based Multiprocessor**
Jinwoo Suh (University of Southern California)

1515 **Break**

1530 **Session 3: Special Session: Software Standards and Their Application**
Richard Games (The MITRE Corporation)

1540 **The Vector, Signal, and Image Processing Library (VSIPL): Emerging Implementations and Further Development**
Randall Janka (Georgia Tech Research Institute)

1550 **Putting Messaging Middleware in Perspective**
Anthony Skjellum (MPI Software Technology, Inc.)

1600 **Data Reorganization and Future Embedded HPC Middleware**
Kenneth Cain (The MITRE Corporation)

1610 **High Performance CORBA**
James Kulp (Mercury Computer Systems, Inc.)

1620 **Implementing VSIPL Using Intelligent Compiler Technology**
Steve Paavola (SKY Computers, Inc.)

1640 **APIs, Benchmarking & Power of Abstraction**
Arkady Kanevsky (Mercury Computer Systems, Inc.)

1700 **A Parallel Algorithm for Matched Field Processing Using MPI and VSIPL**
Randall Judd (SPAWAR SYSCEN San Diego)

1720 **COTS Software Portability Standards and VSIPL Benchmarks**
Roelan Teachey (Lockheed Martin)

1740 **Adjourn**

1745 **Reception**

1830 **Banquet Speaker**
Quantum Computing
Colin Williams (Jet Propulsion Laboratory)

1900 **Banquet**

21 September

0730 **Check-In & Continental Breakfast**

AUDITORIUM

0830 **Announcements**
Robert Bond (MIT Lincoln Laboratory)

0835 **Invited Speaker**
Blue Gene System Overview
Marc Snir (IBM/Waston)

0905 **Session 4: Advanced Software Technologies**
Eric Pancoast (Lockheed Martin)

0915 **Environment for Implementing DSP Algorithms in Reconfigurable Hardware**
Eric Pauer (Sanders, A Lockheed Martin Company)

0945 **Automated Empirical Optimizations of Software and the ATLAS Project**
Antoine Petitet (University of Tennessee)

1015 **Achieving Portable Task and Data Parallelism on Signal Processing Architectures**
Hank Hoffman (MIT Lincoln Laboratory)

1045 **Break**

1100 **SPIRAL: Automatic Implementation of Signal Processing Algorithms**
Jose Moura (Carnegie Mellon University)

1130 **Poster Session B: Middleware and Tools for Embedded Computing**
Larry Bergman (Jet Propulsion Laboratory/NASA)

Poster Session B Précis

Poster B.1
Joint STARS Airborne Ground Surveillance HPC Technology Development Initiatives
Marc Campbell (Northrop Grumman Corporation)

Poster B.2
Towards Real-Time Adaptive QoS Management in Middleware for Embedded Computing Systems
Christopher Gill (Washington University)

Poster B.3
Digital Radio Design Using GEDAE
Richard Jaffe (L-3 Communications Systems East)

Poster B.4
Integration of VSIPL and OpenMP into a Parallel Image Processing Environment
Jeremy Kepner (MIT Lincoln Laboratory)

Poster B.5
Design Flow for Automatic Mapping of Graphical Programming Applications to Adaptive Computing Systems
Sze-Wei Ong (University of Tennessee)

Poster B.6
Autocoding Toolset - Automating Parallel Code Generation from Graphical Design Specifications
Christopher Robbins (MCCI)

Poster B.7
C++ Expression Templates in an Embedded, Parallel, Real-Time Signal Processing Library
Edward Rutledge (MIT Lincoln Laboratory)

Poster B.8
Model Based Parallel Programming with Profile-Guided Application Optimization
Jeffrey Smith (Mercury Computer Systems, Inc.)

Poster B.9
Advanced Radar Signal Processing on General-Purpose Commercial Multiprocessor Systems
Thomas Steck (Johns Hopkins University)

1210 **Lunch**

1255 **Session 5: Embedded System Applications**
Dennis Braunreiter (Raytheon Missiles Systems)

1305 **An Embedded Reconfigurable Computing Architecture Upgrade for a Legacy Radar Countermeasures Processor**
Eric Pancoast (Lockheed Martin)

1335 **An Open Architecture for Next Generation Space Onboard Processing**
David Ngo (Sanders, A Lockheed Martin Company)

1405 **Audio & Speech Processing Algorithms on Embedded Hardware: Custom vs. COTS Hardware & Software**
Douglas Smith (Air Force Research Laboratory)

1435 **Break**

1450 **Supercomputing Onboard the Next Generation Space Telescope**
Maria Nieto-Santisteba (Space Telescope Science Institute)

1520 **Analysis of Computational System Performance in Automatic Target Recognition**
Joseph O'Sullivan (Washington University)

1550 **Panel Session: Starved for Data: Programmability, Reconfigurability, and The Memory Hierarchy.**
Panel Moderator: Richard Linderman (Air Force Research Laboratory)

1710 **Adjourn**

22 September

0730 **Check-In & Continental Breakfast**

AUDITORIUM

0830 **Announcements**
Robert Bond (MIT Lincoln Laboratory)

0835 **Invited Speaker**
High Performance Interconnects: Riding the Standards Wave
Richard Lacerte (Nortel Networks)

0905 **Session 6: New Frontiers: Applications and Technologies**
Daniel Katz (Jet Propulsion Laboratory/Caltech)

0915 **EDDDDI: Error Detection by Diverse Data and Duplicated Instructions**
Nahmsuk Oh (Stanford University)

0945 **High Availability/Fault Tolerant Signal Processor Architecture for Navy Theater Wide Radar Applications**
Rathin Putatunda (Lockheed Martin)

1015 **Dynamic Workload Re-Distribution for Fault Recovery in Embedded Systems**
James Lebak (MIT Lincoln Laboratory)

1045 **Break**

1100 **Linux Lessons**
Craig Lund (Mercury Computer Systems, Inc.)

1130 **Real-Time Processing Challenges of Hyperspectral Sensing**
Gary Shaw (MIT Lincoln Laboratory)

1200 **Closing Remarks**
Robert Bond (MIT Lincoln Laboratory)

1210 **Lunch**

1255 **Adjourn**