The TILE-Gx Processor:
Enabling HPC through Massive-Scale Manycore

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Abstract

Tilera is a fabless processor company, developing low power, high performance manycore processors since 2004. The company has become known for leading the industry in the number of processor cores instantiated on a single silicon die. In 2007, the company launched its first generation TILE64 processor with 64-cores. A year later, the TILE*Pro* family was released, improving performance by 1.5x and incorporating a number of new features and adding a 36-core device to the product line. These processors have generated strong interest and adoption in the DoD and academic fields for HPC and data mining applications.

In 2011, Tilera is delivering its 3rd generation Tile Processor, the TILE-Gx series. This 64-bit processor family features devices ranging from 16 cores up to 100 cores and is implemented in 40nm process technology for low power and very high compute density.

A wide range of integer HPC applications can benefit from the parallel compute offered on these processors. Networking-centric applications such as Deep Packet Inspection (DPI), data search/correlation, and network flow monitoring can scale close to linearly across many dozens of cores.

In this presentation, we will present an overview of this new class of multicore processors and provide examples of specific computing applications that benefit from the TILE-Gx architecture

TILE-Gx Processor Features

The TILE-Gx processors are highly integrated System-on-Chip (SoC) devices with on-board memory controllers and I/O ports.

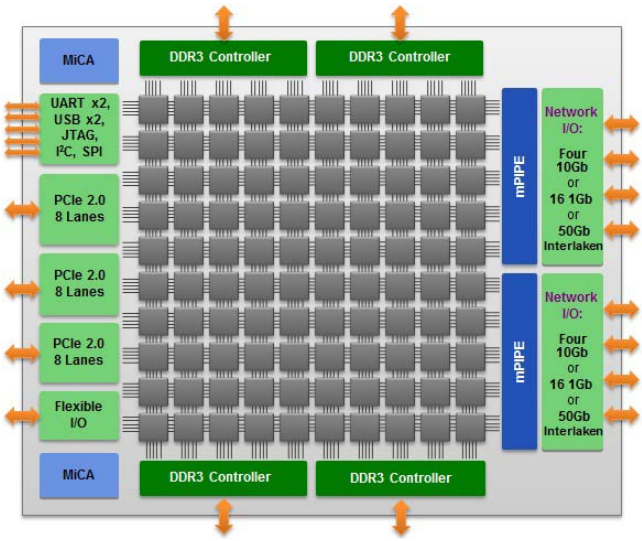

Figure 1: TILE-Gx100 manycore processor.

Specifically, the TILE-Gx100 device includes the following on-chip features:

- Four 72-bit DDR3 memory controllers with ECC at speeds up to 2133MTps
- Eight 10Gb Ethernet ports, or 32 1Gb ports
- Two 50Gb Interlaken packet I/O ports
- Three 8-lane Gen 2 PCI Express ports
- Two USB ports, RS-232 and other low speed I/Os

The aggregate peak performance of the Gx100 is 450 BOPS at a clock frequency of 1.5GHz. With the SIMD capabilities in each core, the Gx100 can deliver 600GMACs per second for DSP computation. Each of the 100 cores is enabled with 32KB L1 instruction cache, 32KB L1 data cache and 256KB L2 unified cache. The L2 caches are coherent across the device, providing an L3 cache of 25.6Mbytes available to all tiles. The peak bandwidth of the mesh interconnect is 200Tbps.

HPC Applications

As general-purpose processors, the TILE-Gx devices can be targeted for a wide range of applications, including cloud computing "farms" for shared access and large scale algorithms. Hadoop and other implementations of the Map/Reduce paradigm align well with the Tile multicore architecture and provide a standard framework for distributed computing.

Example applications that will be discussed include Network packet inspection, flow monitoring, regular-expression pattern search, and other data harvesting techniques. In addition, DSP and audio/video media processing applications will be reviewed.

Platform Deployment

As the TILE-Gx processors become generally available in 2H 2011, a number of hardware platforms will be shipping to enable the DoD and academic institutions to employ these manycore processors.

- PCI Express cards with one to four TILE-Gx chips
- 1U & 2U servers with up to 400 cores (4 Gx100s)
- ATCA, AMC, VPX and other industry-standard blade formats

The availability of these hardware platforms will enable rapid deployment of massive core-count arrays for demanding and compute-intensive applications.