COTS Based High Performance Radar and EW Development Platform

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Introduction

The tremendous development in the computing area has brought many applications such as radar, sonar and electronic warfare (EW) from almost impossible to implement to the point where multiple COTS solutions exists. Today we are at a point where many previously challenging applications can be implemented almost completely defined by software. Furthermore the same computing hardware can be used to implement very different systems. In the same manner, new technology enables low power implementations as well as rapid application development using software defined development and retargeting to appropriate hardware at deployment.

We predict that going forward there will be a multitude of new applications being enabled by commercial developments such as autonomous vehicles, gaming and entertainment that will give us smaller, ultra low cost solutions to our challenges. The defense space will still be pushing the envelope of high end systems, but we will be using repackaged commercial hardware for many of our applications. The computing market is also going to become more specialized with time. The improvement in performance will mainly not come from increase in clock speed but from the use of parallel computing structures.

There will be the X86 compatible high power general purpose multi-core PC processors that maximize usability and performance to very low cost, then there will be the GPU processors with high parallelism and great performance for specific algorithms, the FPGA with or without CPU that provides high data rate processing and hardware like performance, and the new generation of specialized array architectures [1] that provides ultra low power high floating point performance.

For many deployed applications the best solution is not a single architecture, but a combination. The right choice will depend on the desired application properties such as size, weight, power, development time, cost, length of series etc.

In this paper and poster we will demonstrate the use of a Radar and EW Development Platform that is all COTS based.

Challenges in Radar and EW algorithm development

Apart from the challenges in bringing the signal to and from the analog domain, one common obstacle in the development of algorithms for Radar and EW processing is the high rate streamed data. For pulsed radars some of the data may be thrown away by gating in time. But for instance in the search for Low Probability of Intercept (LPI) signals all the data must be processed in order to find the interesting signals. Also, in the development phase it is good to be able to run different algorithms on the same data in order to compare the methods. Ideally one would, during the first development stage, like to continuously store the sample data.

On the other hand continuous storage of all data from the high speed ADC:s can only go on for a couple of hours using state-of-the art 19” rack sized data-loggers of today. And the processing time, even using GPU and/or FPGA acceleration, might even be longer for each tested algorithm. The key is to find the right balance between raw data storage and parallel processing to reduce the data rate and extract the interesting features, occasionally storing interesting raw data for further analysis and algorithm development.

The ability to stream data into a PC also allows for the usage of GP-GPU in algorithm development. This is expected to lower the development cost compared to a FPGA firmware development flow. Some applications, such as a Digital Receiver (DRx) with waterfall presentation of the spectrum, are expected to be demonstrated directly on such a development platform using the GPU both for computation and graphical presentation. For other applications where the latency is important, such as radar jamming applications, the GPU is only a development tool. Due to latency restrictions, such an application will always run in a FPGA environment.

Dependent on the type of algorithm, it is not obvious that the introduction of a GP-GPU will give speed-up. For many radar processing algorithms data transfer may well consume much of the GPU speed-up [1,2]. It is thus important to have the right way to transfer data. In the below presented development platform data is transferred from the transceiver board to the PC and onwards to the GPU using a Direct Memory Access (DMA). Thereby the latency is reduced and synchronization issues introduced by the data transfers are easier handled. The PC multi-core processor is used mainly to perform data storage to disk and system management.

High performance Radar and EW development platform

The development platform combines a high-speed RF transceiver (HRFT) board with tightly coupled ADC, FPGA and DAC with a streaming data system equipped with a NVidia GP-GPU. This platform is very well suited for exploring different partitions between the FPGA and GP-GPU domain as well as developing and evaluating real-time complex Radar and EW algorithms.

Disclaimers and footnotes.

Fig 1 Streaming data system (19" 4U 17"D) together with a 16 TByte disc pack. Several form factors and level of ruggedness are available (half rack, helicopter version).

The streaming data system in fig 1 using off the shelf components with highly tuned software is used to perform I/Q sample data storage at 1100 Ms/s (or 1 GHz analog bandwidth). The ADC can run up to 3000 Ms/s and with a firmware upgrade it is expected that the total storage rate will increase I/Q sample rate to 2200 Ms/s, or a blazing 4.4 GB/s.

Fig 2 Streaming data system with 96TByte (4x24Tbyte) disk-packs cabable of 4.4Gbyte/s continuous record (8Gbyte/s bursts) or playback.

The system support a multitude of IO interfaces such as Ethernet, Infiniband, 10GBitE, Camera Link, GigEVision, CAN, LIN, USB and custom interfaces such as direct DMA over PCIe. There is support for rugged environment (-20ºC – +50ºC, shock, vibration) and high altitude operation, all with off the shelf components and custom encapsulation.

The HRFT module in fig 3 has two high-speed ADC:s, DAC:s and a Xilinx Virtex-6 FPGA. Analog signals may be connected single-ended by using board edge mounted SMA connectors, or differentially using top mount SMP connectors. The latter allow for a separate high quality front-end board to for up- and/or downconversion of the radar signals. The module handles frequencies up to 3 GHz directly by undersampling. The DAC:s also has built-in mix- and Return-To-Zero (RZ) mode for undersampling applications.

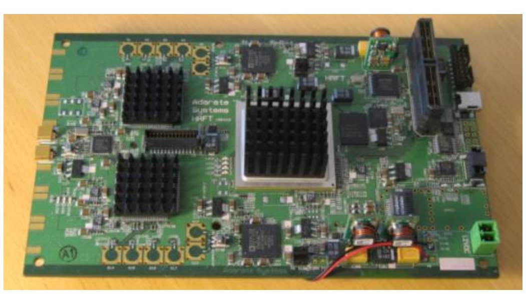

Fig 3 High-Speed RF Transceiver board (HRFT)

The HRFT module may by itself be used in a number of applications such as Broadband communication, Radar systems, Electronic Warfare, Digital RF Memory (DRFM), Arbitrary Waveform Generation (AWG), Direct Digital Synthesis (DDS) and Test Instrumentation. It is a versatile component to have in an EW Development System.

Fig 4 High-Speed RF Transceiver with PCI-express interface

After the development is finalized, the PCIe interface board in fig 4 may be unplugged for embedded applications. The board may then be fitted into a standard single (10x16 cm) eurocard rack.

Platform Demonstration

During the demonstration it will be shown that it is possible to stream data to disc while simultaneously processing typical receiver functions such as waterfall presentation on the GPU.

The signal environment, a combination of fix-frequency, pulsed radar and LPI signals is simulated as base-band RF signals using the HRFT Digital to Analog converters. This signal is the digitized and stored presented just as an ordinary base-band signal. To avoid unintentional signal interference the demonstration will be performed in cables.

The proposed demonstration contains no classified parts.

Conclusions

A versatile EW development platform has been presented. It has been shown that it is eg possible with COTS to do raw AD data streaming to a PC at sampling speed rates, while simultaneously processing typical receiver functions such as waterfall presentation on the GPU.

References

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