



# COTS Based High Performance Radar and EW Development Platform

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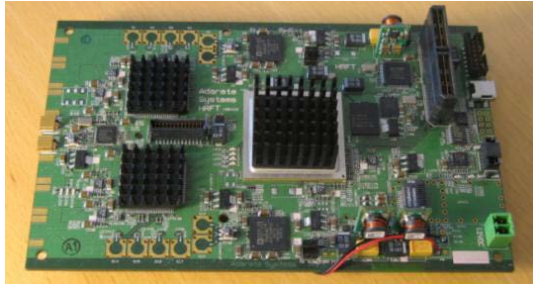
Gunnar Hillerstrom, Swedish Defence Research Agency



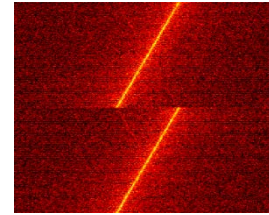
# COTS EW/Radar Development Platform

## Adarate

FPGA Front end & analog interface (ADC/DAC)

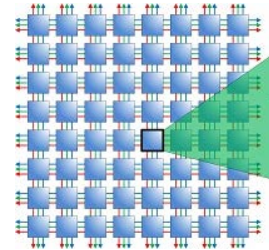


- Virtex6 130LXT – 475SXT
- 2x National ADC083000 (selectable)
- 2x Analog devices AD9739
- 2x 1Gbit Ethernet
- PCI-express



## NVIDIA

Floating point DSP & HMI  
- GPGPU GTX590



## Adapteva (future)

Complex CPU/DSP  
intensive processing  
- ATDSP (future) / Others

## Data Storage and Control



## XCube

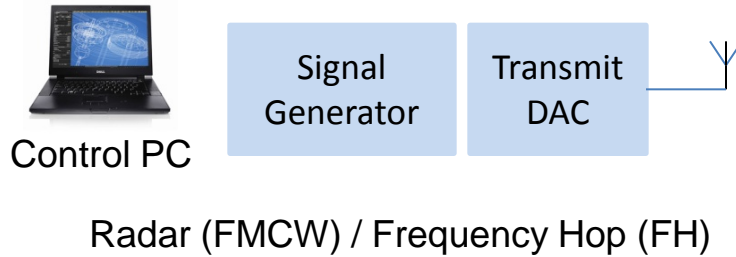
Development Platform

- Control / Record / Replay Software
- Dual Xeon CPU
- Up to 144GByte Memory
- >4.4GByte/s Throughput
- >8 GByte/s Burst
- 96TB removable storage (shown)



# Demo Setup (LPI Radar Simulation & Detection)

## HRFT Standalone



## Host Processing

2.4Gps - 8 bit data  
8 Channels 150MHz (I/Q-data)  
Window FFT waterfall  
1200MByte/s throughput (and storage)

## External Interfaces

## Buffering and Processing

## Disk Manager

