TDM Photonic Interconnection Network Using CMOS-Compatible Multilayer Integration

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***Abstract*—Communication bandwidth requirements among computing cores on a chip and to off-chip memory is quickly becoming a limiting factor in scaling performance at reasonable power budgets, especially in embedded systems. However, simulations have shown that silicon photonics could alleviate many of the limitations chip designers are faced with, including high IO pin counts and high speed signaling challenges. In this work, we present the design of a TDM-arbitrated photonic network using deposited materials instead of crystalline silicon, enabling lower loss, lower crosstalk, lower energy, and higher scalability than comparable designs.**

I. Introduction

High performance computing is approaching limitations that make performance scaling extremely difficult. Some of the same fundamental challenges are plaguing computing from extreme scale to embedded systems, namely interconnect design from increased parallelism, limited IO bandwidth from constrained pin count, and getting the most performance out of constrained power budgets.

Silicon photonics has shown through system simulation to be a superior communication medium than convention electronics for many reasons. Photonics can achieve a bandwidth density orders of magnitude higher than electronics using wavelength division multiplexing (WDM), a technique of transmitting many optical signals on different wavelengths in parallel simultaneously in a single transmission line. In addition, unlike electronics, the energy dissipated for optical signal propagation through waveguides and switches is independent of the datarate.

Numerous advances in silicon photonic integration and the emerging field of CMOS photonics [1], [2] allows us to consider practical designs of full-scale interconnects using this technology platform. Many such novel photonic-enabled network architectures have been recently proposed that can deliver performance improvement over equivalent electronic interconnect designs [3]–[5]. However, these designs make aggressive or even unrealistic assumptions about the abilities and scale of integration of photonic devices for the 15-year time frame.

Recently, using CMOS-compatible deposited materials such as silicon nitride and polysilicon to create photonic devices has become of interest [6], [7]. These photonic structures can be deposited directly on top of conventional CMOS logic, alleviating much of the post-fabrication costs that would have come with integrating a separate pure crystalline silicon substrate. Also, one added benefit is that silicon nitride exhibits lower loss than crystalline silicon in the telecom wavelength range, down to about 0.1 dB/cm [8]. Furthermore, since multiple layers of material can be deposited on top of each other, network topologies can be constructed to eliminate waveguide crossings, a large contributor to loss for some architectures [9].

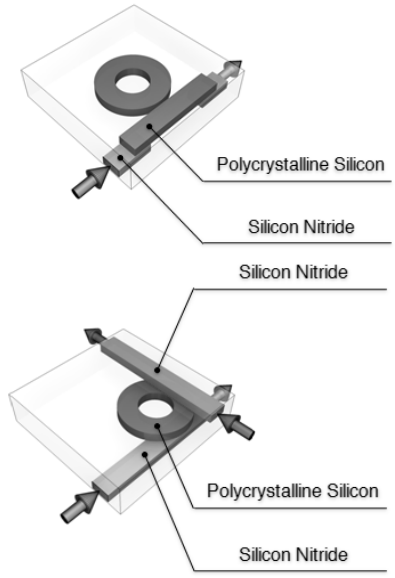

Fig. 1. **Arrangement of silicon nitride and polysilicon for making multi-layer ring resonators.**

However, silicon nitride is not electrically active, which is needed to change the refractive index of the material of a ring resonator to perform modulation and switching by changing the resonant wavelength of the device. Therefore, thermally-annealed polysilicon can be used for these purposes. Multiple layers of silicon nitride can be used for traveling longer distances, and evanescently couple vertically to polysilicon for active regions. This regime can be seen in Figure 1.

In this work, we explore the implementation of an existing TDM-arbitrated network design [10], [11] using deposited materials intead of crystalline silicon. Through analysis and simulation, we measure instertion loss, which affects both scalability and power dissipation, and crosstalk, which affects performance. Because the design is simple, effective, and targets CMOS-compatible deposition on top of a convention processor, this work is aimed at a design that is feasible within the next 15 years.

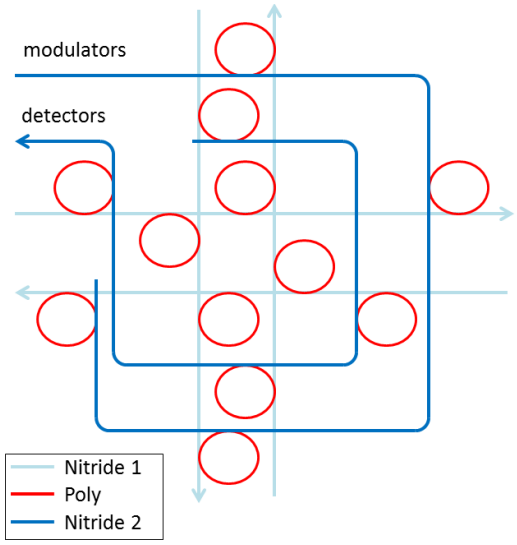

Fig. 2. **Layout of photonic switc tile, showing waveguides and ring resonators.**

II. TDM Network Design

The TDM network design we consider in this work is a good candidate for high performance embedded applications, which has been shown in previous work [11], because it achieves higher network bandwidth by providing a fairness mechanism through statically scheduled time slots. Furthermore, by scanning in the control registers, the network can be reconfigured to implement the specific communication patterns for a given application, thus optimizing the performance and power.

Figure 2 shows the switch tile necessary for a mesh topology using three layers of deposited materials: one polysilicon layer sandwiched between two silicon nitride layers. Besides the manufacturing benefit of deposited materials being able to be placed directly on top of CMOS logic, the network design is also conducive to first-generation photonic networks because it is a regularly tiled layout, easing design, fabrication, and test.

III. Evaluation

One of the most important characterizations of a photonic interconnection system is the insertion loss profile. The measure of worst-case insertion loss allows us to determine (1) the number of wavelengths that the network can support in parallel (if any), or the width of the links and/or (2) the amount of laser power needed to reliably traverse the network and reach the detectors.

For ring resonators, the insertion loss experienced when either passing by or dropping through the device is dependent on the radius of the ring. For this reason, we plot the total network insertion loss versus ring radius in Figure 3. The deposited-material (multi-layer) implementation of the network clearly exhibits lower loss with the elimination of most waveguide crossings. Also, an important mark on this graph is the insertion loss which corresponds to an optical power that a modulator cannot support, and therefore a network that is infeasible. Further analysis of this work will include

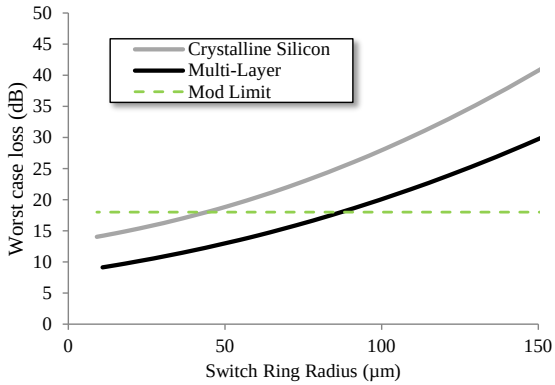

Fig. 3. **Comparison of insertion loss between crystalline silicon and multi-layer implementations.**

simulation that will yeild network-level crosstalk as well as power consumption.

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