Supercomputing with Embedded Efficiency: Electronic Warfare

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Energy Efficiency and Electronic Warfare

The power-wall problem is well known in modern processors, which imposes a fixed upper limit on power budgets due to thermal and battery issues, but evidence for an energy efficiency limit is also arising that caps the number of operations that can be computed within this power budget. This energy efficiency limit would greatly impact radar, imaging, and electronic warfare capabilities.

We present detailed analysis of the current state of the industry. First, the definition of an operation (op) was carefully selected based on typical electronic warfare algorithms and all data was normalized to a 32-bit fixed point multiply accumulate operation. In modern processors a limit of 7 million multiply accumulates per second per milliWatt (MMACs/mW) results. Further results show only a 5% increase in MMACs/mW over the last several technology nodes. Reasons behind this trend are discussed.

An analysis of electronic warfare systems is also presented that show how system capabilities would change under such a limit. Finally several suggestions and solutions are discussed.

An Energy Efficiency Asymptote

Figure 1 shows the results of an energy efficiency survey of processors that was done including processors as far back as the 1970's as well as processors sold commercially, presented by research labs, and presented by academia up through March, 2011.
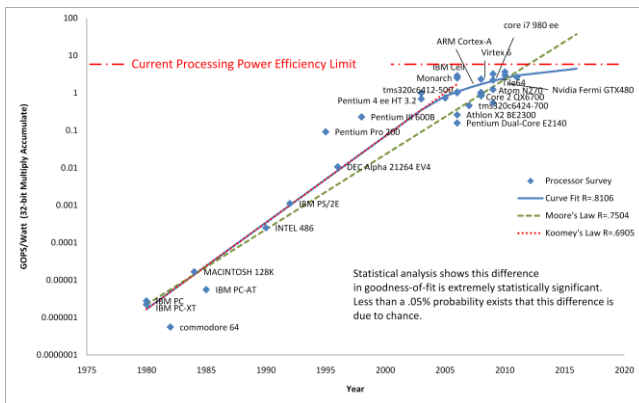

Figure 1: Processor survey showing an energy efficiency asymptote

A statistical analysis was done rating the curve fits of Koomey's Law, which has predicted a better than Moore improvement energy efficiency over the last 40 years, a Moore's law type curve which predicts a doubling of energy efficiency ever 2 years, and a quadratic curve fit showing an asymptote forming. The asymptotic curve fit was the best fit with a less than 0.05% probability that the

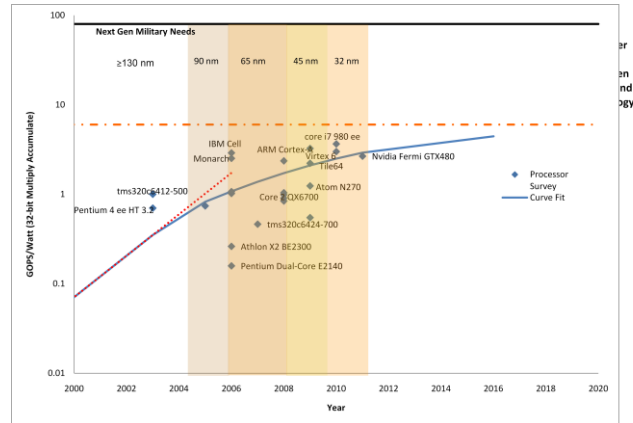difference is due to chance, making these results extremely statistically significant.

Figure 2. Efficiency by process node

As Figure 2 shows, the change from the Koomey's Law trend is very much related to the device physics at sub-100nm node, these will be addressed. Also shown here is the current gap between the reality and the need. The need will be discussed in more detail as well.

The Dataflow paradigm

Much of determining the energy efficiency for a system relies on defining what that system will be doing. The dataflow systems studied here have several key differences from the typical Von Neumann systems, such as workstations and servers, that have been the dominant form of computing.

We define a dataflow system in several key ways: almost all data consumed by the dataflow system is sensory input data as opposed to data being loaded from memory. Second, this sensory data must be processed in real time, and the effectiveness of the system is directly dependent on how much data can be processed in real time, hence a greater importance is placed on filtering and computing the data quickly as opposed to storing it for later use. Third, mathematical signal processing dominates the types of computations being done -- specifically the multiply accumulate (MAC) operation. Finally, the opportunity for parallel thread computing is limited because the incoming data is largely treated as a single stream, limiting the use of multi-core processors.

It is in this context that the analysis shown in Figure 1 and Figure 2, causes, and possible solutions will be discussed.

References

[1] J. Koomey, S. Berard, M. Sanchez, and H. Wong. "Assessing trends in the Electrical Efficiency of Computation over time", *IEEE Annals of the History of Computing*, 2009.