On Chip Nonlinear Digital Compensation for RF Receiver

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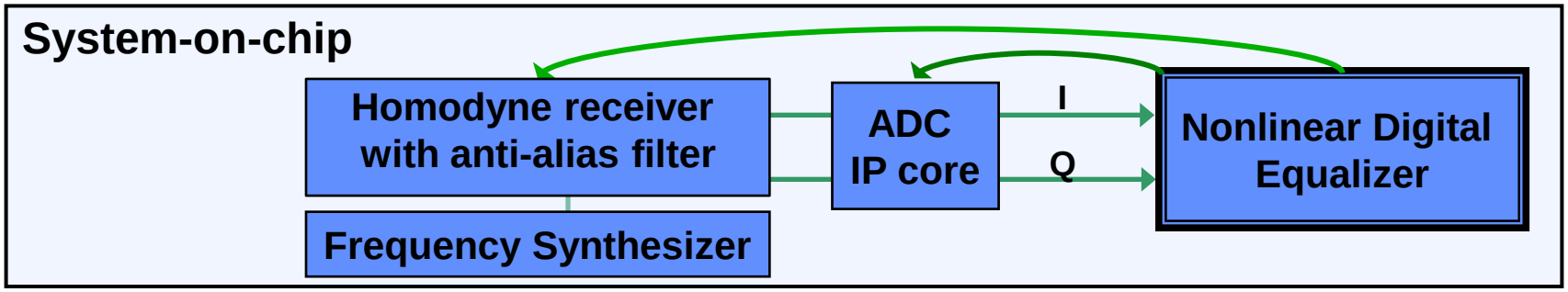
System On Chip Equalization



- We designed a nonlinear digital compensation circuitry that is part of a System On Chip (SOC) design
- SOC implementations are an attractive solution for SWaP restricted applications, partly because of targeted design needs
- We exploit the benefits of SOC implementations by ***co-designing*** the analog hardware and digital processing

Previous Work:

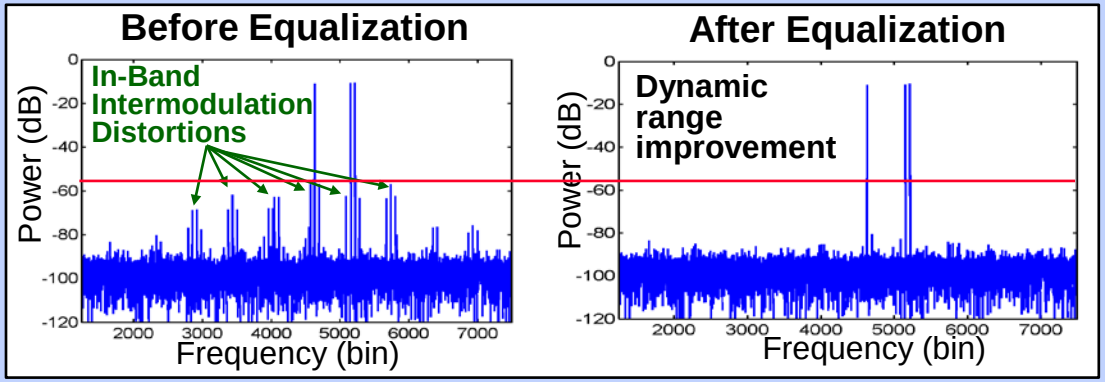
NLEQ Processor

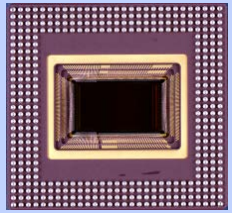
+20~25 dB SFDR/IFDR

@500MHz BW

>1 Teraops

< 2 Watts

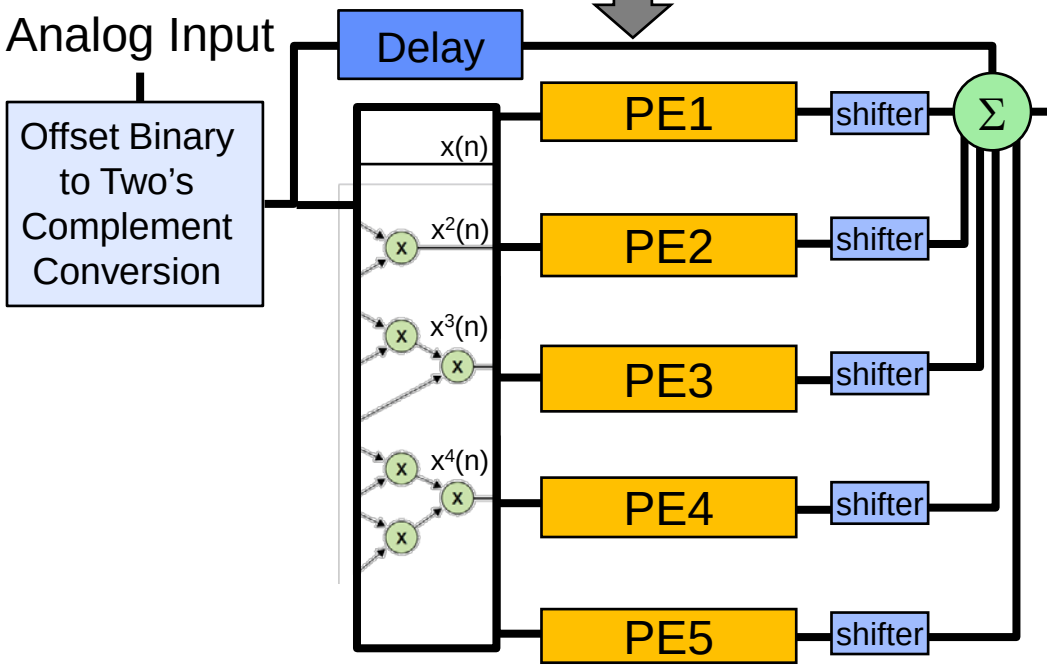


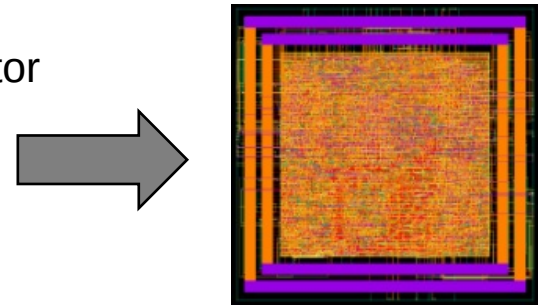


Song et al., "Nonlinear Equalization Processor IC for Wideband Receivers and Sensors," HPEC 2009

Nonlinear Digital Equalizer Design

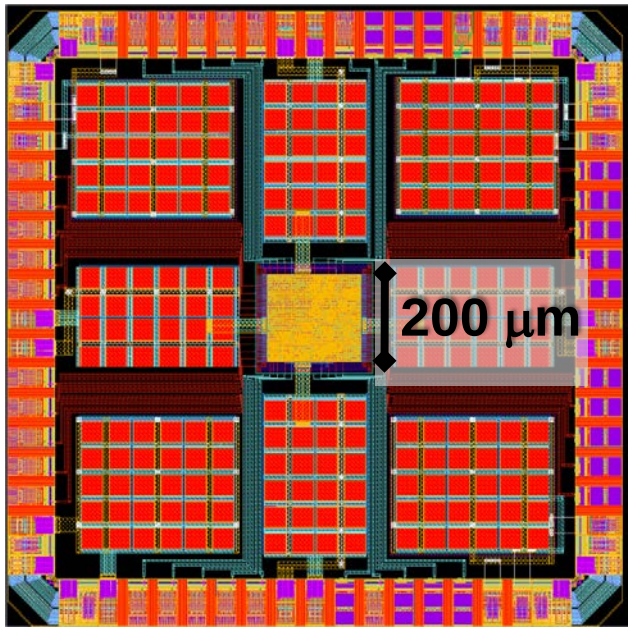
$$y(n) = x(n) + \sum_{i=1}^{5} x(n - m_{1,i}) x^{p_i}(n - m_{2,i}) h_i$$

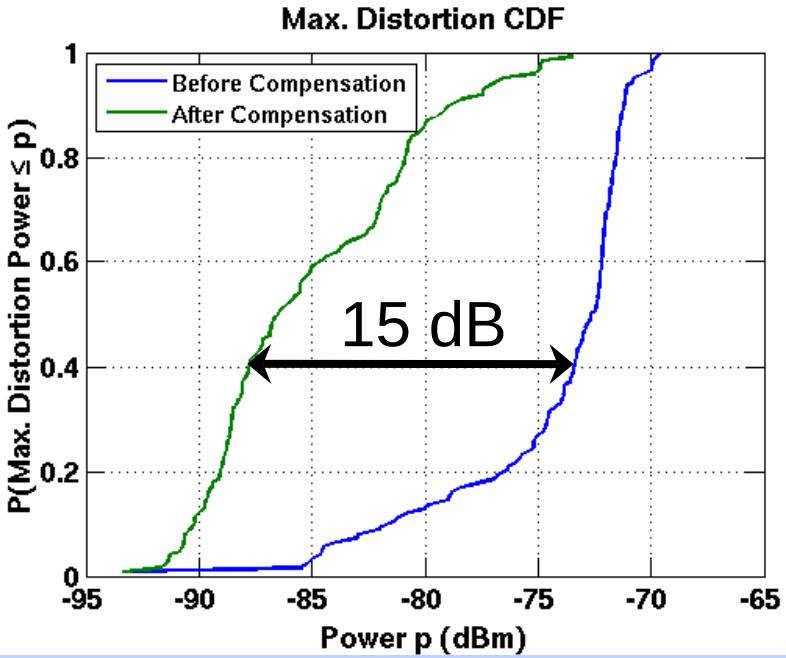




- **Established a low-power standard-cell synthesis design flow**
  - **IBM 65 nm CMOS process**
- **Created an overall compensation architecture customized for our current front end system**
  - **Design is optimized to minimize power consumption**

Projected Design Performance





- **The digital compensation architecture has been synthesized, placed, routed and taped-out**
  - **Core size: 200 μm by 200 μm**
  - **Simulation results show:**
    - **Approximately 10 mW of power at 200 MHz**
    - **Compensation of front end filter:**
      - **15 dB improvement for median dynamic range**