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Implementation of Digital Front End Processing Algorithms with Portability Across Multiple Processing Platforms

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A Process for Implementing Algorithms Across Hardware Platforms





2) Establish Trade Space

Critical system requirements Limitations on implementation 4) Final Architectural Selection

Can use this process with any algorithm and implementation

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Example: Digital Beamforming



- Digital Beamforming
 - Architecture elements: time delays, phase shifts, synchronization
 - Key Parameters: number of channels, number of beams, signal bandwidth, data bandwidth
- Hardware Implementation Options
 - Devices: ASIC, FPGA, multi-core processors, GPUs
 - Boards:
 - COTS
 - Custom

Hardware Platform Capabilities and Limitations



Medium

Medium

Low

High

High

Low

Lowest

Medium

Each implementation option offers a unique set of capabilities and limitations

None

High

Highest

Lowest

Medium

Medium

Medium

High

I/O Flexibility

Processing Efficiency

Programmability

Capability

Complexity

NRE Cost

Power

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Example Architecture: FPGAs on a Custom Board

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- System Requirements
 - Process multiple channels
- Algorithm Requirements
 - Over 100 Giga-operations/second
- Trade Space Restrictions
 - Radiation-tolerant FPGAs

- Data Dependencies
 - None between sub-bands
 - Significant dependencies between beams
- Candidate Architectures
 - Minimize number of devices
 - Increase number of subbands in a given device



Architecture achieves a balance between capability, flexibility, and cost

- COTS Modular Processor
 - Open system architecture using off-the-shelf hardware.
- COTS and Advanced Processors
 - Highly programmable

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An adaptable design process allows algorithm portability across platforms

Results: Beamforming Architectures for Land, Air, Sea, and Space

- Full Custom ASICs and Custom Board
 - Minimizes power, maximizes performance
- FPGA and Custom Board
 - Minimizes the number of FPGAs
 - Maximizes resource use



Full Custom Digital Beamformer



COTS Modular Processor Beamformer

