Modular, Scalable Computing for Systems with Tight SWaP Constraints

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Abstract

Size, Weight, and Power (SWaP) are important considerations in system design, but SWaP is especially critical in airborne platforms where all three parameters are at a premium. The design challenge is increasing with the proliferation of small, unmanned airborne platforms. This paper describes an out-of-the-box architectural approach, developed under a program sponsored by the Missile Defense Agency (MDA), enabling modular, scalable embedded processing solutions capable of meeting tight SWaP budgets.

Introduction

Meeting the SWaP challenges of airborne platforms suggests a need for heterogeneous computing so the engineer can optimize the system design. General purpose processors, graphics processors, FPGAs, and ASICs all represent a different balance of computing horsepower, efficient power consumption, and programmability, and having these technologies available allows the designer to choose the right tool(s) for the job. Heterogeneous approaches also imply a need for modularity and scalability. Such approaches have traditionally used backplanes which add weight, size, and cost to the overall system and constrain incremental scalability. A truly SWaP-optimized backplane-centric solution should have no empty slots. However, zero available slots means the system cannot incrementally scale to address fluid requirements. A solution would then require an additional backplane, or the replacement of the existing backplane, neither of which are SWaP-friendly.

MDA funded an SBIR Phase I and II to define an architecture and develop technology addressing the challenges of modularity, scalability, and heterogeneity in SWaP-constrained environments. The program was named RARE (Reconfigurable Advanced Rapid-prototyping Environment) and executed by Colorado Engineering Inc. under the technical guidance and influence of NRL, NSWC, and ONR.

Modularity and Scalability with no Backplane

RARE provides a modular, scalable heterogeneous computing architecture facilitating high performance embedded computing in strict cost, size, weight, and power budgets. This award-winning technology is currently being used across multiple RF sensor designs spanning a variety of missions including ground imaging, collision avoidance, and target acquisition.

RARE defines an open-systems, "out-of-the-box" approach to embedded processing architectures by decomposing a system into functional building blocks of commercial-off-the-shelf (COTS) hardware. The blocks provide a modular way to achieve loosely coupled common operational subsystem components that, when tied together using well defined interfaces form a complete scalable processing and control system. Processing systems targeted for platforms ranging from small UAVs to large manned aircraft can be realized using these same building blocks. RARE modules are based upon state-of-the-art general purpose processors, FPGAs, A/Ds, D/As, and standard I/O fabrics to facilitate high performance embedded computing system design and heterogeneous implementation.

Modules are 6.25" by 6.25" square cards (Figure 1) that have multiple parallel and serial high speed I/O connections in all three dimensions (x, y, and z; Figure 2). This allows integrators to stack and/or tile the building blocks to simultaneously address processing load, I/O bandwidth, and physical installation footprint. For example, tiled structures fit well on the back of phased array antennas, while vertical stacking can realize denser processing cubes better suited for tight spaces such as UAVs. Systems can be physically reconfigured to address different footprints while maintaining common hardware, firmware, and software across platforms and families of processing solutions.

(a) (b)

Figure 1: RARE Modules; (a) PPC+FPGA; (b) A/D+FPGA.

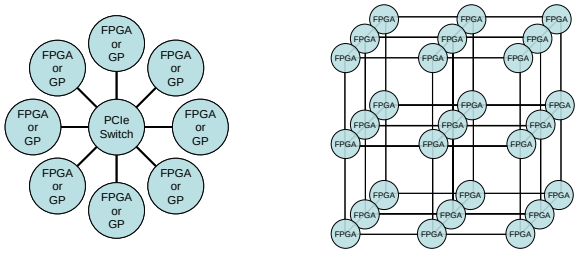
Figure 2: RARE 3D Connectivity between Modules.

A key distinguishing feature of RARE modules is that they are stand-alone; they do not require a backplane or chassis infrastructure for connectivity. They plug together similar to LEGOs™, thus supporting system modularity and fine-grain scalability. RARE's ability to increase processing horsepower or channel count on a small incremental basis reduces system board count, increases reliability, and reduces total ownership cost by optimizing the amount of hardware to what is needed to achieve the system.

High Bandwidth 3D Connectivity

Multiprocessing systems must provide a balance of high bandwidth cross-channel I/O and processing to achieve performance. The RARE architecture supports high capacity PCIe, LVDS, and SerDes communication links/fabrics between processing elements leveraging the

3D connectivity between modules. A single RARE module provides 39GB/sec of bandwidth with full crossbar functionality. Processing elements can communicate over a PCIe switched serial fabric while FPGA-specific elements can simultaneously use SerDes and LVDS to build three-dimensional interconnects (Figure 3) for extremely low-latency applications requiring high bandwidth cross-channel communications (such as digital beamforming). Legacy backplane connectivity approaches do not generally provide for dedicated FPGA communication planes.



(a) (b)

Figure 3: (a) PCIe Fabric; (b) 3D FPGA Connectivity.

Backplane architectures such as VXS and VPX typically rely on dedicated switch cards to support fabric interconnects between processing elements. RARE's integrated PCIe routing technology eliminates the need to spend dollars and SWaP resources on dedicated switch cards. By eliminating the need for a backplane and switch cards, system designers can package more high performance computing elements in a tighter SWaP envelope – critical for airborne sensor or avionics applications.

RARE's 3D connector topology also supports distributed I2C leveraging on-board microcontrollers. The network provides real-time health monitoring across the modules. The microcontrollers precisely monitor all voltages, currents, and temperatures in the system and can shut down modules if a problem is detected. The monitoring network also controls voltage sequencing and power distribution. RARE's embedded real-time health monitoring is key to supporting the requirements of mission-critical applications.

In addition to the inter-module 3D connectivity, the RARE architecture also provides "off module" interfaces including 1Gb/10Gb Ethernet, USB, JTAG, SPI, short-range wireless, and RS-232. The variety of standard interfaces supported within the RARE family promotes network connectivity with a wide range of 3rd party systems and subsystems, including commercially available switches and routers, and promotes the integration of a system-of-systems in a net-centric environment.

Graphical Programmability

In addition to developing a novel modular architecture for SWaP constrained applications, the MDA program also focused on facilitating model-based programmability. MATLAB™ and Simulink™ are defacto-standard tools for systems engineering, algorithm development, modeling, and simulation. RARE provides software wrappers around each module which allows them to be represented in a Simulink™ model flow. Thus a systems engineer can map functional blocks into the processing elements distributed across multiple RARE modules and define the I/O mechanisms between the elements.

The approach allows systems engineers to graphically program RARE's heterogeneous processing architecture through a well-established simulation, modeling, and development tool flow. It accelerates the design and verification process by eliminating the iterative, time consuming steps of converting MATLAB and Simulink models into C or VHDL code and generating the resulting embedded applications with separate tool flows and different engineering skill sets.

Example Applications

RARE is being utilized by multiple DoD agencies to economically meet SWaP constrained systems while adhering to Modular Open Systems Architecture (MOSA) design concepts. One example is a ship-based phased array radar program focused on scalability and affordability. RARE technology forms the basis of the digital receiver subsystem which can scale from 10s to 100s of channels. Another example is a small footprint programmable radar collection system (Figure 4). This application takes full advantage of RARE's ability to provide multiple analog channels and digital processing in a small space. It uses a DAC module to provide a multichannel programmable digital waveform generator (exciter), an ADC module to realize a multichannel digital receiver, and a processing module for data collection, user interfacing, and Ethernet networking to other systems. The operator can upload transmit waveforms, select modes, set PRFs, and enable collection windows to test radar waveforms in a real-world environment. The module stack up used to realize the system is 6.25" x 6.25" x 4" and contains two D/As, 10 A/Ds, three Xilinx Virtex-6 FPGAs, a PowerPC, and two 1GbE ports. In this configuration the FPGAs and PPC have PCIe connectivity while the FPGAs also can communicate directly via LVDS.

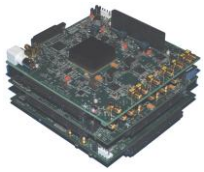


Figure 4. DREX Using Three RARE Modules.

A third example is the realization of a radar supporting sense-and-avoid (SAA) systems in UAVs. For this application, the baseline RARE ADC, DAC, and processor ecosystem was enhanced with the design of up/down converter and LO synthesizer modules adhering to the same philosophy pioneered under the MDA program.

Conclusion

RARE combines heterogeneous high performance computing, ease of programmability, and commercial standard I/O flexibility to facilitate cost-effective, scalable processing for SWaP-constrained applications. The approach enables embedded processing in spaces not amicable to backplane-centric solutions. The architecture's modularity and flexibility supports the integration of future A/Ds, D/As, processors, and other technologies not part of the baseline MDA program.