Modular, Scalable Computing for Systems with Tight SWaP Constraints

Prepared by
Colorado Engineering, Inc.
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Outline

• Highlight considerations for meeting Size, Weight, and Power (SWaP) of embedded processing systems within constrained platforms

• Present an architecture developed under a Missile Defense Agency (MDA) SBIR facilitating SWaP-optimized solutions
Meeting SWaP Challenges

• Suggests need for optimized system solutions
• Engineer should have flexibility to address size, weight, and power in trade space
• Ideal toolbox would be
  - Heterogeneous
    • ASICs
    • FPGAs
    • GPUs
    • General purpose / multi-core
  - Modular
  - Scalable
Legacy Approach to Modularity and Scalability: Backplanes

- Add weight, size, and cost
- Constrain incremental scalability
  - Truly SWaP-optimized, backplane-centric solution should have zero empty slots
  - But zero available slots means system cannot incrementally scale to address fluid requirements
  - Solution then requires an additional backplane, or a new backplane with more slots
- Bottom line: backplanes are not SWaP friendly
Out-of-the-Box Approach to Embedded Computing for SWaP

- CEI and the Navy, sponsored by MDA, defined an open approach to SWaP-friendly embedded computing architectures
  - NRL
  - NSWC
  - ONR
- RARE: Reconfigurable Advanced Rapid-prototyping Environment
- SBIR Phase I & II
- Recipient of 2011 Tibbetts Award
- No backplane!
RARE: MOSA-Inspired Technology

- Decomposes a general sensor system into functional COTS building blocks
- Blocks provide a modular way to achieve loosely coupled common operational subsystem components
- When tied together using well defined interfaces, blocks form a complete, scalable processing and control system
- Addresses systems for small UAVs to large manned aircraft
- Applicable to radar, -INT, EW, and digital communications
Modularity, Scalability, and Flexibility

- RARE modules are 6.25” x 6.25” cards with interface connections in all three dimensions (x, y, z)
  - PCIe fabric, LVDS, and SerDes for data and control plane communications
  - Provide combined I/O bandwidth of 39 GB/sec per module
- Allows integrators to stack and/or tile modules in x, y, or z to scale performance while simultaneously addressing processing load, I/O bandwidth, and physical installation footprint
  - Systems can be physically reconfigured to address different footprints while maintaining common hardware, firmware, and software across platforms
  - RARE modules can implement solutions in a fraction of the volume of traditional 20-slot 6U style backplanes
Module Examples

Processor Module
- AMCC 460SX PowerPC
- Xilinx Virtex-6 FPGA
- Dual 1Gb Ethernet
- USB, RS-232
- Short range wireless

Architecture easily incorporates other technologies (GPUs, multicore, ASICs, ADCs, DACs, I/O...)

ADC+Processor Module
- 10 ADC channels
- 16b @ 160MSPS
- Xilinx Virtex-6 FPGA

DAC+Processor Module
- 2 DAC channels
- 16b @ 1GSPS
- Xilinx Virtex-6 FPGA

Other Modules
- Dual 10Gb Ethernet
- Adapter for commercial PCIe cards
- Tailored interfaces
- High performance LO synthesis and clock distribution
- RF functions (up/down conversion)

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Heterogeneous Processing

### Xilinx Virtex 6 High Level Stats

<table>
<thead>
<tr>
<th>Part Number</th>
<th>XC6VLX240T</th>
<th>XC6VLX550T</th>
<th>XC6VSX475T (DSP optimized part)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLBs</td>
<td>18,840</td>
<td>42,960</td>
<td>37,200</td>
</tr>
<tr>
<td>Block Memory</td>
<td>14.976Mbits</td>
<td>22.752Mbits</td>
<td>38.304Mbits</td>
</tr>
<tr>
<td>Clock Managers (DLL/PLL)</td>
<td>12</td>
<td>18</td>
<td>18</td>
</tr>
<tr>
<td>Multiplier Accumulators</td>
<td>768</td>
<td>864</td>
<td>2,016</td>
</tr>
<tr>
<td>Configuration Memory</td>
<td>70.4Mbits</td>
<td>1.374Gbits</td>
<td>149.4Mbits</td>
</tr>
</tbody>
</table>

CLB= Configuration Logic Block: 8 x 6 input LUTs and 16 Flip-Flops

Multipliers = 18 to 40 bit inputs with 48-bit output  (much more functionality – 50 page data sheet)

### AMCC PPC460SX

- 1.2GHz
- Three Gen 2 PCI Express interfaces
- On-chip DDR2 SRAM controller
- Storage and network encryption engines
- 1Gb Ethernet, full duplex MACs with TCP/IP assist and Quality of Service support
# RARE Inter-Module I/O Bandwidths

<table>
<thead>
<tr>
<th>RARE Connector</th>
<th>Half Duplex (FPGA LVDS @ 1GHz)</th>
<th>Full Duplex</th>
<th>Bandwidth (per Connector)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td># of Clusters</td>
<td># of LVDS Pairs</td>
<td>LVDS Total (Gb/s)</td>
</tr>
<tr>
<td>X</td>
<td>3</td>
<td>7</td>
<td>21,000</td>
</tr>
<tr>
<td>Y</td>
<td>3</td>
<td>7</td>
<td>21,000</td>
</tr>
<tr>
<td>Z</td>
<td>2</td>
<td>13</td>
<td>26,000</td>
</tr>
</tbody>
</table>

## RARE Connector Total Bandwidths

<table>
<thead>
<tr>
<th>RARE Connector</th>
<th>Total Bandwidth (Dual Connectors per Direction)</th>
<th>Total Bandwidth per RARE Module</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>13.25 GB/s</td>
<td></td>
</tr>
<tr>
<td>Y</td>
<td>9.25 GB/s</td>
<td>39.00 GB/s</td>
</tr>
<tr>
<td>Z</td>
<td>16.50 GB/s</td>
<td></td>
</tr>
</tbody>
</table>
Cross Channel Communication without Dedicated Switch Cards

- FPGAs also interconnect with low latency, high bandwidth across the 3D topology
  - LVDS
  - SerDes

- PCIe switches built into modular architecture
- End points can be FPGAs or General Purpose Processors
### X and Y Interfaces per Module

**X & Y “1” Style Module Connectors (Plug into “2” Style)**

<table>
<thead>
<tr>
<th>Processor X1</th>
<th>Processor Y1</th>
<th>ADC Y1</th>
<th>DAC X1</th>
</tr>
</thead>
<tbody>
<tr>
<td>LVDS</td>
<td>LVDS</td>
<td>LVDS</td>
<td>LVDS</td>
</tr>
<tr>
<td>PCIe PPC</td>
<td>PCIe PPC</td>
<td>PCIe</td>
<td>PCIe</td>
</tr>
<tr>
<td>PCIe FPGA</td>
<td>PCIe FPGA</td>
<td>PCIe</td>
<td>PCIe</td>
</tr>
</tbody>
</table>

**X & Y “2” Style Module Connectors (Plug into “1” Style)**

<table>
<thead>
<tr>
<th>Processor X2</th>
<th>Processor Y2</th>
<th>ADC Y2</th>
<th>DAC X2</th>
</tr>
</thead>
<tbody>
<tr>
<td>LVDS</td>
<td>LVDS</td>
<td>LVDS</td>
<td>LVDS</td>
</tr>
<tr>
<td>PCIe PPC</td>
<td>PCIe PPC</td>
<td>PCIe</td>
<td>PCIe</td>
</tr>
<tr>
<td>PCIe FPGA</td>
<td>PCIe FPGA</td>
<td>PCIe</td>
<td>PCIe</td>
</tr>
</tbody>
</table>

- Supports LVDS, PCIe (PPC), and PCIe (FPGA) supports LVDS and PCIe (PPC) supports LVDS and PCIe (PPC)
- Supports LVDS and PCIe (PPC) supports LVDS (please call CEI for PCIe support)

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### Z Interfaces per Module

#### "Z" Style Module Connectors (1 ↔ 2; 3 ↔ 4)

<table>
<thead>
<tr>
<th>Processor Z1</th>
<th>Processor Z3</th>
<th>ADC Z1</th>
<th>DAC Z1</th>
<th>DAC Z3</th>
</tr>
</thead>
<tbody>
<tr>
<td>LVDS; PCIe PPC; PCIe FPGA</td>
<td>LVDS; PCIe FPGA</td>
<td>LVDS</td>
<td>LVDS; PCIe FPGA</td>
<td>n/a</td>
</tr>
<tr>
<td>LVDS; PCIe PPC; PCIe FPGA</td>
<td>n/a</td>
<td>supports LVDS</td>
<td>supports LVDS and PCIe (FPGA)</td>
<td>n/a</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Processor Z2</th>
<th>Processor Z4</th>
<th>ADC Z2</th>
<th>DAC Z2</th>
<th>DAC Z4</th>
</tr>
</thead>
<tbody>
<tr>
<td>LVDS; PCIe PPC; PCIe FPGA</td>
<td>SERDES</td>
<td>supports LVDS and PCIe (FPGA)</td>
<td>supports LVDS</td>
<td>supports SERDES</td>
</tr>
<tr>
<td>n/a</td>
<td>supports SERDES</td>
<td>n/a</td>
<td>supports LVDS</td>
<td>n/a</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Y1: LVDS; PCIe PPC</th>
<th>X1: LVDS; PCIe PPC; PCIe V6</th>
<th>Z1: LVDS; PCIe PPC; PCIe V6</th>
<th>Z3: SERDES</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>RARE PPC/FPGA Module</th>
<th>RARE ADC/FPGA Module</th>
<th>RARE DAC/FPGA Module</th>
</tr>
</thead>
<tbody>
<tr>
<td>Z1: LVDS</td>
<td>Z1: LVDS; PCIe V6</td>
<td>Z1: LVDS; PCIe V6</td>
</tr>
<tr>
<td>Z2: LVDS; PCIe PPC; PCIe V6</td>
<td>Z2: LVDS; PCIe V6</td>
<td>Z2: LVDS</td>
</tr>
<tr>
<td>Z4: SERDES</td>
<td>Z4: SERDES</td>
<td>Z4: SERDES</td>
</tr>
</tbody>
</table>

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Integrated Health and Status Monitoring

• $I^2C$ network of microcontrollers distributed throughout architecture for health and status
  - ADCs built into microcontrollers monitor voltages, currents, and temperatures
  - Used to sequence power supplies and protect modules in event of supply issues or overheating
  - Microcontrollers can shut down modules or system when tolerances are not within defined limits

• Fully programmable and tailorable
• More information available in poster session

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Software and High Level Programming Model

- Leverages open source
  - Avoids sole source proprietary operating systems
  - Lower TOC
  - Can be tailored by user
- SDK handles module communications protocols and data movement between processors and FPGAs
  - Linux kernel
  - Fedora x86-64 gcc cross compiler tool chain
  - U-Boot boot loader
  - Core root file system
- Code wrappers encapsulate modules and enable MATLAB™ / Simulink™ tool flows for code development
- Enables quick turn from algorithms concept and simulation to implementation
SDK Encompasses CPUs and FPGAs
Packaging Strategies

• RARE flexibility opens up packaging trade space to systems integrator
  - Physical enclosure
  - Thermal management

• Enables solutions that are truly optimized for C-SWaP on the deployment platform
  - Standard 19” rack mount enclosure
  - Tailored box-level solutions
  - Platform-ready deployment
Extreme Packaging Flexibility to Address Size: FlexRARE

- Increases system “morphability,” flexibility, and out-of-the-box installations (literally!)
- Increases bandwidth for stacked systems
- No performance degradation
- Fully customizable cable lengths available (SamTec)
- Right angle or straight connectors available
- Promotes straight-forward board level replacement in mesh structure
Example Applications

• RARE architecture is being utilized by multiple DoD agencies to meet C-SWaP while adhering to MOSA philosophies

• Two examples
  - Programmable MIMO radar transmit / receive system
  - Sense and Avoid radar for UAVs
Example 1: Multichannel DREX

- Programmable MIMO radar transmit / receive system
- Uses three COTS RARE modules
  - 2x exciter channels (1 GHz)
  - 10x receive channels (160 MSPS)
  - 3x Virtex-6 FPGAs
  - 1x PPC
  - 2x 1GbE
- Electronics: 6.25” x 6.25” x 4”
- Dual 10GbE can be supported through the addition of one more module
Example 2: Sense and Avoid Radar

- Turnkey search & track capability
- 21.25” x 16” x 5.5”
- 400W input power (28VDC)
- <45 lbs.

Antenna Sub-Assembly
Includes heat sink and mounting hardware

RF Sub-Assembly
Up converter
Down converters
LO Synthesis
RF filters

Digital Electronics Sub-Assembly
6 RARE modules in 2 layers
(capacity = 9 in 3 layers)
Summary

• RARE facilitates embedded processing solutions for SWaP-constrained applications
  - Heterogeneous technology helps balance processing capability with power consumption
  - Solutions are not backplane constrained thus maximizing flexibility within SWaP trade space
  - Architecture enables integrators to simultaneously address processing capacity, I/O bandwidth, and physical installation footprint while eliminating the cost and impact of backplane and dedicated switch card architectures
  - Model-based software development accelerates transition from algorithmic concept to deployment

• MOSA approach facilitates the realization of common subsystem building blocks and lowers total ownership costs

• Award winning technology being utilized in multiple DoD programs
Thank You!

For more information please contact:

Michael J. Bonato  
Colorado Engineering, Inc.  
michael.bonato@coloradoengineeringinc.com  
719-388-8582 (office)

www.coloradoengineeringinc.com
About Colorado Engineering

- Provides engineered solutions for high performance computing and sensor systems
  - Hardware: FPGA design and multi-layer high speed digital and analog circuit card designs for C-SWaP
  - Software: high performance computing and system management at real-time embedded and enterprise levels
  - Systems: radar, -INT, EW, digital communications, DSP, grid computing, situational awareness, THz technologies
- Recognized industry leaders in MOSA applications
- Cross discipline experience of engineering staff
- Woman-Owned small business located in Colorado Springs
- TS facility clearance (in process)
- Recent recipient of Tibbetts and Nunn-Perry awards
- 23 Phase I/II SBIR & STTR awards with over 37 technologies deployed in DoD and Government systems
- For more information
  - www.coloradoengineeringinc.com
  - 719-388-8582