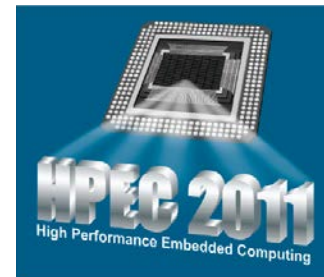




Modular, Scalable Computing for Systems with Tight SWaP Constraints

Prepared by
Colorado Engineering, Inc.
for HPEC 2011
September 21, 2011



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Outline

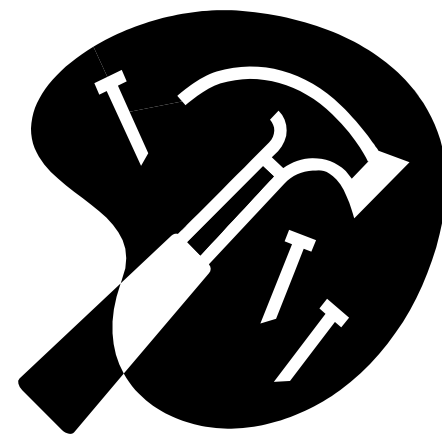
- Highlight considerations for meeting Size, Weight, and Power (SWaP) of embedded processing systems within constrained platforms
- Present an architecture developed under a Missile Defense Agency (MDA) SBIR facilitating SWaP-optimized solutions





Meeting SWaP Challenges

- Suggests need for optimized system solutions
- Engineer should have flexibility to address size, weight, and power in trade space
- Ideal toolbox would be
 - Heterogeneous
 - ASICs
 - FPGAs
 - GPUs
 - General purpose / multi-core
 - Modular
 - Scalable





Legacy Approach to Modularity and Scalability: Backplanes

- Add weight, size, and cost
- Constrain incremental scalability
 - Truly SWaP-optimized, backplane-centric solution should have zero empty slots
 - But zero available slots means system cannot incrementally scale to address fluid requirements
 - Solution then requires an additional backplane, or a new backplane with more slots
- Bottom line: backplanes are not SWaP friendly



Image courtesy of Kontron

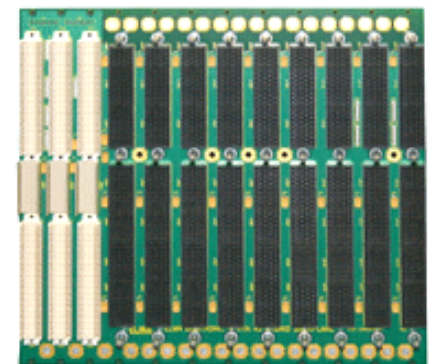


Image courtesy of Elma Bustronic

Out-of-the-Box Approach to Embedded Computing for SWaP



- CEI and the Navy, sponsored by MDA, defined an open approach to SWaP-friendly embedded computing architectures
 - NRL
 - NSWC
 - ONR
- RARE: Reconfigurable Advanced Rapid-prototyping Environment
- SBIR Phase I & II
- Recipient of 2011 Tibbetts Award
- No backplane!





RARE: MOSA-Inspired Technology

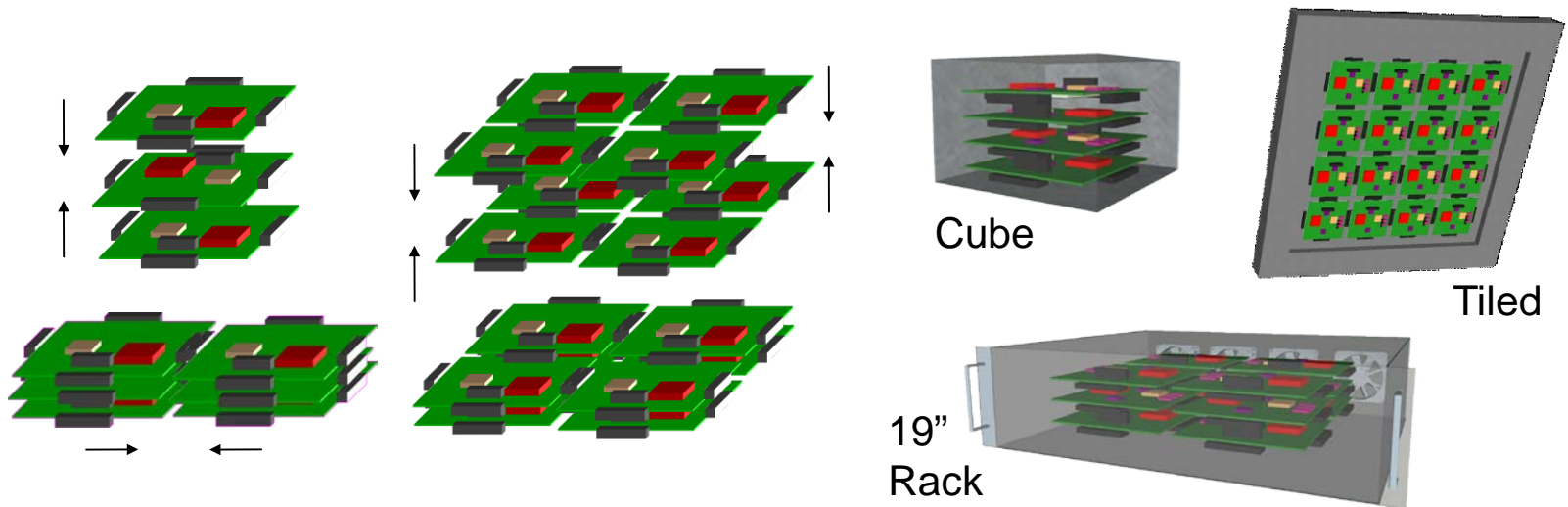
- Decomposes a general sensor system into functional COTS building blocks
- Blocks provide a modular way to achieve loosely coupled common operational subsystem components
- When tied together using well defined interfaces, blocks form a complete, scalable processing and control system
- Addresses systems for small UAVs to large manned aircraft
- Applicable to radar, -INT, EW, and digital communications



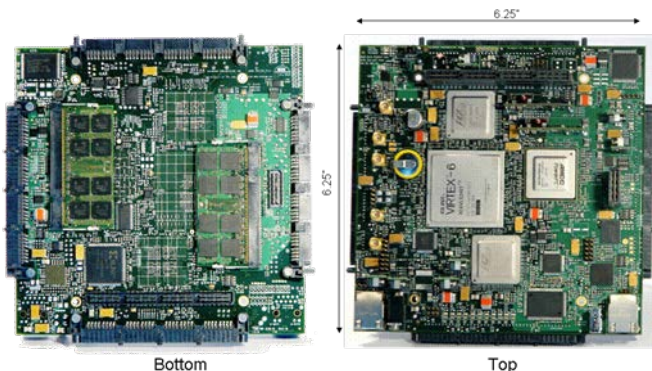


Modularity, Scalability, and Flexibility

- RARE modules are 6.25" x 6.25" cards with interface connections in all three dimensions (x, y, z)
 - PCIe fabric, LVDS, and SerDes for data and control plane communications
 - Provide combined I/O bandwidth of 39 GB/sec per module
- Allows integrators to stack and/or tile modules in x, y, or z to scale performance while simultaneously addressing processing load, I/O bandwidth, and physical installation footprint
 - Systems can be physically reconfigured to address different footprints while maintaining common hardware, firmware, and software across platforms
 - RARE modules can implement solutions in a fraction of the volume of traditional 20-slot 6U style backplanes



Module Examples



Processor Module

- AMCC 460SX PowerPC
- Xilinx Virtex-6 FPGA
- Dual 1Gb Ethernet
- USB, RS-232
- Short range wireless

Architecture easily incorporates other technologies (GPUs, multicore, ASICs, ADCs, DACs, I/O...)



ADC+Processor Module

- 10 ADC channels
- 16b @ 160MSPS
- Xilinx Virtex-6 FPGA



DAC+Processor Module

- 2 DAC channels
- 16b @ 1GSPS
- Xilinx Virtex-6 FPGA

Other Modules

- Dual 10Gb Ethernet
- Adapter for commercial PCIe cards
- Tailored interfaces
- High performance LO synthesis and clock distribution
- RF functions (up/down conversion)



Modules Stacked



Modules Tiled



Heterogeneous Processing

XILINX VIRTEX 6 HIGH LEVEL STATS

Part Number:	XC6VLX240T	XC6VLX550T	XC6VVSX475T (DSP)
optimized part)			
CLBs	18,840	42,960	37,200
Block Memory	14.976Mbits	22.752Mbits	38.304Mbits
Clock Managers (DLL/PLL)	12	18	18
Multiplier Accumulators	768	864	2,016
Configuration Memory	70.4Mbits	1.374Gbits	149.4Mbits



CLB= Configuration Logic Block: 8 x 6 input LUTs and 16 Flip-Flops
Multipliers = 18 to 40 bit inputs with 48bit output (much more functionality – 50 page data sheet)

AMCC PPC460SX

- 1.2GHz
- Three Gen 2 PCI Express interfaces
- On-chip DDR2 SRAM controller
- Storage and network encryption engines
- 1Gb Ethernet, full duplex MACs with TCP/IP assist and Quality of Service support





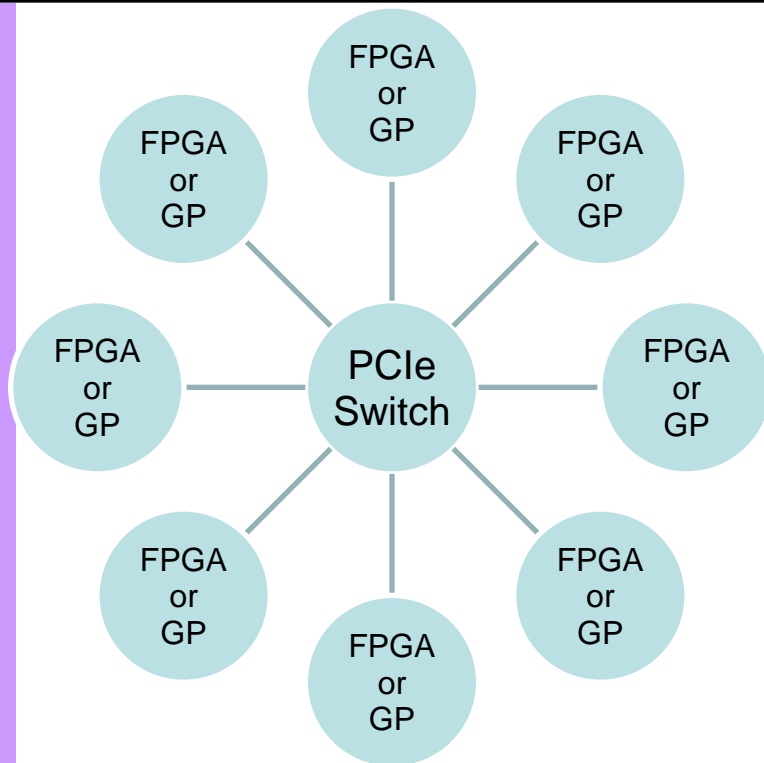
RARE Inter-Module I/O Bandwidths

RARE Connector	Half Duplex (FPGA LVDS @ 1GHz)				Full Duplex			Bandwidth (per Connector)
	# of Clusters	# of LVDS Pairs	LVDS Total (Gb/s)	LVDS Total (MB/s)	PCIe FPGA (MB/s)	PCIe PPC (MB/s)	SerDes FPGA (MB/s)	
X	3	7	21,000	2,625	2,000	2,000	0	6.625 GB/s
Y	3	7	21,000	2,625	0	2,000	0	4.625 GB/s
Z	2	13	26,000	3,250	2,000	2,000	1,000	8.250 GB/s

RARE Connector	Total Bandwidth (Dual Connectors per Direction)	Total Bandwidth per RARE Module
X	13.25 GB/s	39.00 GB/s
Y	9.25 GB/s	
Z	16.50 GB/s	

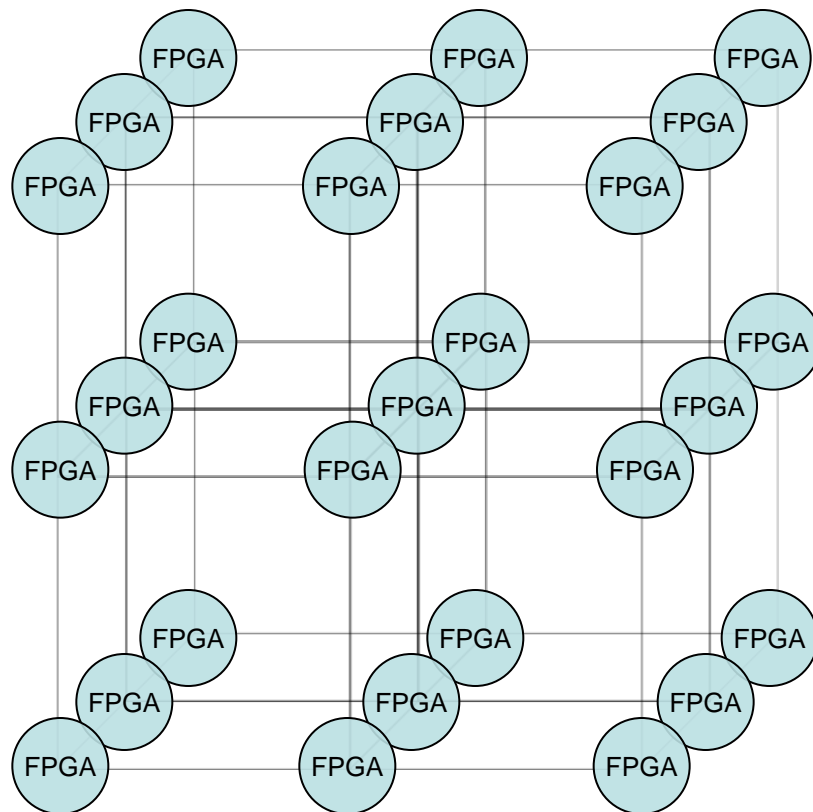
RARE Modules Balance High Bandwidth Cross-Channel I/O with Processing to Maximize Performance.

Cross Channel Communication without Dedicated Switch Cards



- PCIe switches built into modular architecture
- End points can be FPGAs or General Purpose Processors

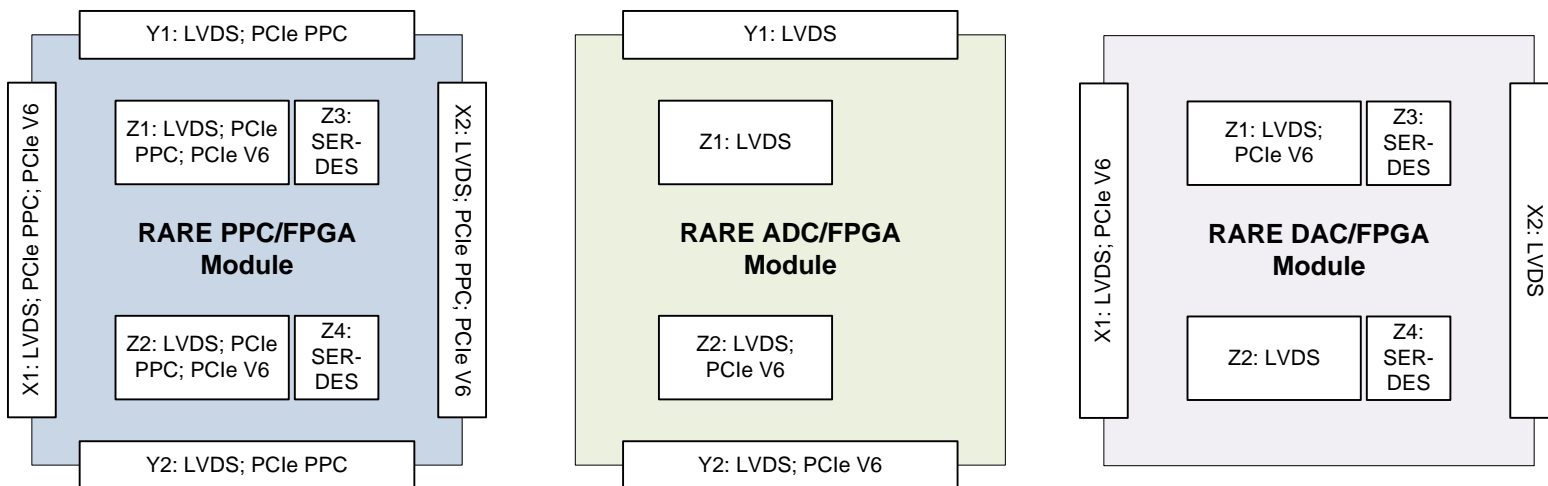
- FPGAs also interconnect with low latency, high bandwidth across the 3D topology
 - LVDS
 - SerDes





X and Y Interfaces per Module

		X & Y “1” Style Module Connectors (Plug into “2” Style)			
		Processor X1 - LVDS - PCIe PPC - PCIe FPGA	Processor Y1 - LVDS - PCIe PPC	ADC Y1 - LVDS	DAC X1 - LVDS - PCIe FPGA
X & Y “2” Style Module Connectors (Plug into “1” Style)	Processor X2 - LVDS - PCIe PPC - PCIe FPGA	supports LVDS, PCIe (PPC), and PCIe (FPGA)	supports LVDS and PCIe (PPC)	supports LVDS	supports LVDS and PCIe (FPGA)
	Processor Y2 - LVDS - PCIe PPC	supports LVDS and PCIe (PPC)	supports LVDS and PCIe (PPC)	supports LVDS	supports LVDS
	ADC Y2 - LVDS - PCIe FPGA	supports LVDS and PCIe (FPGA)	supports LVDS	supports LVDS	supports LVDS (please call CEI for PCIe support)
	DAC X2 - LVDS	supports LVDS	supports LVDS	supports LVDS	supports LVDS

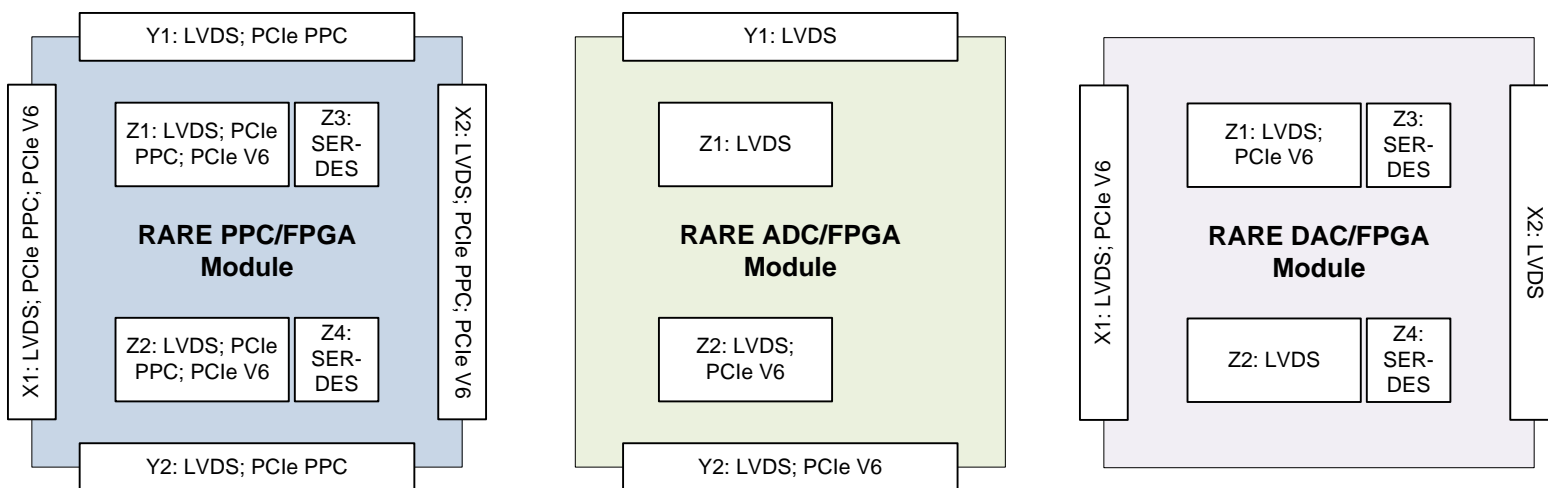


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Z Interfaces per Module

		"Z" Style Module Connectors (1 ↔ 2; 3 ↔ 4)				
		Processor Z1 - LVDS - PCIe PPC - PCIe FPGA	Processor Z3 - SERDES	ADC Z1 - LVDS	DAC Z1 - LVDS - PCIe FPGA	DAC Z3 - SERDES
"Z" Style Module Connectors (1 ↔ 2; 3 ↔ 4)	Processor Z2 - LVDS - PCIe PPC - PCIe FPGA	supports LVDS, PCIe (PPC), and PCIe (FPGA)	n/a	supports LVDS	supports LVDS and PCIe (FPGA)	n/a
	Processor Z4 - SERDES	n/a	supports SERDES	n/a	n/a	supports SERDES
	ADC Z2 - LVDS - PCIe FPGA	supports LVDS and PCIe (FPGA)	n/a	supports LVDS	supports LVDS (please call CEI for PCIe support)	n/a
	DAC Z2 - LVDS	supports LVDS	n/a	supports LVDS	supports LVDS	n/a
	DAC Z4 - SERDES	n/a	supports SERDES	n/a	n/a	supports SERDES



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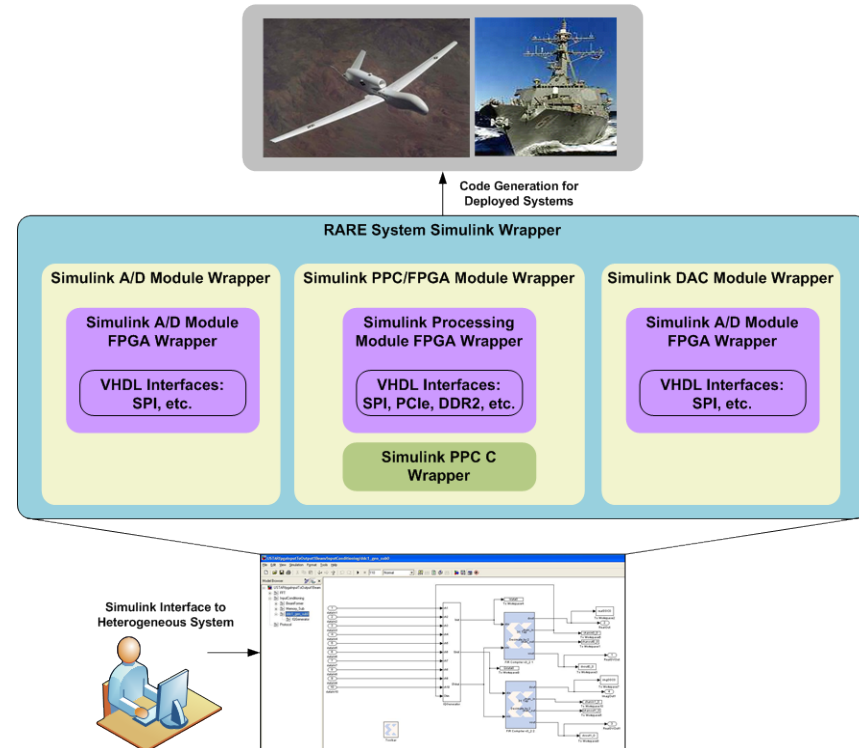
Integrated Health and Status Monitoring

- I²C network of microcontrollers distributed throughout architecture for health and status
 - ADCs built into microcontrollers monitor voltages, currents, and temperatures
 - Used to sequence power supplies and protect modules in event of supply issues or overheating
 - Microcontrollers can shut down modules or system when tolerances are not within defined limits
- Fully programmable and tailorable
- More information available in poster session

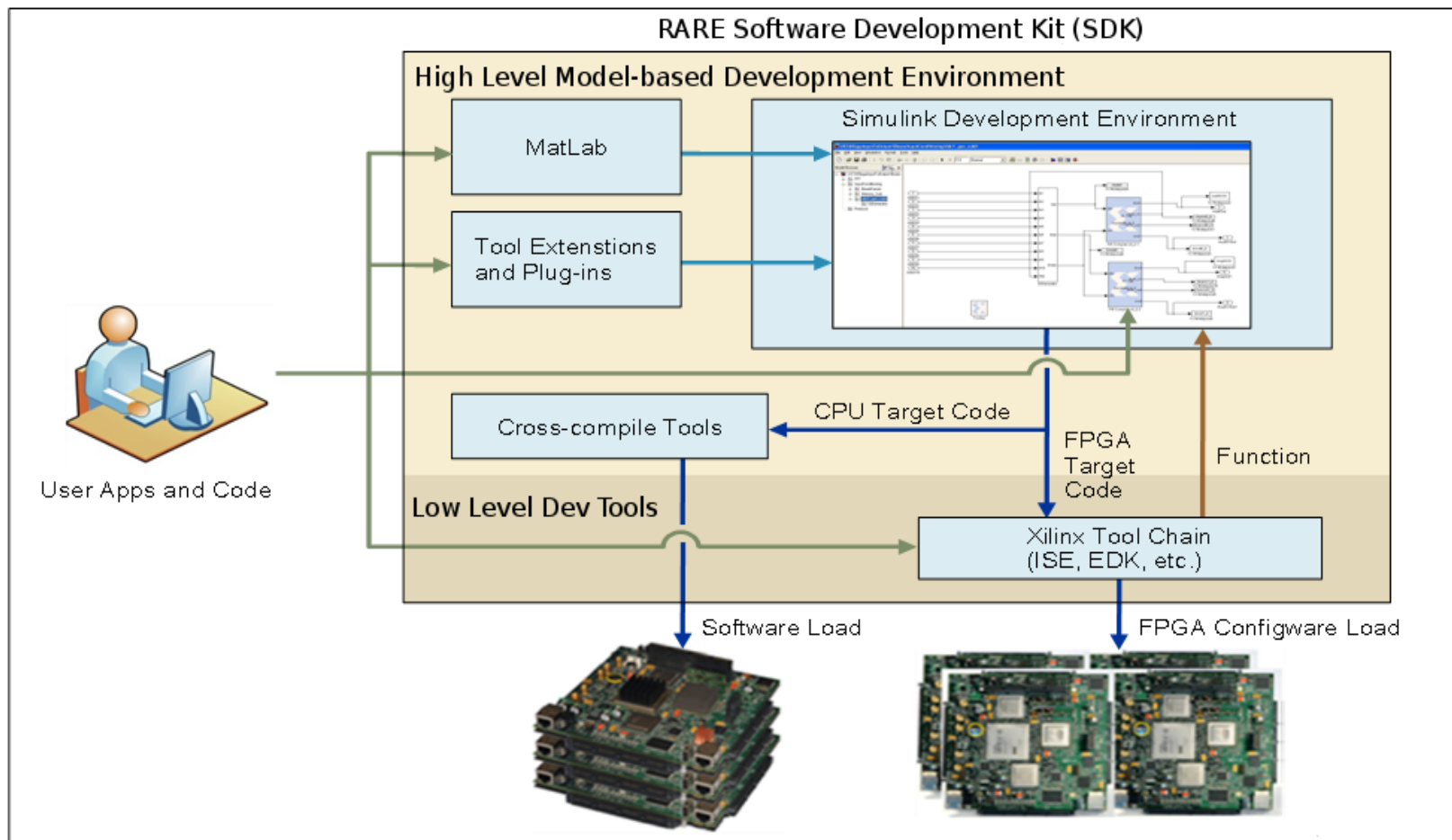
Software and High Level Programming Model



- Leverages open source
 - Avoids sole source proprietary operating systems
 - Lower TOC
 - Can be tailored by user
- SDK handles module communications protocols and data movement between processors and FPGAs
 - Linux kernel
 - Fedora x86-64 gcc cross compiler tool chain
 - U-Boot boot loader
 - Core root file system
- Code wrappers encapsulate modules and enable MATLAB™ / Simulink™ tool flows for code development
- Enables quick turn from algorithms concept and simulation to implementation



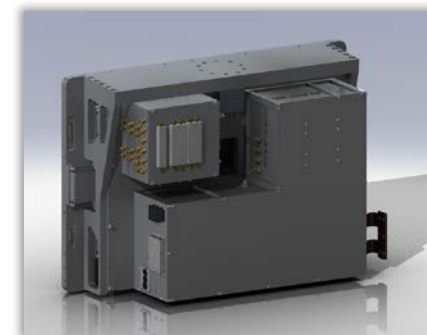
SDK Encompasses CPUs and FPGAs





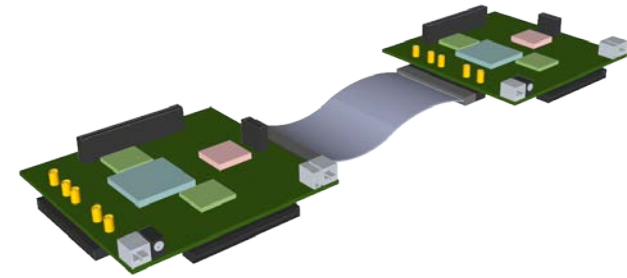
Packaging Strategies

- RARE flexibility opens up packaging trade space to systems integrator
 - Physical enclosure
 - Thermal management
- Enables solutions that are truly optimized for C-SWaP on the deployment platform
 - Standard 19” rack mount enclosure
 - Tailored box-level solutions
 - Platform-ready deployment

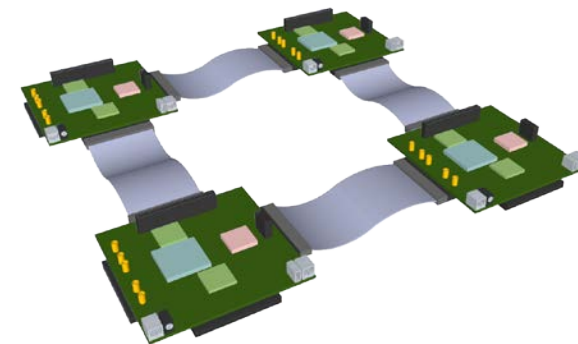


Extreme Packaging Flexibility to Address Size: FlexRARE

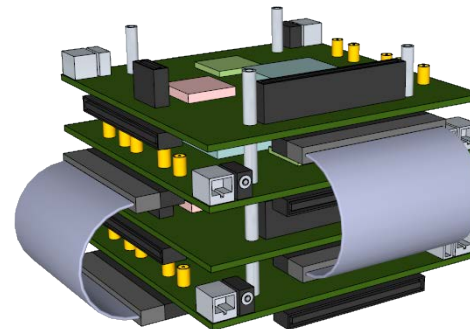
- Increases system “morphability,” flexibility, and out-of-the-box installations (literally!)
- Increases bandwidth for stacked systems
- No performance degradation
- Fully customizable cable lengths available (SamTec)
- Right angle or straight connectors available
- Promotes straight-forward board level replacement in mesh structure



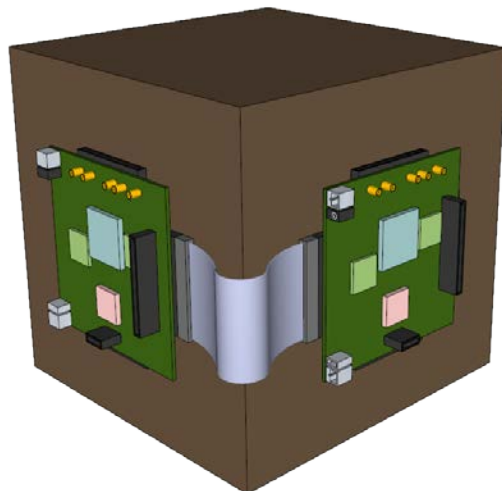
Ex: FlexRARE Basic Option



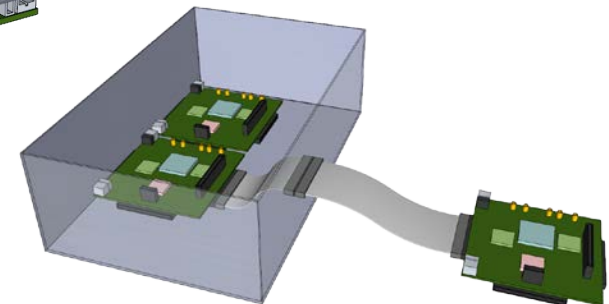
Ex: FlexRARE Mesh Option



Ex: FlexRARE Stackable Option



Ex: FlexRARE Corner-Turn Option



Ex: FlexRARE Through-Wall Option



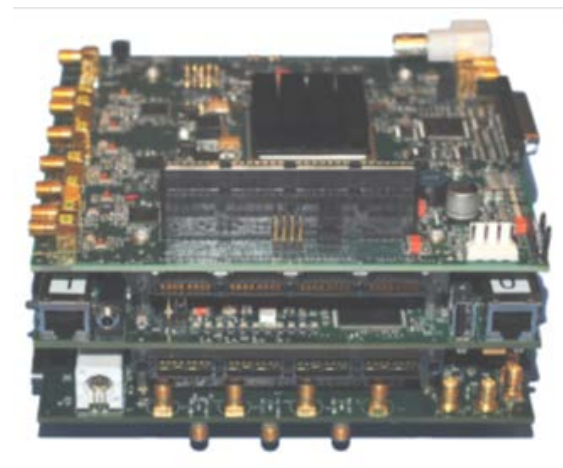
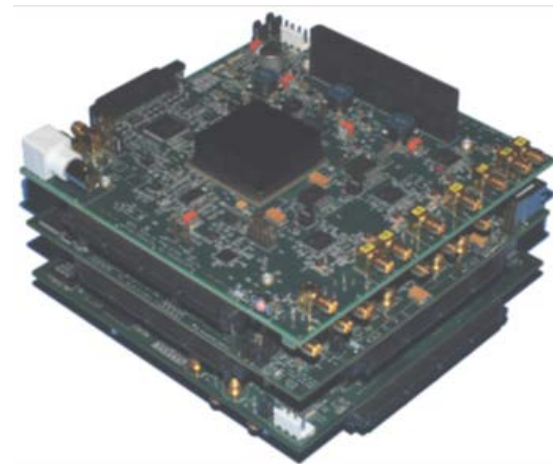
Example Applications

- RARE architecture is being utilized by multiple DoD agencies to meet C-SWaP while adhering to MOSA philosophies
- Two examples
 - Programmable MIMO radar transmit / receive system
 - Sense and Avoid radar for UAVs



Example 1: Multichannel DREX

- Programmable MIMO radar transmit / receive system
- Uses three COTS RARE modules
 - 2x exciter channels (1 GHz)
 - 10x receive channels (160 MSPS)
 - 3x Virtex-6 FPGAs
 - 1x PPC
 - 2x 1GbE
- Electronics: 6.25" x 6.25" x 4"
- Dual 10GbE can be supported through the addition of one more module

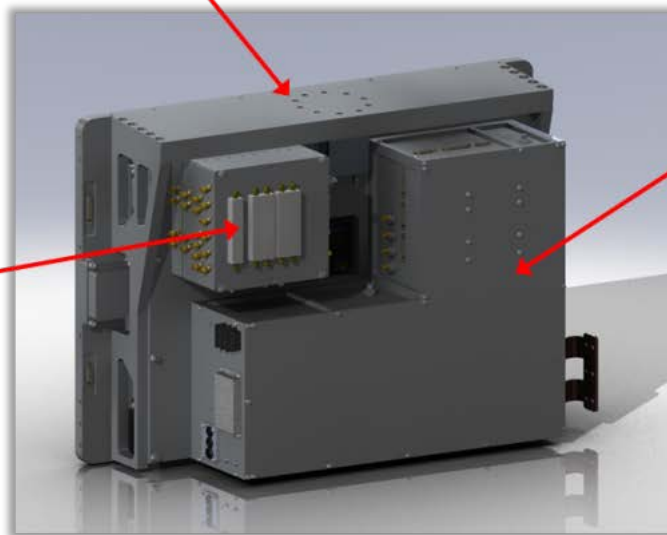




Example 2: Sense and Avoid Radar

- Turnkey search & track capability
- 21.25" x 16" x 5.5"
- 400W input power (28VDC)
- < 45 lbs.

Antenna Sub-Assembly
Includes heat sink and mounting hardware



RF Sub-Assembly
Up converter
Down converters
LO Synthesis
RF filters

Digital Electronics Sub-Assembly
6 RARE modules in 2 layers
(capacity = 9 in 3 layers)



Summary

- RARE facilitates embedded processing solutions for SWaP-constrained applications
 - Heterogeneous technology helps balance processing capability with power consumption
 - Solutions are not backplane constrained thus maximizing flexibility within SWaP trade space
 - Architecture enables integrators to simultaneously address processing capacity, I/O bandwidth, and physical installation footprint while eliminating the cost and impact of backplane and dedicated switch card architectures
 - Model-based software development accelerates transition from algorithmic concept to deployment
- MOSA approach facilitates the realization of common subsystem building blocks and lowers total ownership costs
- Award winning technology being utilized in multiple DoD programs



Thank You!

For more information please contact:

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About Colorado Engineering

- Provides engineered solutions for high performance computing and sensor systems
 - Hardware: FPGA design and multi-layer high speed digital and analog circuit card designs for C-SWaP
 - Software: high performance computing and system management at real-time embedded and enterprise levels
 - Systems: radar, -INT, EW, digital communications, DSP, grid computing, situational awareness, THz technologies
- Recognized industry leaders in MOSA applications
- Cross discipline experience of engineering staff
- Woman-Owned small business located in Colorado Springs
- TS facility clearance (in process)
- Recent recipient of Tibbetts and Nunn-Perry awards
- 23 Phase I/II SBIR & STTR awards with over 37 technologies deployed in DoD and Government systems
- For more information
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