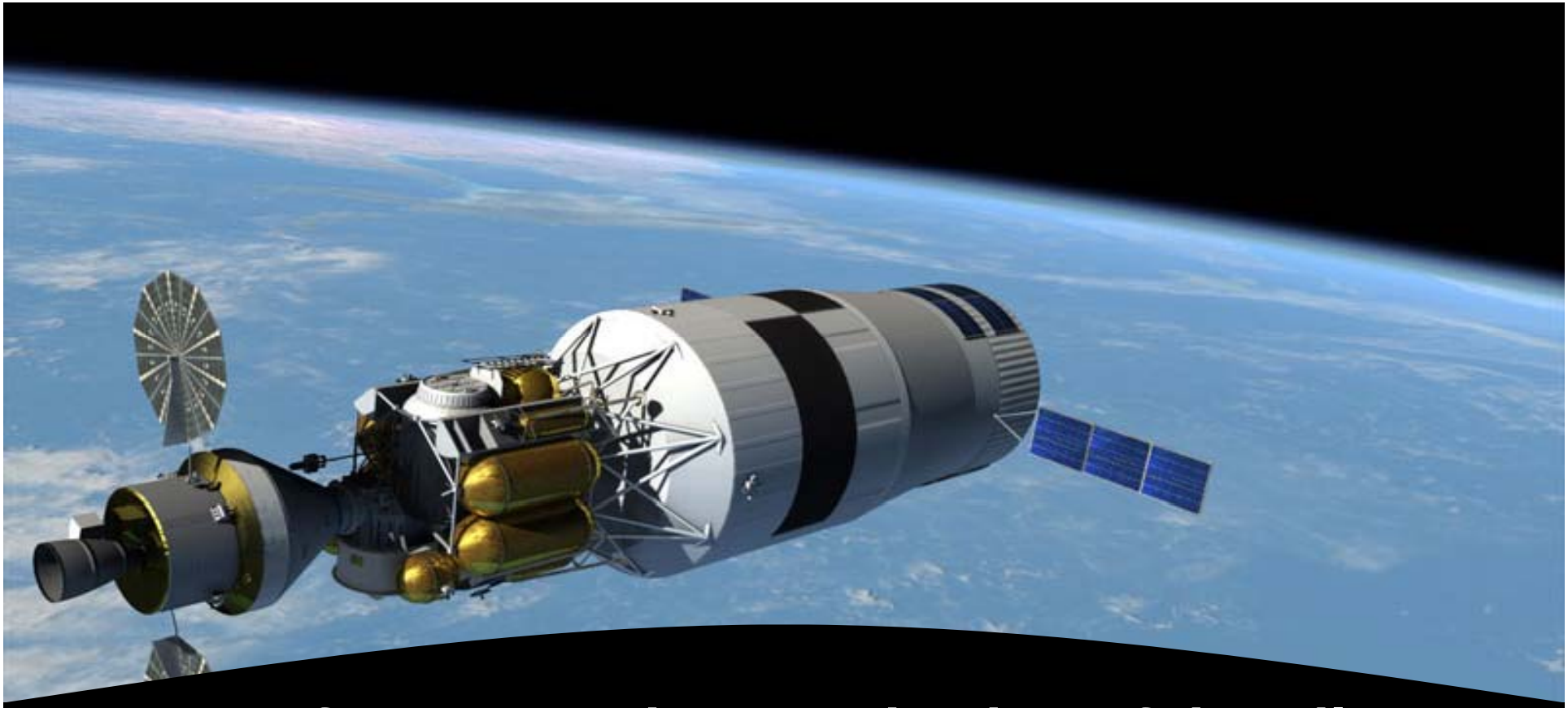

Performance Characterization of the Tile Architecture

Précis Presentation

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Honeywell

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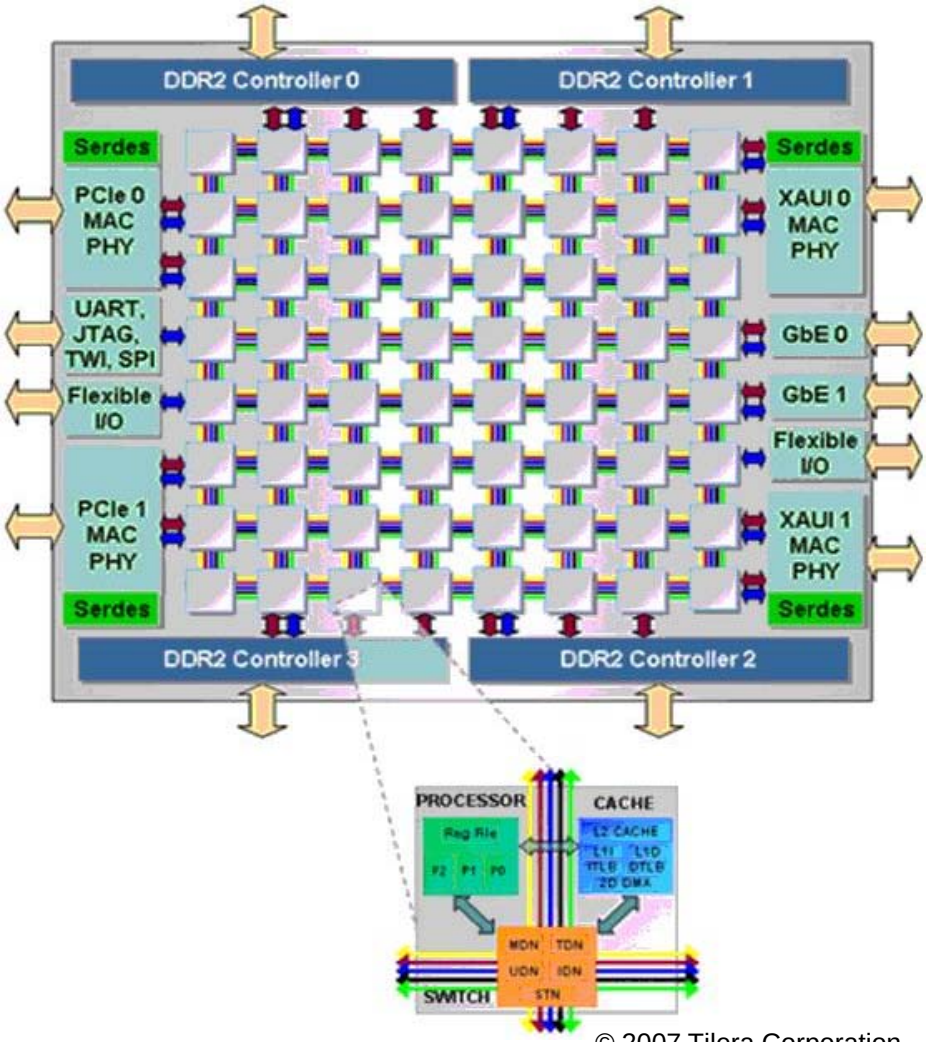
Tilera Tile64

Tile64 Features

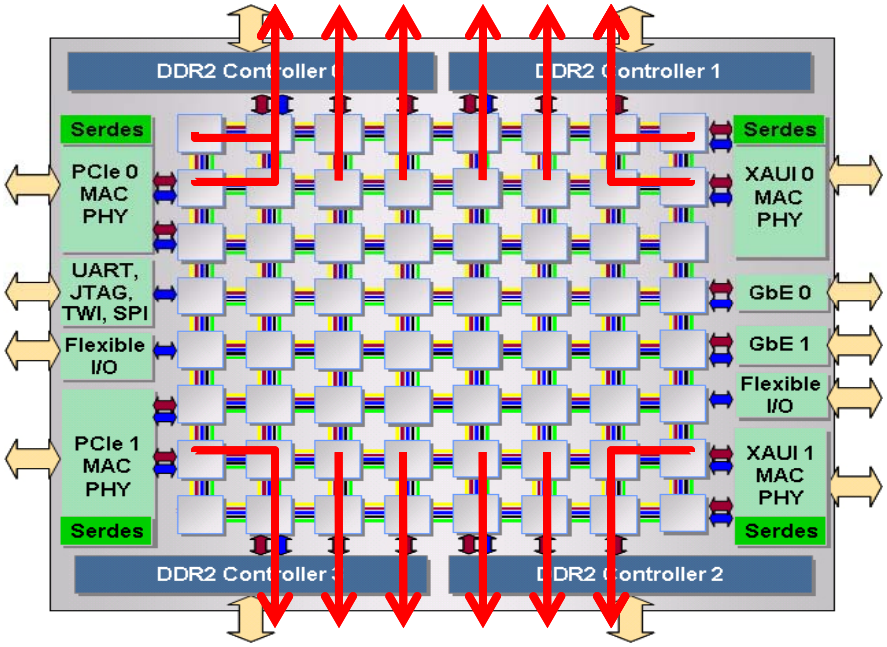
- Tilera *64-core* processor @700MHz
  - 8x8 grid of processor cores with iMesh interconnect
  - 4x DDR2 memory controllers with optional ECC
  - 2x 10GbE XAUI configurable MAC or PHY Interfaces
  - 2x 1GbE MAC interfaces
  - 2x 4-lane PCIe interfaces
  - Connectors for utility IO (GPIO, I2C, UART, HPI, etc).
- Standard development tools
  - Eclipse based IDE
  - ANSI standard C/C++ compiler
  - Supports Linux 2.6 SMP kernel
  - Libraries for inter-tile communication.

Intended Application Domains

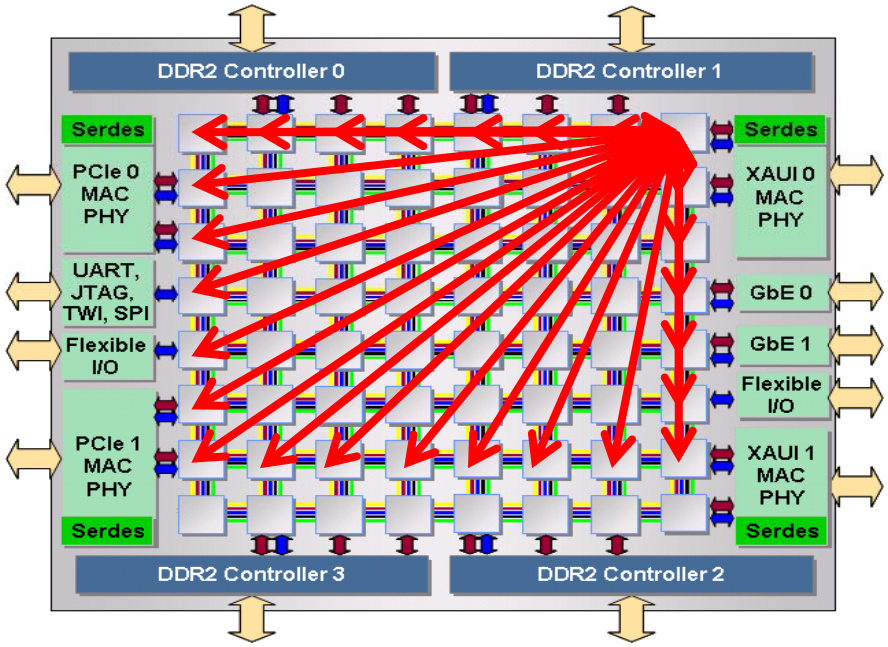
- Cloud Computing
- Wireless Infrastructure
  - Digital Baseband
  - Wireless Core Networks
- Advanced Networking
  - Unified Threat Management
  - Network Security Appliances
  - In-Line L4-7 Deep Packet Inspection
  - Quality of Service
- Digital AV Processing
  - AV Encoding/Transcoding
  - Video on Demand
  - Video Surveillance



Tile Architecture Benchmarks



DMA write transfers were executed for each tile between its local buffer and process-private memory allocated on the heap. Memory interface was tested for both geographic preference and user selection, as well as with and without cross-tile traffic noise.



iLib messages were sent from a single tile to a “ring” of receiver tiles using the available channels (raw, streaming, buffered) for a varying number of packets and payload sizes.

Benchmarking Results

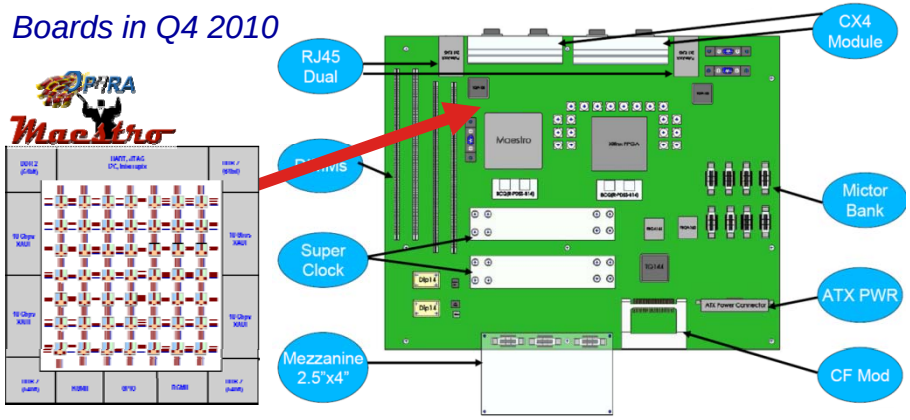
- **Results of each benchmark are available at the poster session**
- **Analysis will guide porting efforts as applications move from a single core to multi-core platform.**
- **The Radiant Lab at Honeywell is focusing on performance issues with multi-core computing as customers seek increasingly better performance for their applications.**

Honeywell *Symphony MEP*

Symphony Maestro/SIRF Exploration Platform

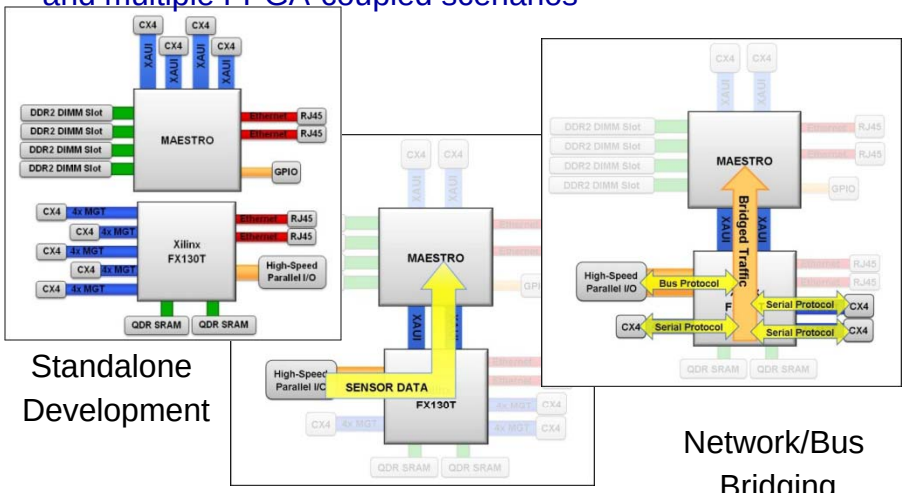
- Prototyping platform for both Maestro and SIRF processors on a single board
- Boeing Rad-Hard Maestro *49-core* processor
  - 4x DDR DIMM slots that accept standard PC3200 memory modules
  - 2x 10/100/1000 Base-T Ethernet ports
  - 4x 10 Gbps XAUI ports (CX4 connectors)
  - Connectors for utility IO (GPIO, I2C, UART, HPI, etc).
- Xilinx SIRF or FX130T commercial FPGA part compatible
  - 2x banks of QDR SRAM (72Mb each)
  - ~5x 10Gbps SERDES (CX4 connectors)
  - 256 bits of GPIO
- Symphony versions of standard development tools
  - Maestro MDE with networked boot of Maestro via TFTP

Boards in Q4 2010



Detailed whitepaper on Symphony available upon request

Symphony supports standalone Maestro/SIRF development and multiple FPGA-coupled scenarios



Standalone Development

Sensor Interfacing

Network/Bus Bridging

Why Symphony?

- Addresses need for a flexible Maestro and SIRF prototyping platform to explore real-world processing applications
  - Allows integration with external hardware for streaming of real data in processing applications
  - Exploration of advanced Maestro/SIRF partitioned application configurations

Additional features

- Powered via standard ATX (PC) power supply
- All major IO groups of both Maestro and Xilinx FPGA are accessible via commercial connectors
- Removable non-volatile memory for storing Maestro boot images and FPGA configuration images

Symphony - Advanced Maestro & SIRF Prototyping Platform