A Prototype FPGA Tile for Subthreshold-Optimized CMOS

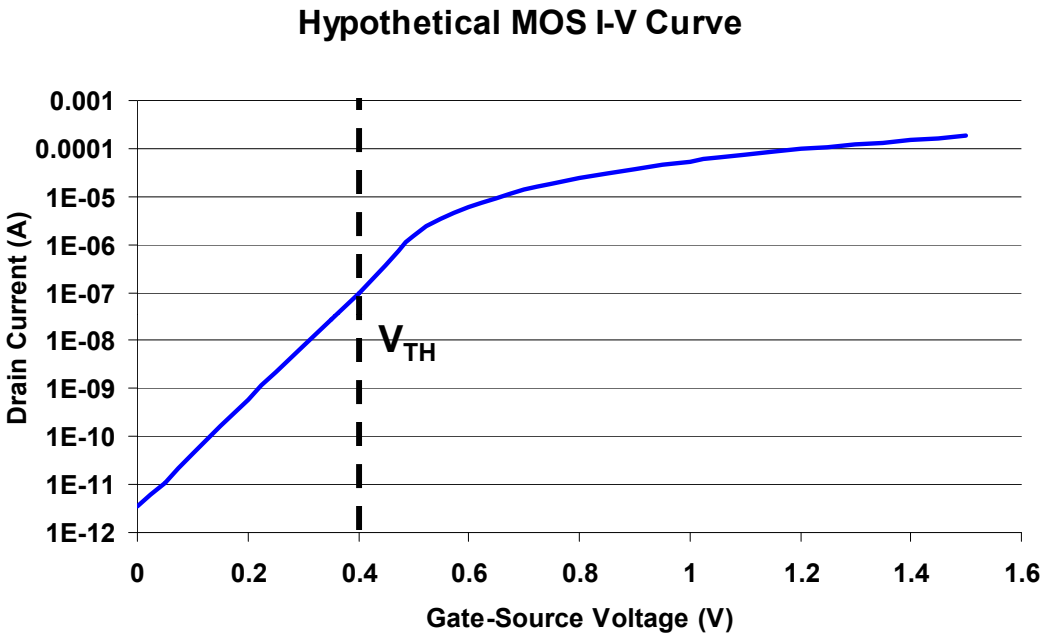
Northeastern University

Peter Grossmann, Miriam Leeser

- Low power systems benefit from FPGAs
  - Improved energy efficiency/performance vs. microcontroller
  - Improved design via reconfigurability
  - Lower cost vs. ASIC
- State of the art low power FPGAs: 10s to 100s of mW
- Ultra-low power applications require 10s to 100s of *µW*
  - Wireless sensor networks
  - RFID
  - Digital hearing aids
- Ultra-low power budgets motivate extreme voltage scaling
  - Subthreshold supply voltages yield peak energy efficiency

This work is funded by the Lincoln Scholars Program, MIT Lincoln Laboratory. The Lincoln Laboratory portion of this work was sponsored by the United States Government under Air Force contract number FA8721-05-C-0002. The opinions, interpretations, conclusions and recommendations are those of the authors and are not necessarily endorsed by the United States Government.

Subthreshold vs. Superthreshold Circuits



$$I_D = I_0 \frac{W}{L} e^{\frac{V_{GS}-V_{TH}}{nV_T}} \left[1 - e^{\frac{-V_{DS}}{V_T}}\right]$$

Subthreshold

$$I_D = I_0 \frac{W}{L} (V_{GS} - V_{TH})^2$$

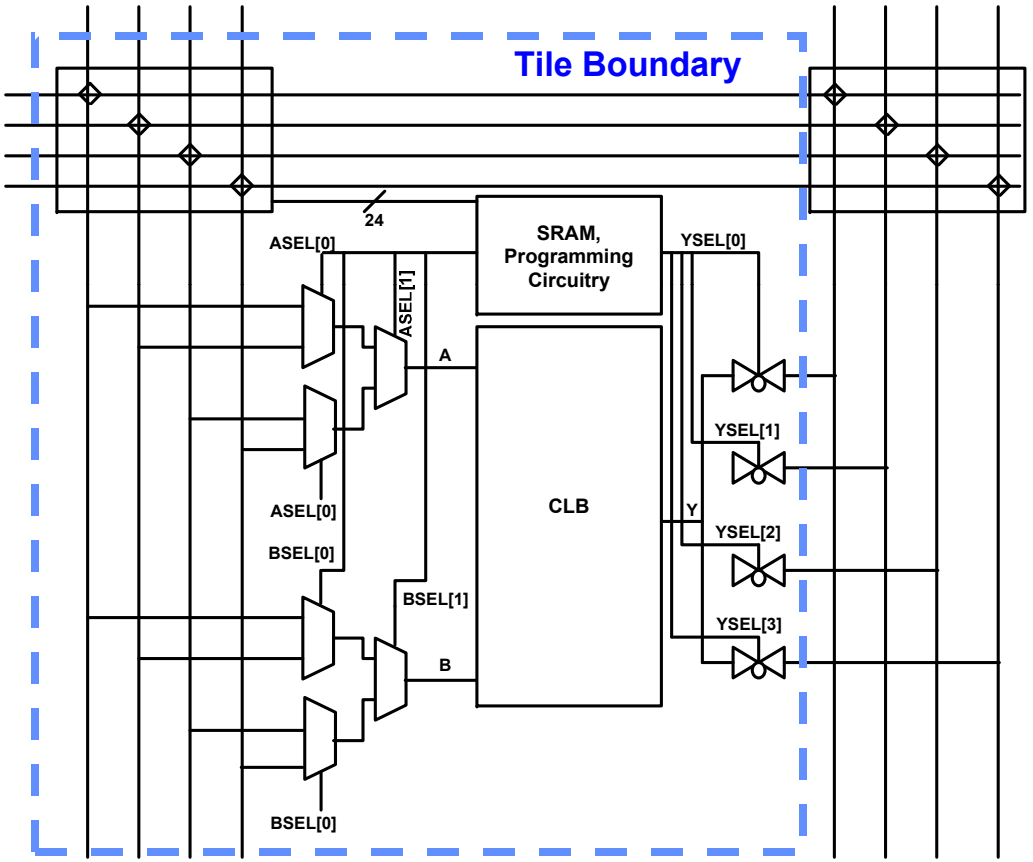
Superthreshold

Key Tradeoffs in Subthreshold Operation:

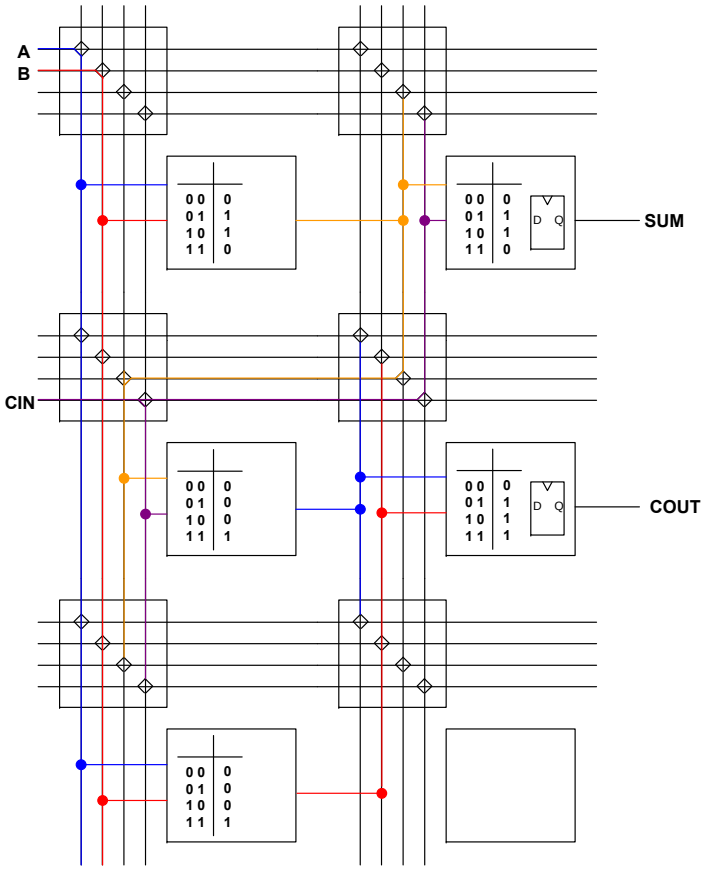
- High energy efficiency
- Large circuit delays
- High sensitivity to process variation
- Low sensitivity to transistor size
- High sensitivity to supply voltage

Prototype Tile Architecture

- 2-input CLB
- 4 routing channels
- 32 programming bits
- Flexible I/O



Prototype Tile Demonstration



Serial Adder

- Functional verification of all tile components through implementation of serial adder
- Tile average power ≈ tens of nanowatts
- Enables useful circuits on sub-mW power budgets
- Implementation of 6x6 tile array on test chip currently in fabrication at Lincoln Laboratory