NORTHROP GRUMMAN

Queueing Theory Modeling of a CPU-GPU System

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Problem/Goals

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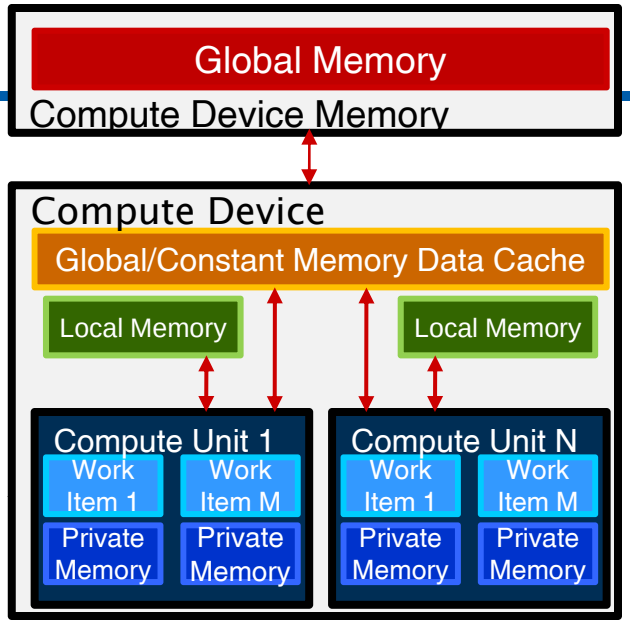
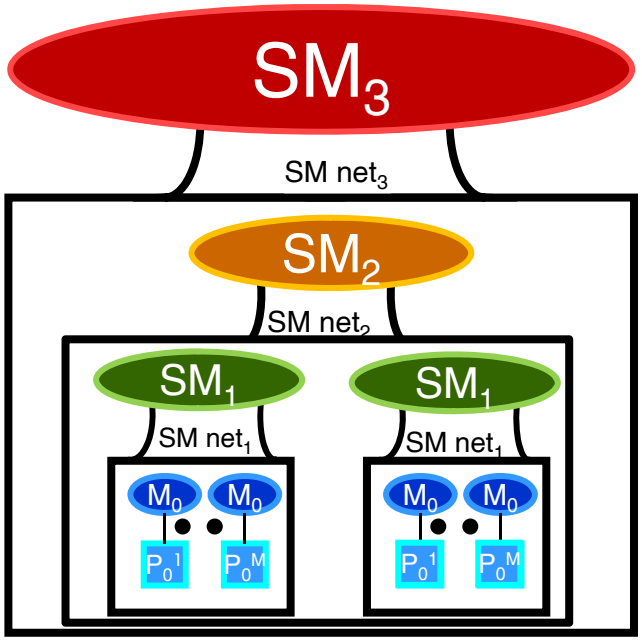
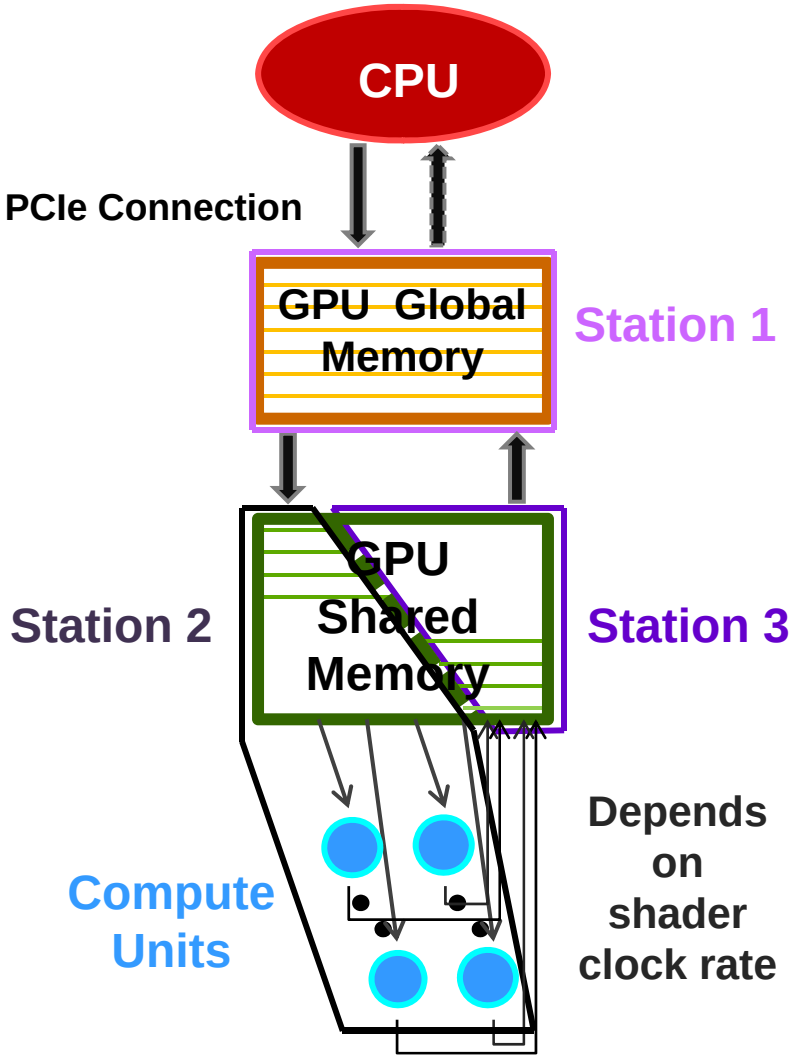
- GPGPUs have been touted as the solution to the loss of the Altivec engine in PowerPCs in the embedded space

- We set out to answer a few questions…
  - Are GPGPUs all that they are purported to be?
  - What are some of the defining architectural limitations?
  - We know they're good for graphics but how well do they map into our problem space?
  - Is there a discernable task/data level parallelism "line" defined by the architecture?
  - Is there a reasonable mathematical modeling approach to this problem?

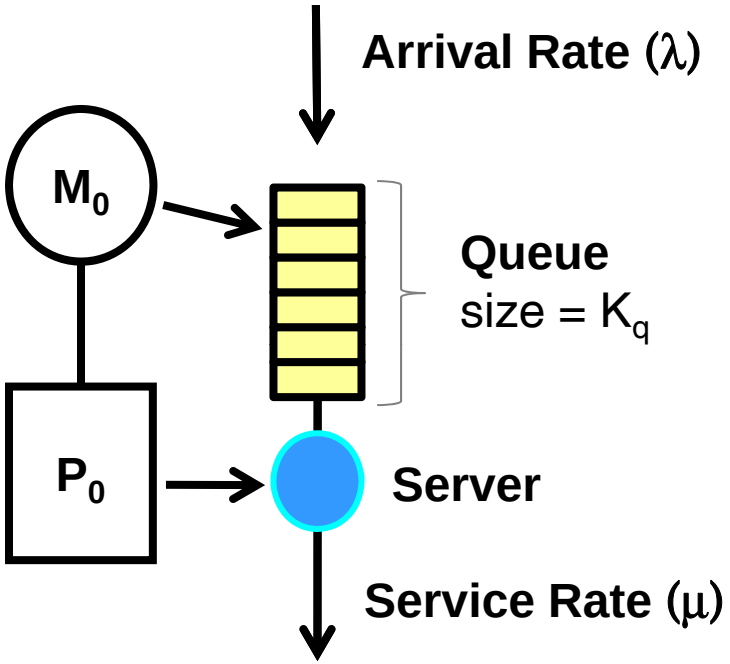
OpenCL Model, Kuck Diagram, and Queueing Model







Queueing Equations



M/M/1/K

$$P_K = \begin{cases} \dfrac{(1-\rho)\rho^K}{1-\rho^{K+1}} & (\rho \neq 1) \\ \dfrac{\rho^K}{K+1} & (\rho = 1) \end{cases}$$

$$\lambda^* = \lambda(1-P_K)$$

$$N = \begin{cases} \dfrac{\rho^*}{1-\rho^*} - \dfrac{(K+1)(\rho^*)^{K+1}}{1-(\rho^*)^{K+1}} & (\rho^* \neq 1) \\ \dfrac{K}{2} & (\rho^* = 1) \end{cases}$$

$\rho = \lambda / \mu$

K = K_q+1

ρ^*, λ^* include effects of blocking

GPGPUs for HPEC – Hype or Hope?