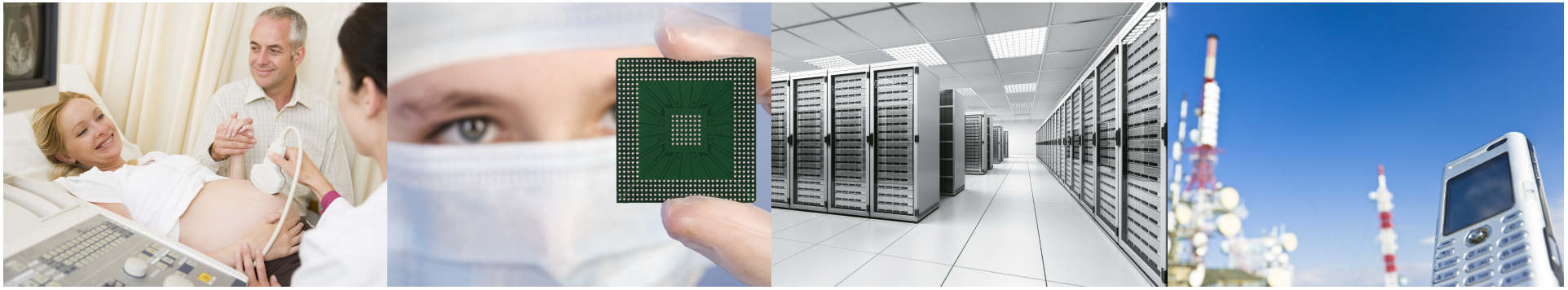

A 25 GFLOP / W Software Programmable Floating Point Accelerator

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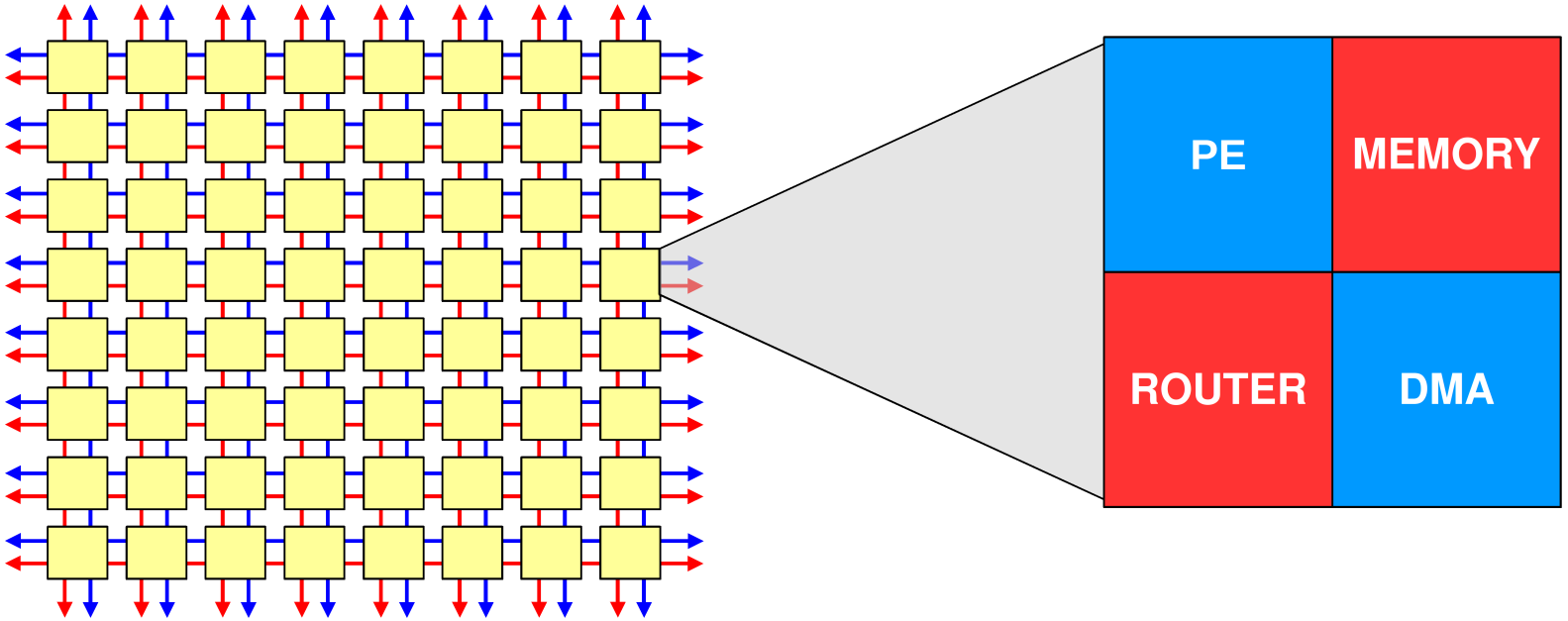
adapteva

Introduction

- Technology Trends:
  - Performance demand is out-pacing chip vendors year over year energy efficiency improvements
  - ASIC development is becoming prohibitively expensive
  - Area efficiency growing in importances as standby leakage increases exponentially at lower process geometries
  - Development times and budgets always shrinking
- There is currently no single technology that can offer an energy efficient architecture that is sufficiently flexible, easy to use, and scales well into lower process geometries.

The future of embedded computing is heterogenous/diverse computing where each device type is used for the task that it performs most efficiently.

The Epiphany Scalable Processor Fabric



- Shared Memory Architecture
- ANSI C-Programmable
- IEEE Floating Point Processing
- "Infinite" Scalability

- 50 GFLOP/W at 65nm
- 2 GFLOP per Processor Element
- 8GB/sec Inter-core BW
- 100 GFLOP/W at 28nm

Epiphany Technology Prototype

Features:

- 16 Independent Processor Cores
- 4 duplex FPGA LVDS links
- 4Mb On-chip Shared Memory
- 65nm Process Platform

Silicon Verified Performance

- 16 cores running independent programs and producing expected results
- Up to 700MHz operating frequency
- 25 GFLOP / W energy efficiency

Availability:

- Silicon in lab confirms power advantage
- Currently sampling to lead customers