An FPGA Implementation of Incremental Clustering for Radar Pulse Deinterleaving

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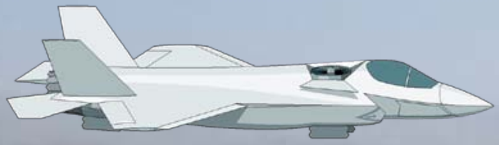
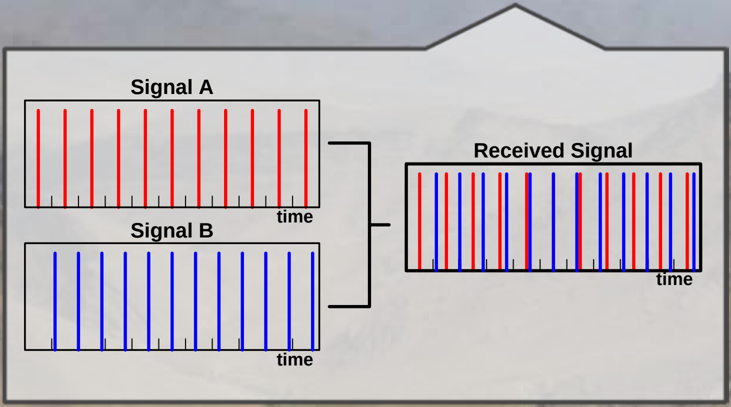
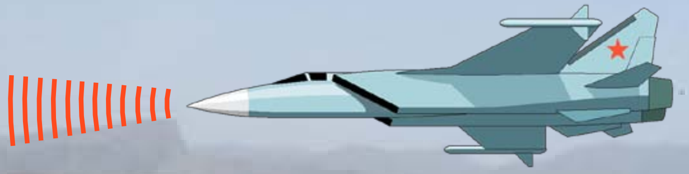
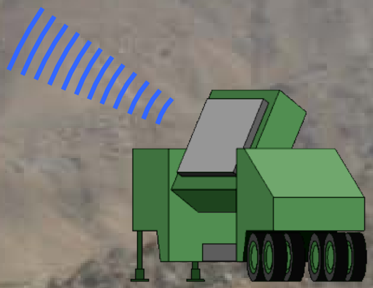
Pulse Deinterleaving for Electronic Warfare









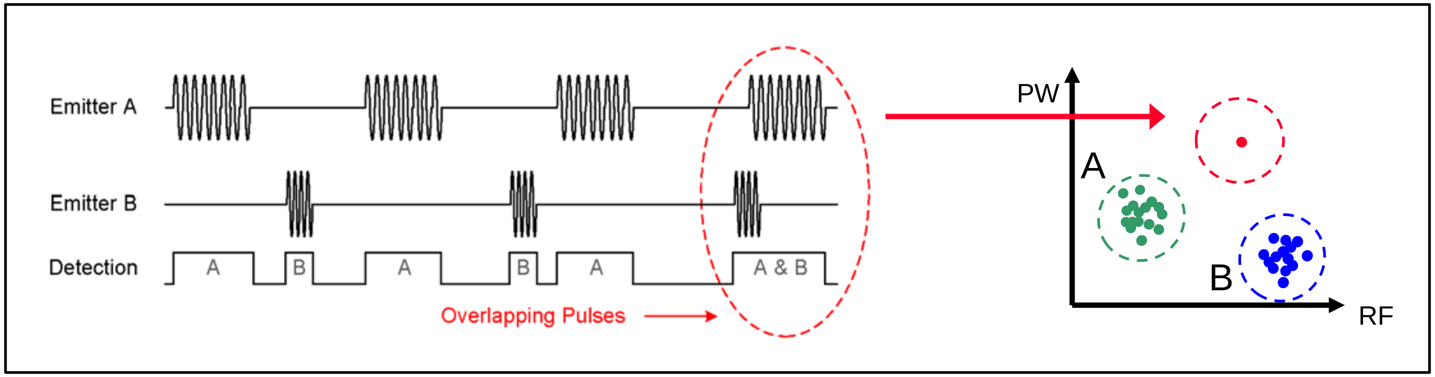
- Multiple radars in the environment can result in a single stream of interleaved pulses at a receiver
- Deinterleaving separates the combined receive signal into individual pulse streams for processing
- Dense environments can contain >1M pulses / second

Approach

- Use an incremental clustering algorithm to identify individual radar emitters

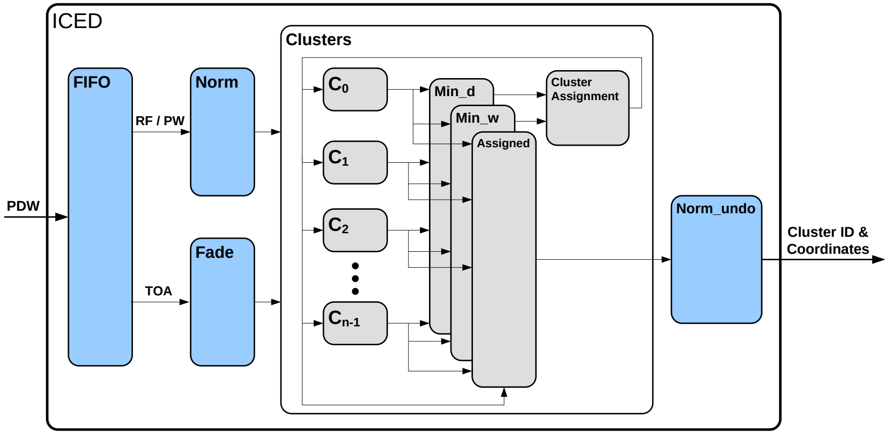
- What is Incremental Clustering?
  - Clustering partitions similar data samples into groups called clusters
  - Incremental algorithms operate in on-line (streaming) mode
    - Fast, require minimal storage, suitable for dynamic data

- Proposed Solution
  - 2-D Clustering of frequency and pulse width parameters
  - Cluster coordinates evolve over time
  - Fade mechanism emphasizes newer data and filters outliers



Implementation

- Parallelize cluster modules to minimize processing latency
  - Each cluster simultaneously determines distance to current input
  - Input is assigned to nearest cluster



- Implementation platform Innovative Integration X5-400M
  - Xilinx Virtex 5 SX95T

- Results
  - 16 cluster design yields 70% FPGA utilization
  - 420ns processing latency at 200 MHz
  - Capable of processing 2.4 million pulses per second
  - 39X speedup over software implementation