Nonlinear Equalization Processor IC for Wideband Receivers and Sensors

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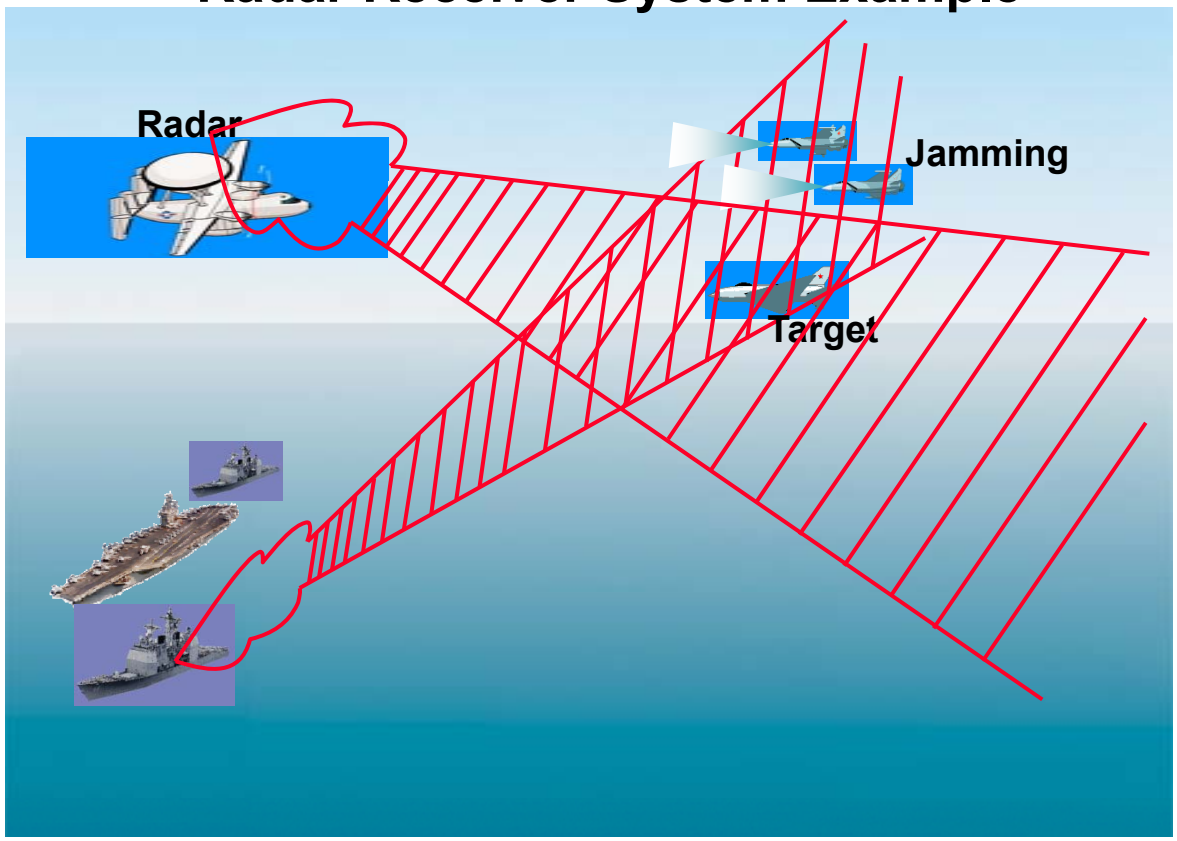
Outline

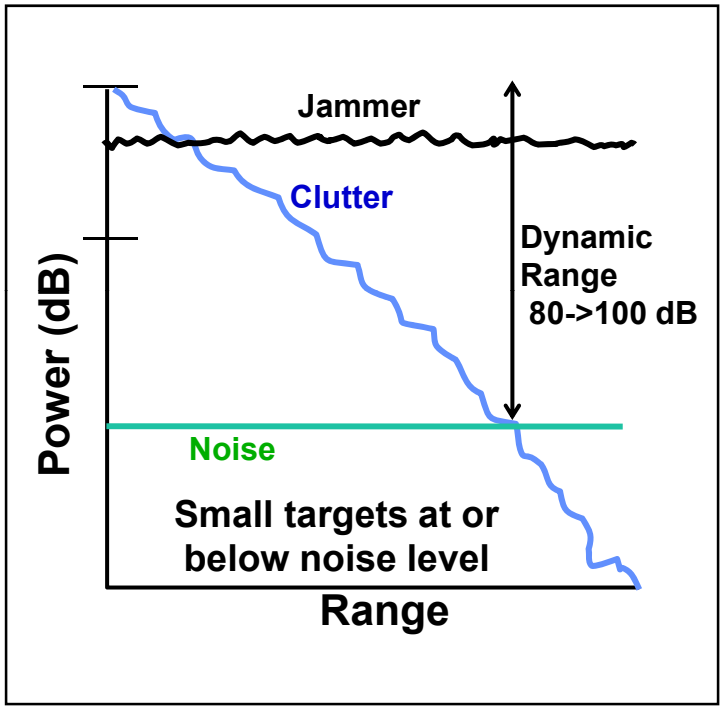
- Introduction
  - Nonlinear Equalization (NLEQ) applications
  - NLEQ program objective
- NLEQ processor architecture
- VLSI NLEQ processors
- Performance demonstration results
- Summary

High Dynamic Range Requirements for Military and Commercial Sensor Systems

Radar Receiver System Example

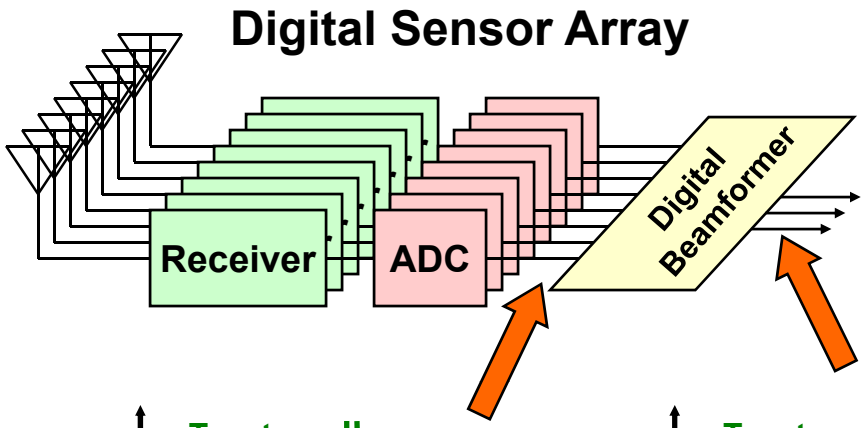


Radar Receiver System Interference + Noise Environment

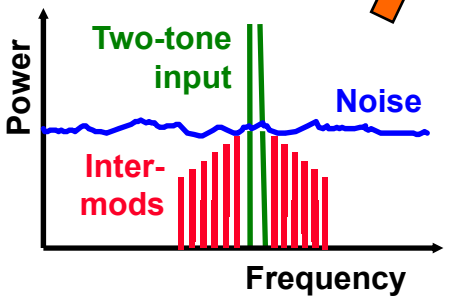


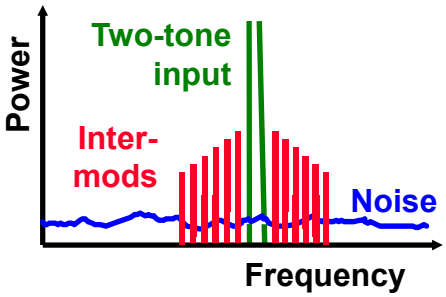
- Radar, ELINT, SIGINT, Comm receiver systems must support high dynamic range operation
  - To detect small targets/signals in interference/clutter environment
  - High signal-to-noise ratio and linearity required

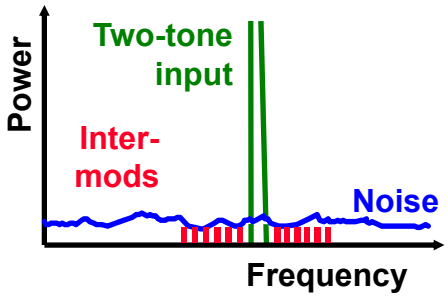
Linearity Concerns in Highly Digitized Arrays and Frequency Channelized Systems

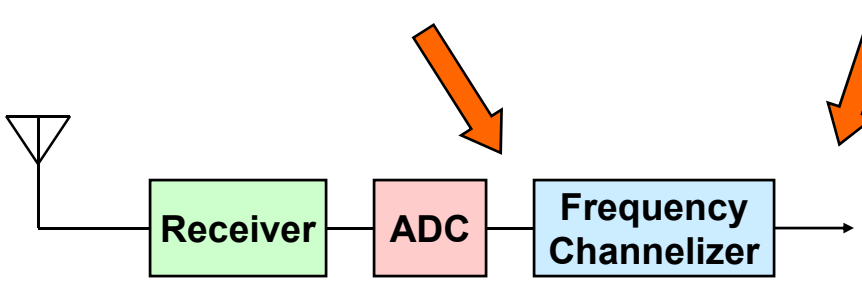


- Digital beamforming and frequency channelization increase in-band signal-to-noise ratio (SNR)
- Non-linearity generated spurs and intermods can interfere with small signal detection

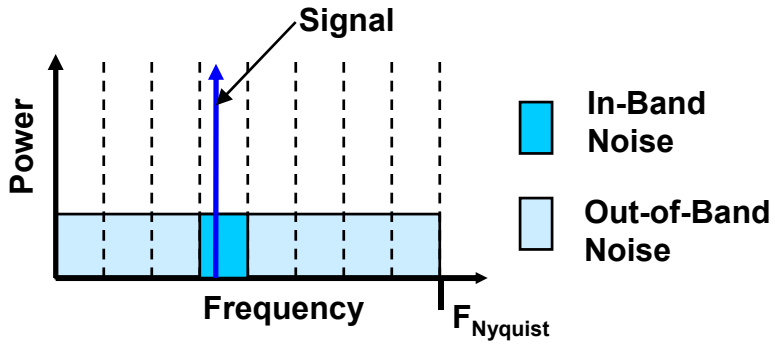




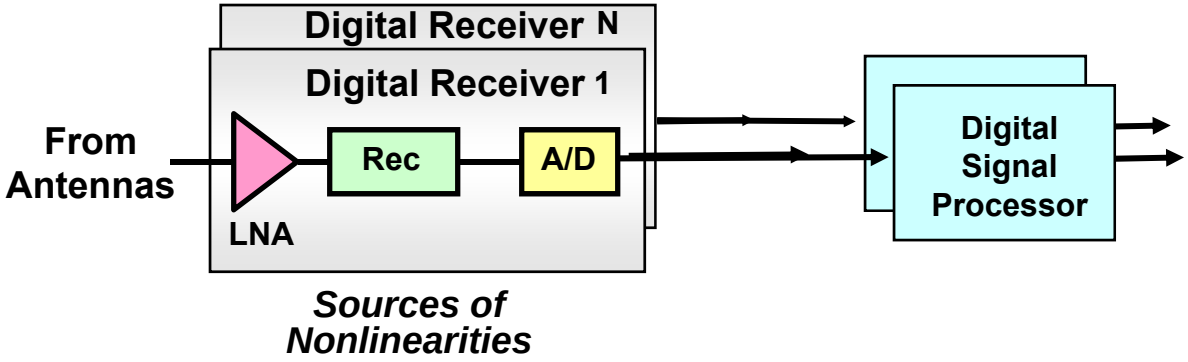




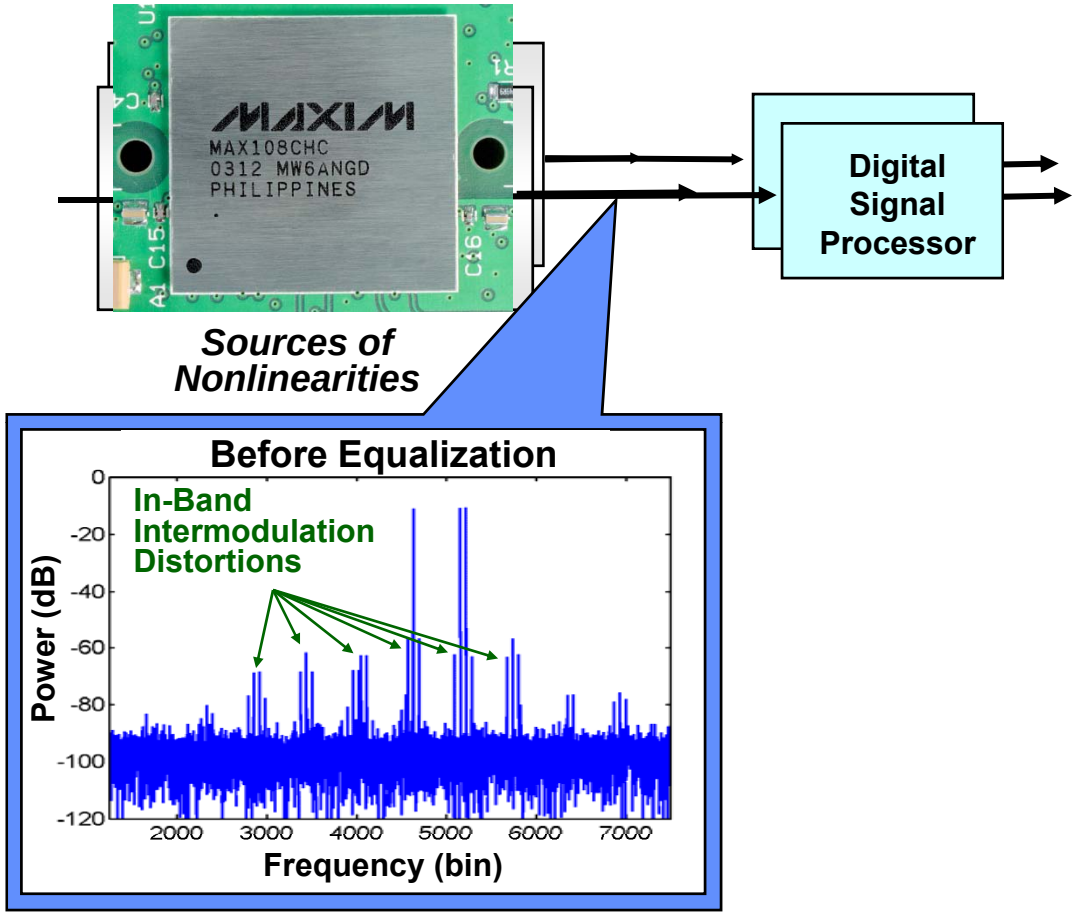
Frequency Channelized Receiver



Nonlinear Equalization (NLEQ)



Nonlinear Equalization (NLEQ)



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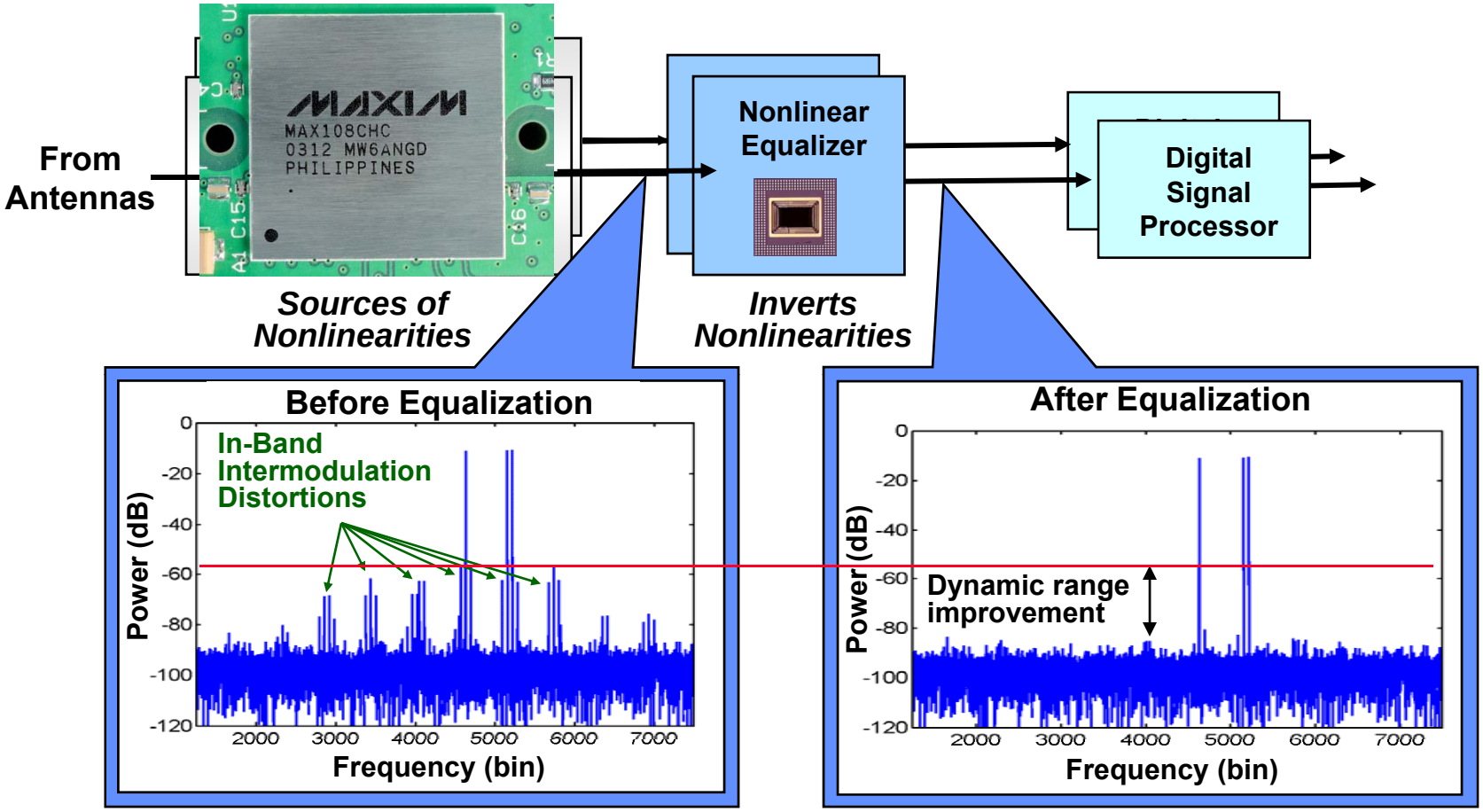
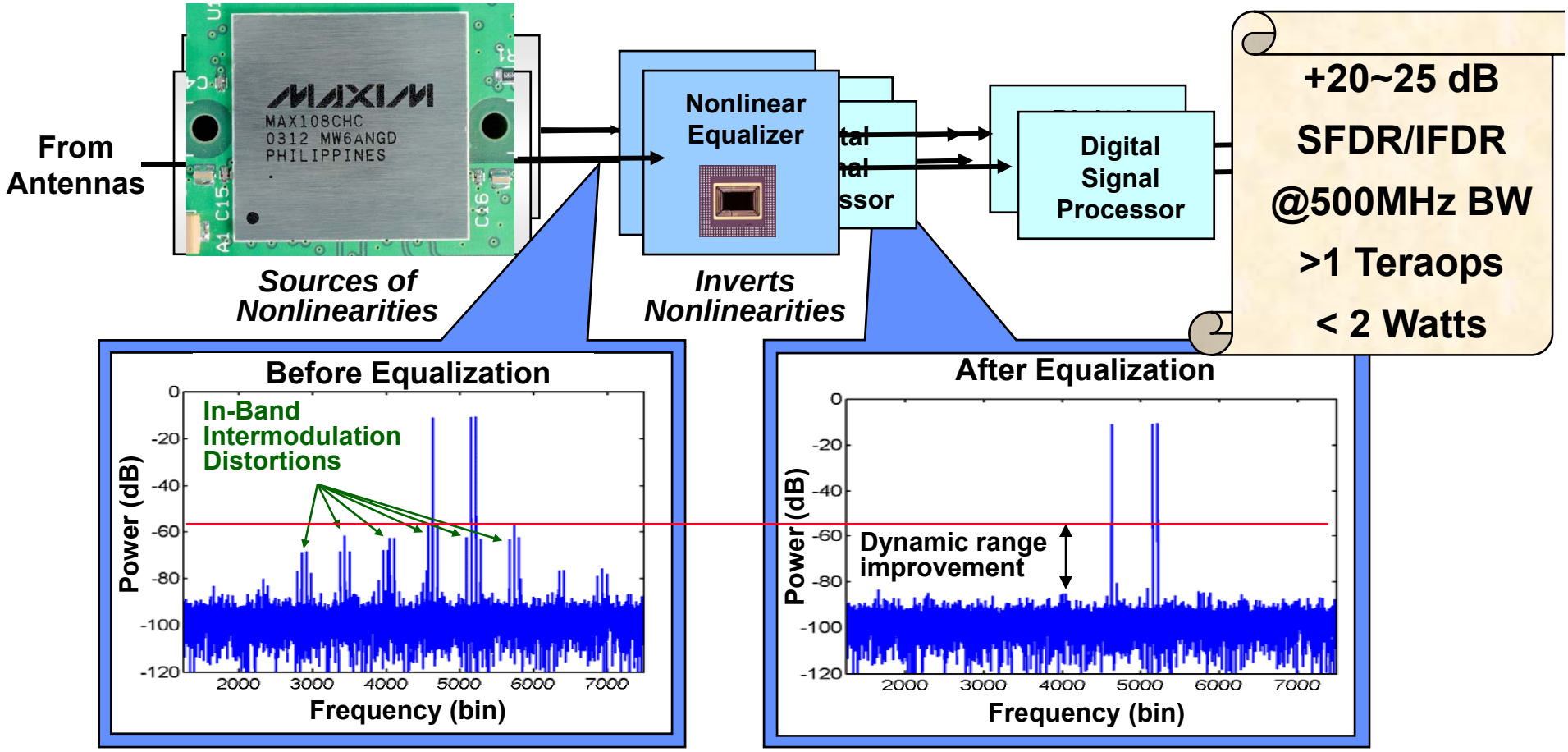


Nonlinear Equalization (NLEQ)

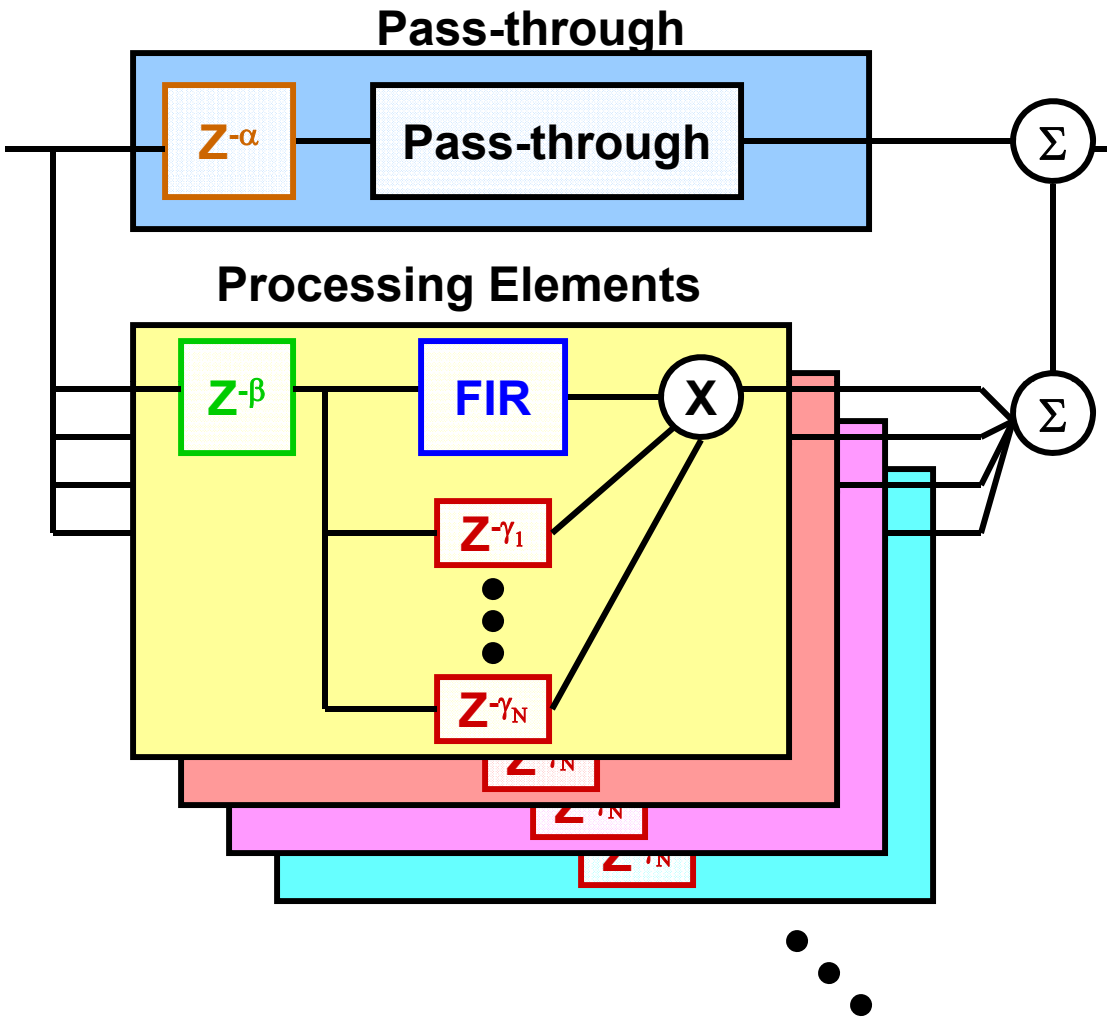


- Nonlinear equalizer processor can reduce nonlinear distortion levels in analog and mixed signal circuitry
- Equivalent to having devices 10-20 years ahead of their time

Outline

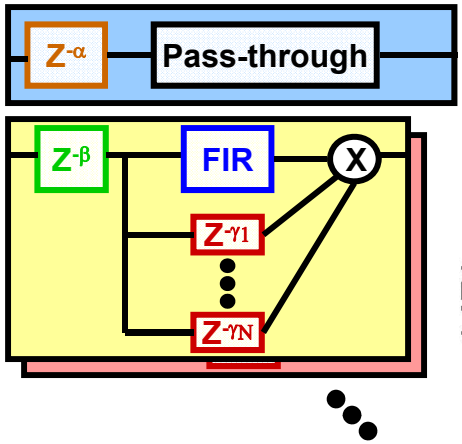
- Introduction
- NLEQ processor architecture
  - Processor architecture
  - Architecture optimization
- VLSI NLEQ processors
- Performance demonstration results
- Summary

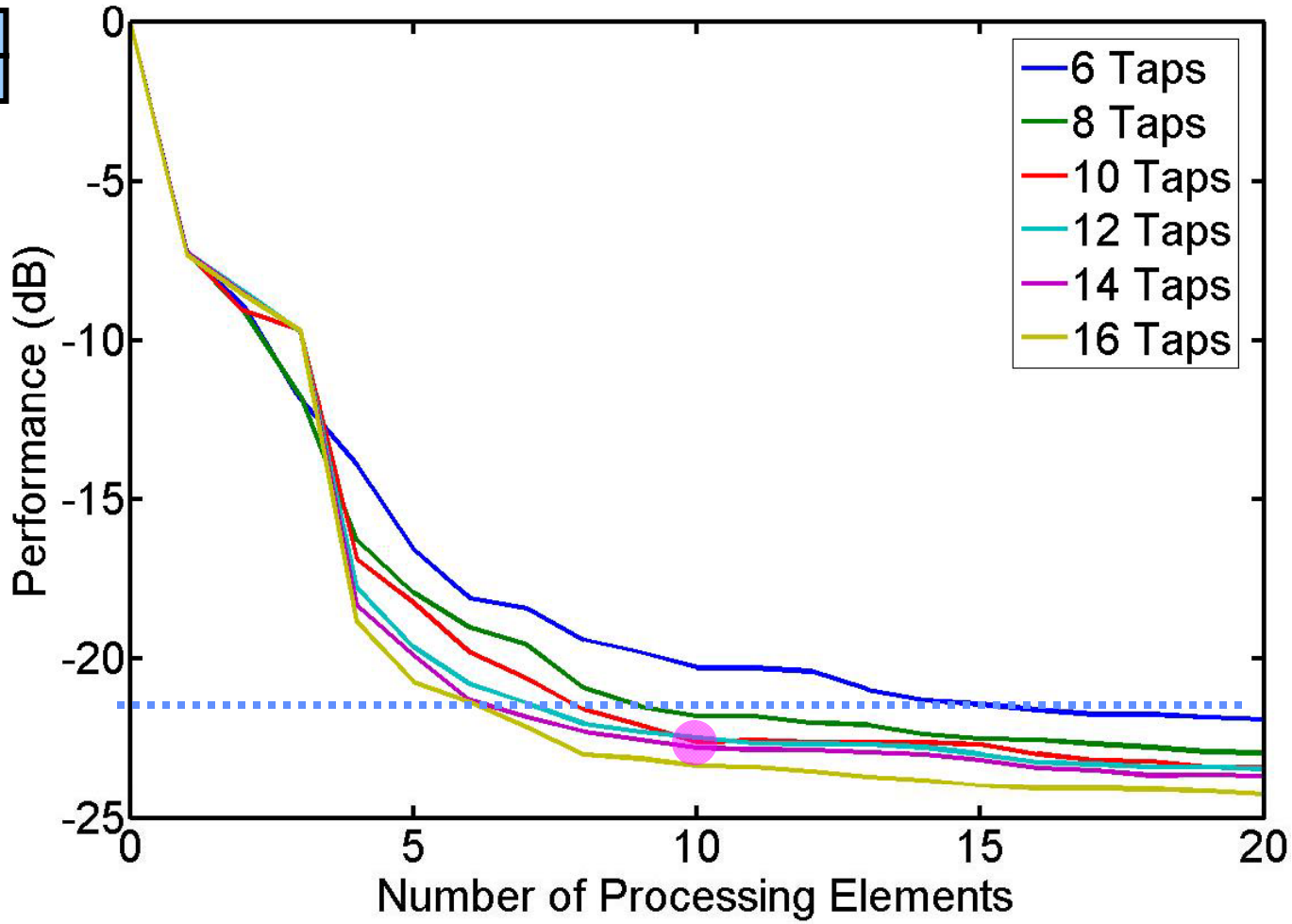
NLEQ Polynomial Nonlinear Filter Architecture



- Parameters to optimize:
  - Number of processing elements
  - Polynomial orders of processing elements
  - Number of taps
  - Delay values

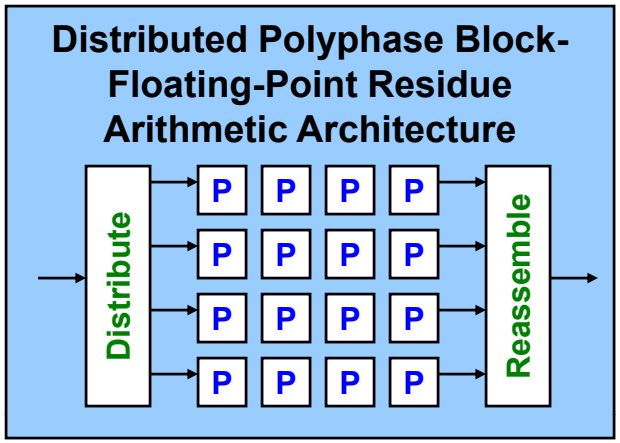
Wideband NLEQ Processor Parameter Optimization

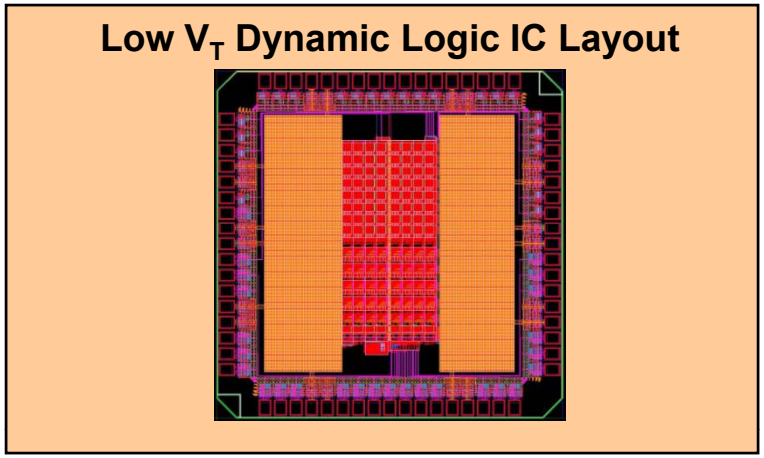




- **Parameter selection**
  - **10 filters, 10 taps, 0-3 tap delay, 0-3 group delay, 3 pass through delay**

Parallel NLEQ Processor Architecture Optimization





Design ⇄ Feedback (Performance Trades)

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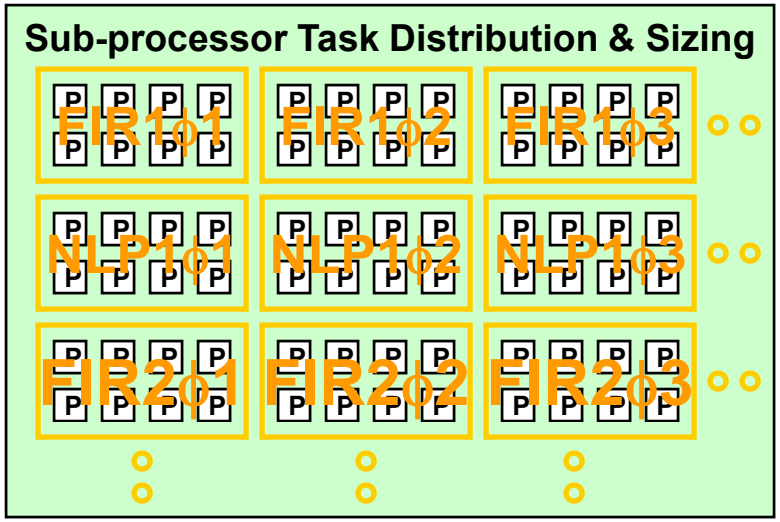
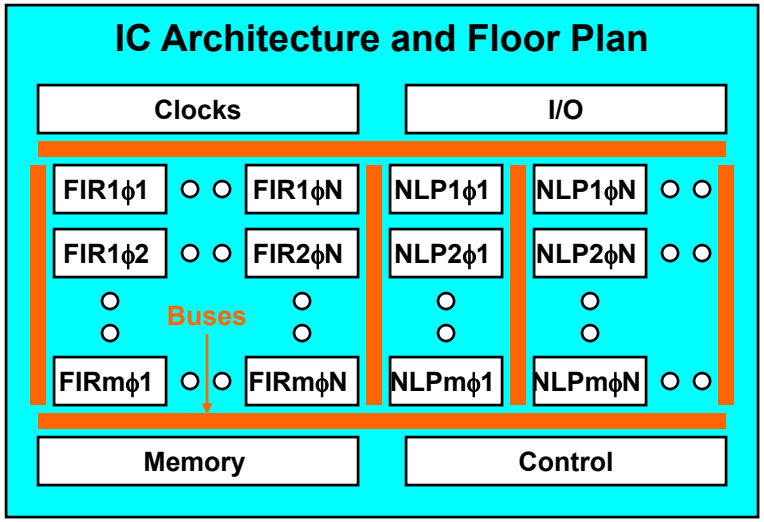
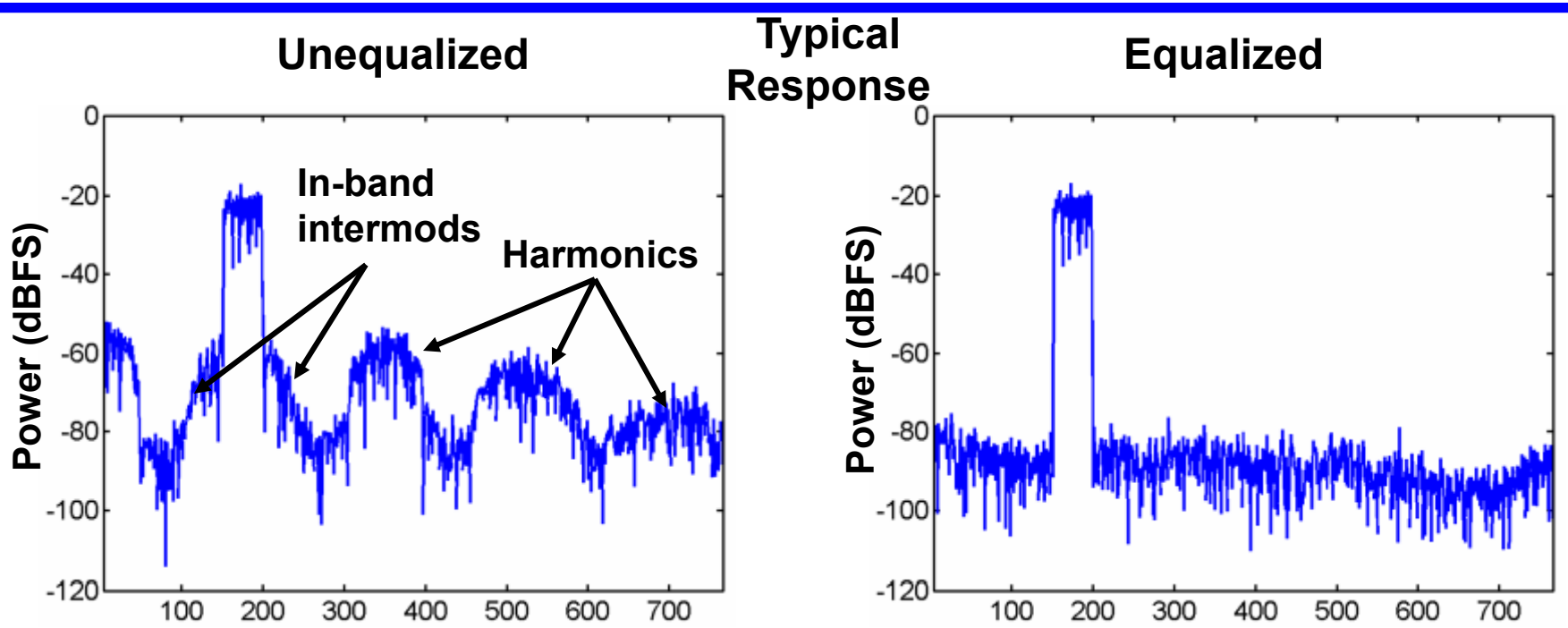


Design ⇄ Feedback (Routing Efficiency)

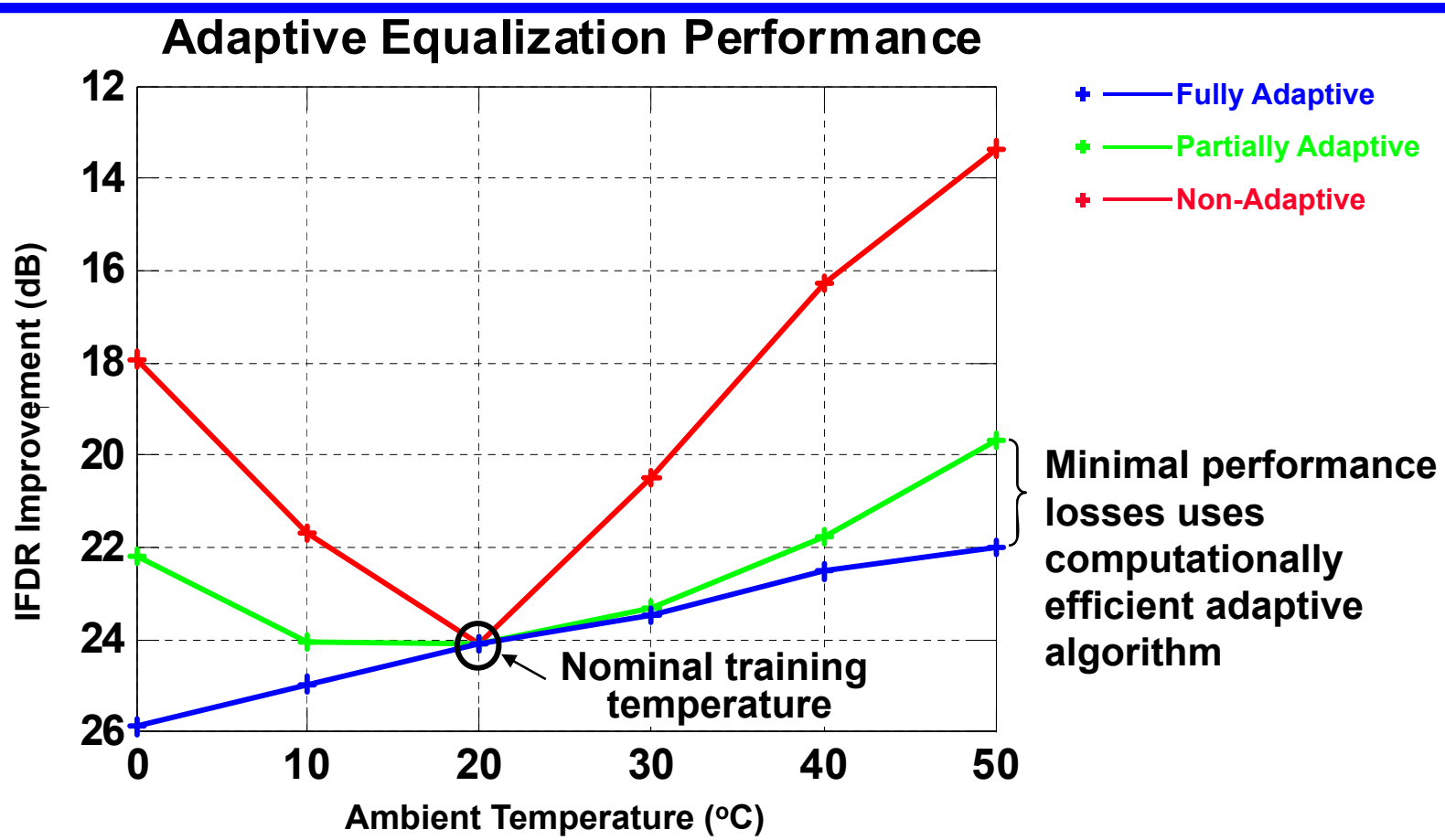


Measured Results: PRN Signal with Amplifier & ADC Distortions



- Non-tonal signal experiment parameters
  - Amplifier in saturation region
  - Max 104 included in testbed system
  - Pseudo-Random Noise (band-limited) input waveform
- Greater than 25 dB dynamic range improvement
  - In-band signal component is not distorted by the equalizer

NLEQ Adaptive Equalization Performance

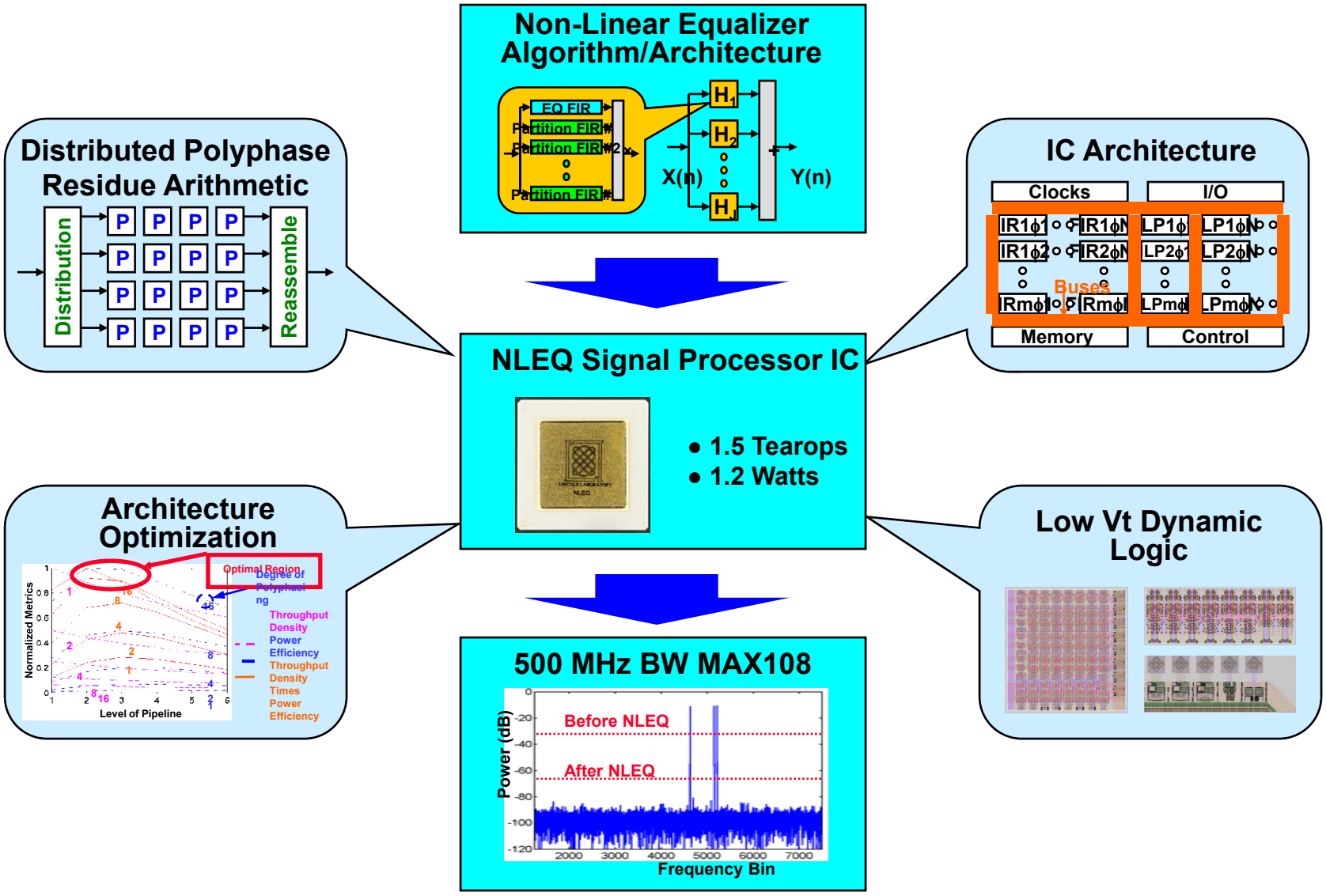


- Characterized Max 108 device sensitivity to changes in temperature
- Applied adaptive equalizations
  - Fully temperature adaptive approach achieve good performance
  - Partially adaptive approach can achieve similar performance with much higher computational efficiency

Outline

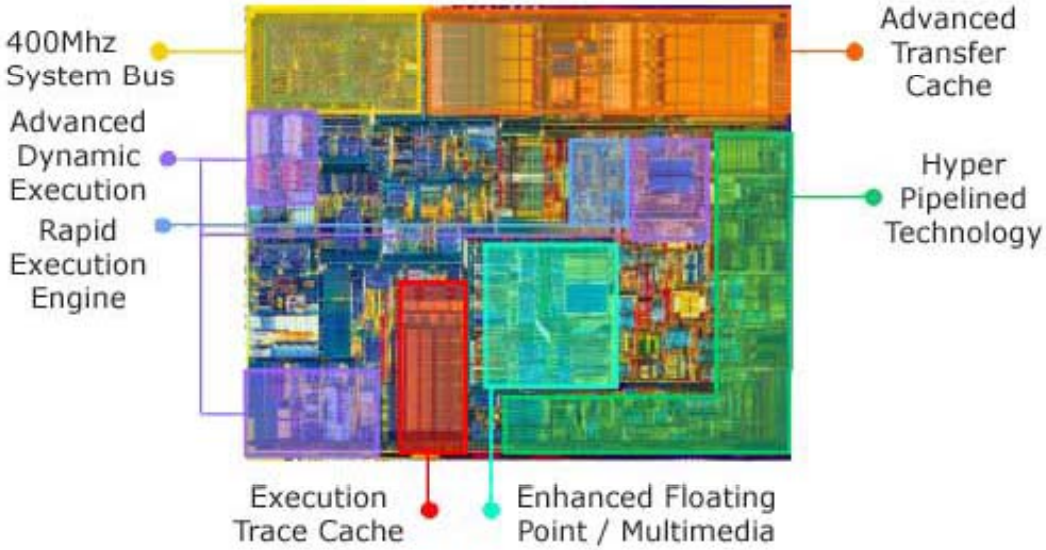
- Introduction
- NLEQ processor architecture
- VLSI NLEQ processors
  - Enabling technologies
  - NLEQ4000 ultra-wideband processor IC
  - NLEQ500 wideband processor IC
- Performance demonstration results
- Summary

Nonlinear Equalizer Processor IC Development Process



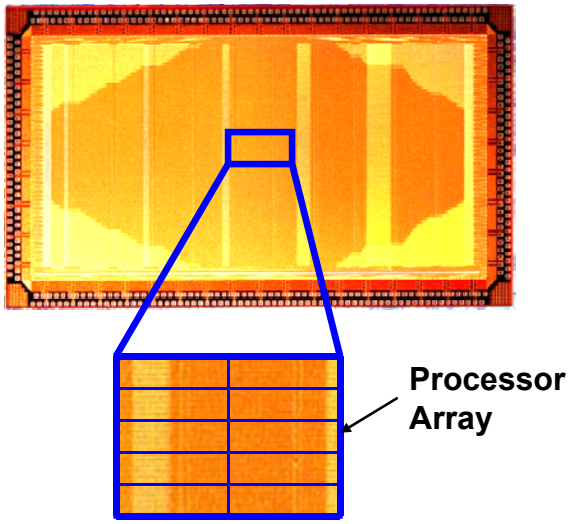
Architectural Comparison of Pentium 4 and MIT LL Processor Dies

Pentium 4 Die



- Single processor
- Multiple caches and memory bus
- Only core runs at high speed
- General purpose processing
- Large design team (>100)

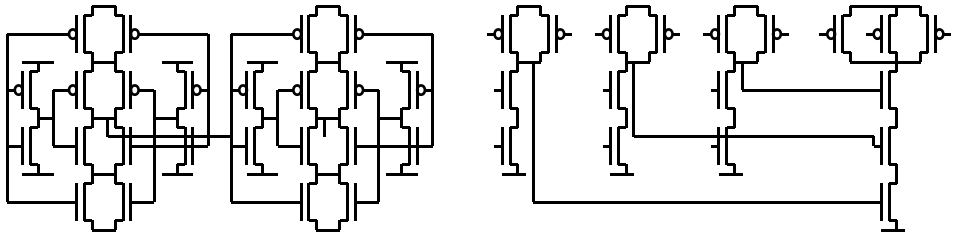
MIT LL Processor Die

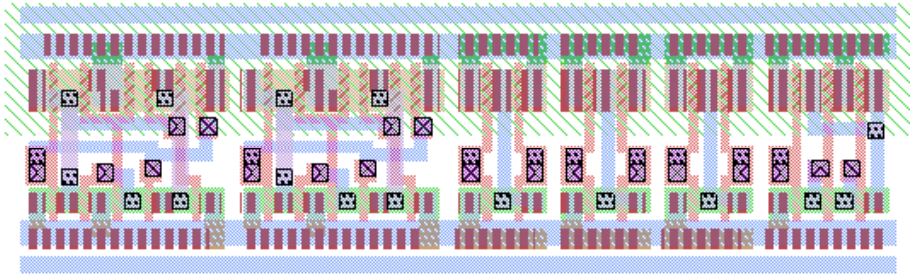


- 1000's of parallel processors
- Local memory only
- Entire die runs at high speed
- Signal processing functions
- Small design team (<10)

Custom CMOS Circuit Design

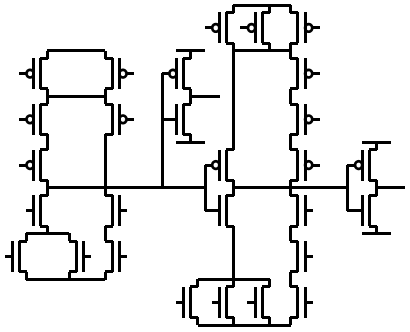
Standard Cell Full Adder





- Pre-designed logic gates only
- Automatic device placement and routing
- Large area and power consumption

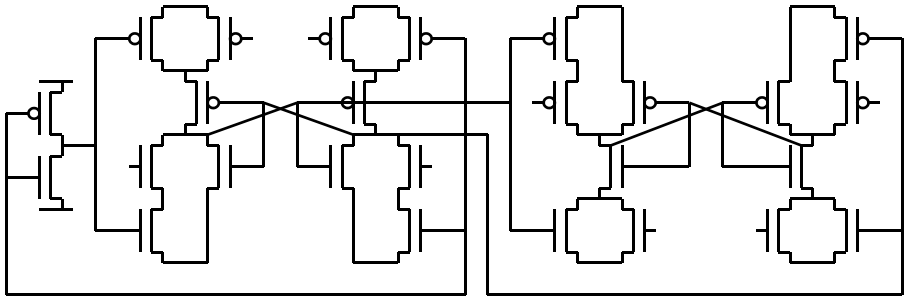
Full Custom Full Adder

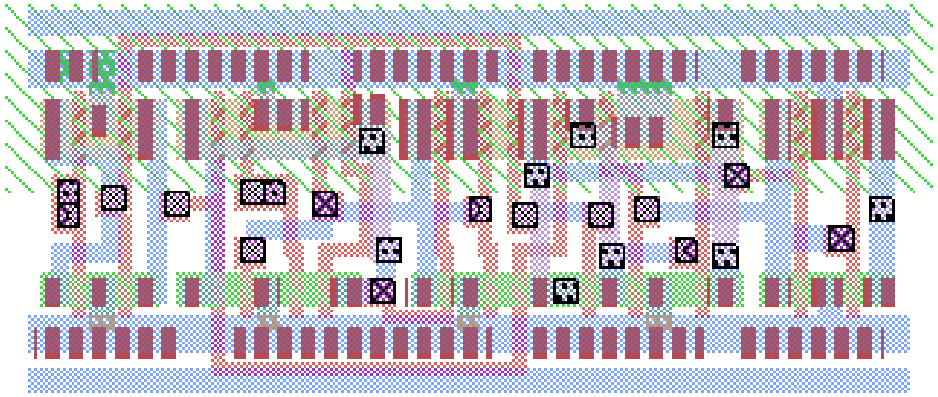


- Custom logic and devices sizing
- Manual device placement and interconnect
- Small area and power consumption

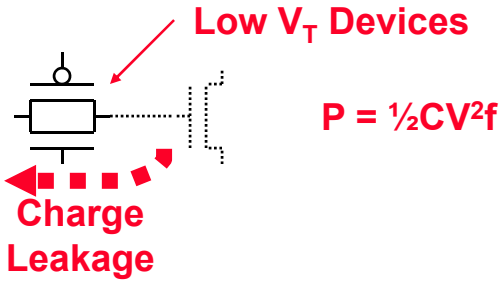
Full Custom Low Threshold Voltage (V_T) Dynamic Logic Circuits

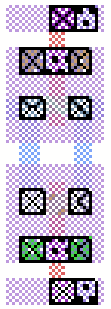
Standard Cell Static Register





Full Custom Dynamic Register





Design Techniques

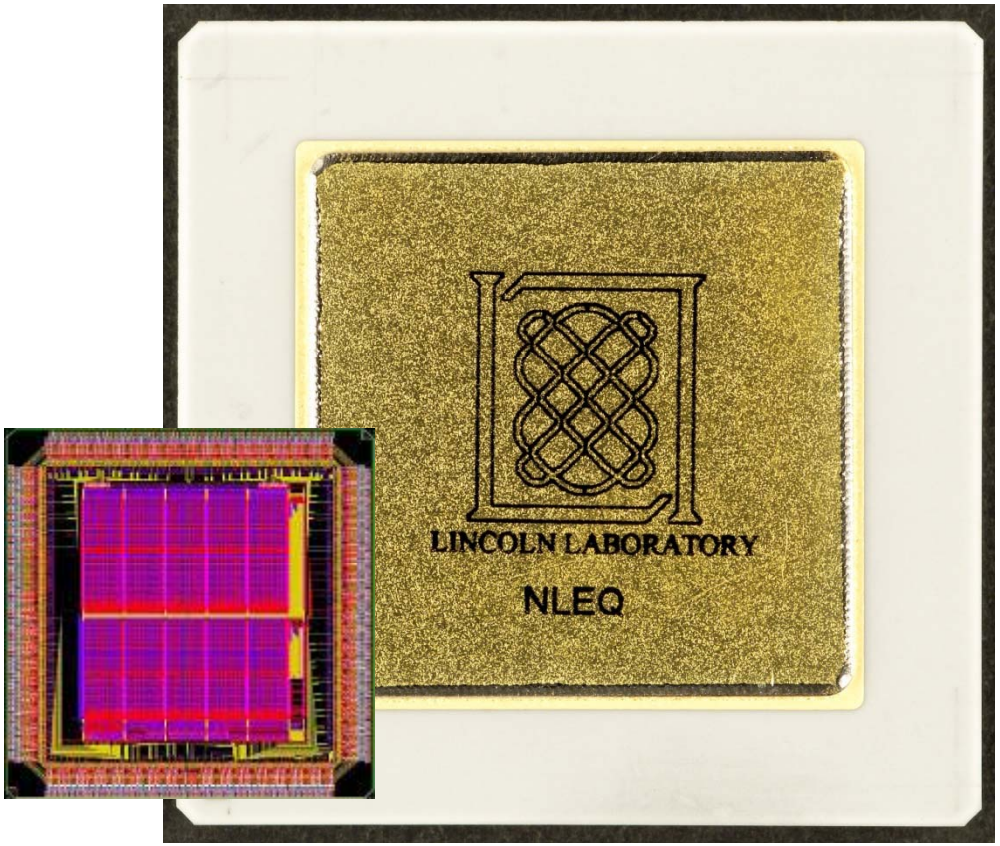
- Frequent refresh
- Bypass capacitors
- Signal isolation
- Guard rings
- Robust circuits

- Logic based computation and storage
- Many devices
- Large area and power consumption

- Charge based computation and storage
- Fewer devices
- Small area and power consumption

NLEQ4000 Processor IC

Wideband NLEQ Processor IC Layout And BGA Package

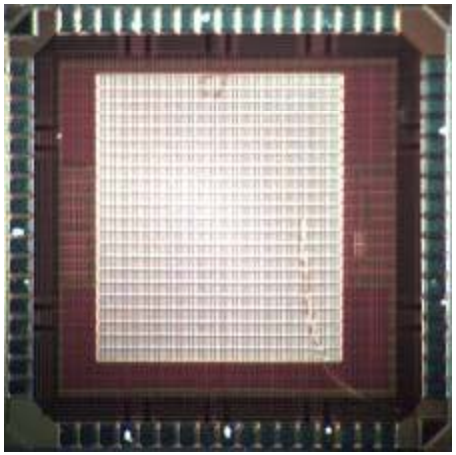


- Up to 4,000MSPS
- Selectable bit widths
  - Up to 12 bits input
  - Up to 16 bits output
- LVDS and CMOS I/O
- Programmable coefficients
- Block floating point residue arithmetic

Parameter (IBM 0.13um)	Core	Chip
Die Size	2.6 mm x 3.3 mm	6mm x 6mm
Power @1500MSPS	266mW	453mW
Power @4000MSPS	706mW	1219mW

NLEQ500 Processor

IBM 0.13µm Die



BGA

- Up to 500MSPS
- Selectable bit widths
  - Up to 18 bits input
  - Up to 22 bits output
- Low voltage CMOS I/O
- Programmable configuration and coefficients
- Block floating point residue arithmetic
- Yield 14/15 for LowVt and 14/15 for RegVt

Parameter (IBM CMOS 0.13um)	Core	I/O	Chip
Size	0.65mm x 1.4mm	N/A	2.2mm x 2.2mm
Power @100MSPS (Vdd=0.6V)	6mW	19mW*	25mW*
Power @500MSPS (Vdd=1.2V)	122mW	121mW*	243mW*

*With 50 Ohm Load Termination

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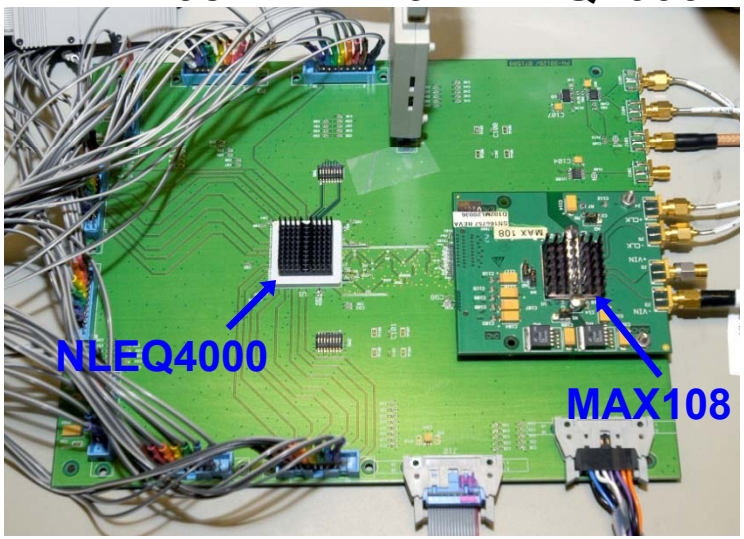
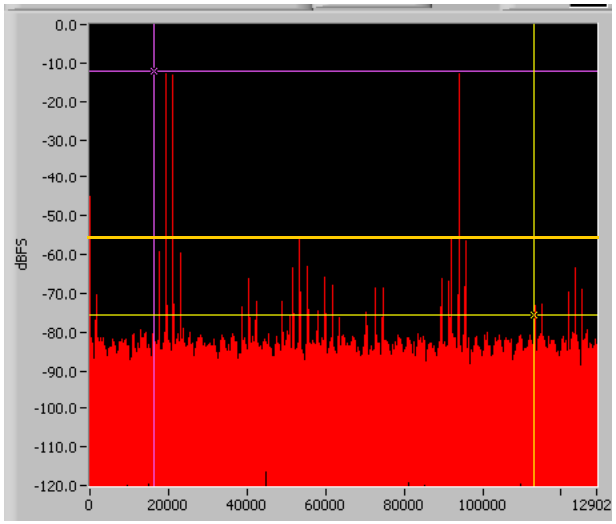
MAX108 Demonstration Results

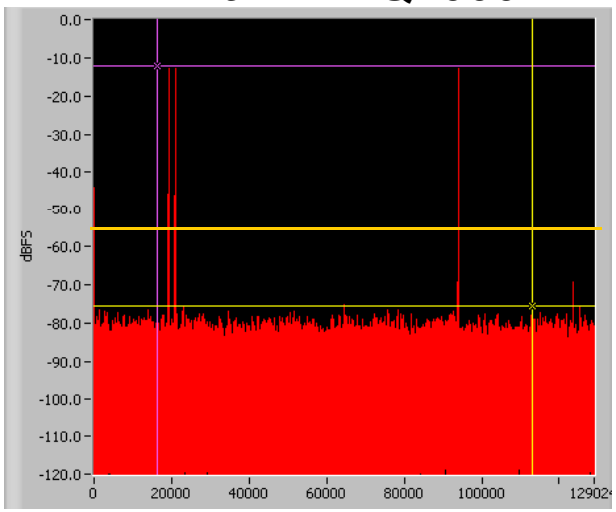
MAX108 ADC with NLEQ4000



Without NLEQ4000

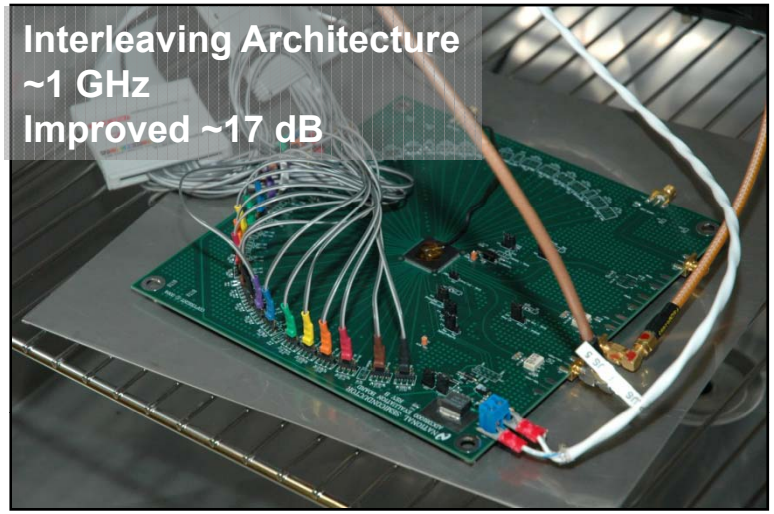


With NLEQ4000

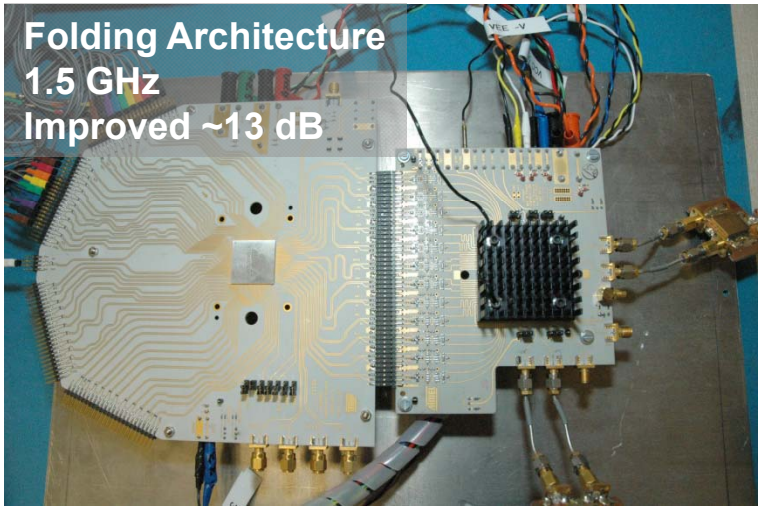


- ~21 dB linearity improvement demonstrated with NLEQ4000 IC at 1.5GSPS

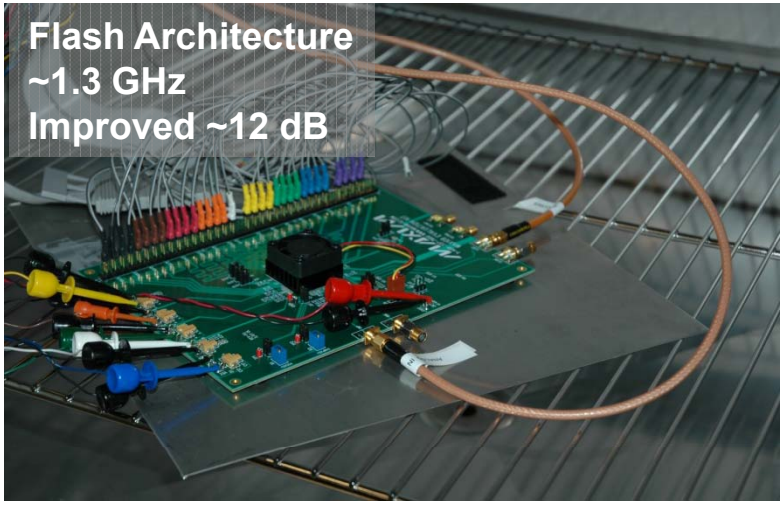
Measured NLEQ Performance Improvement for Other ADCs



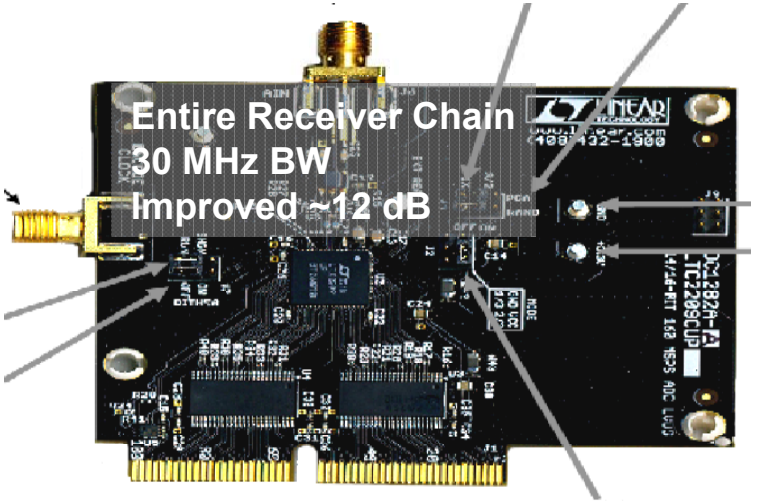
National 81000



Atmel AT84AS008

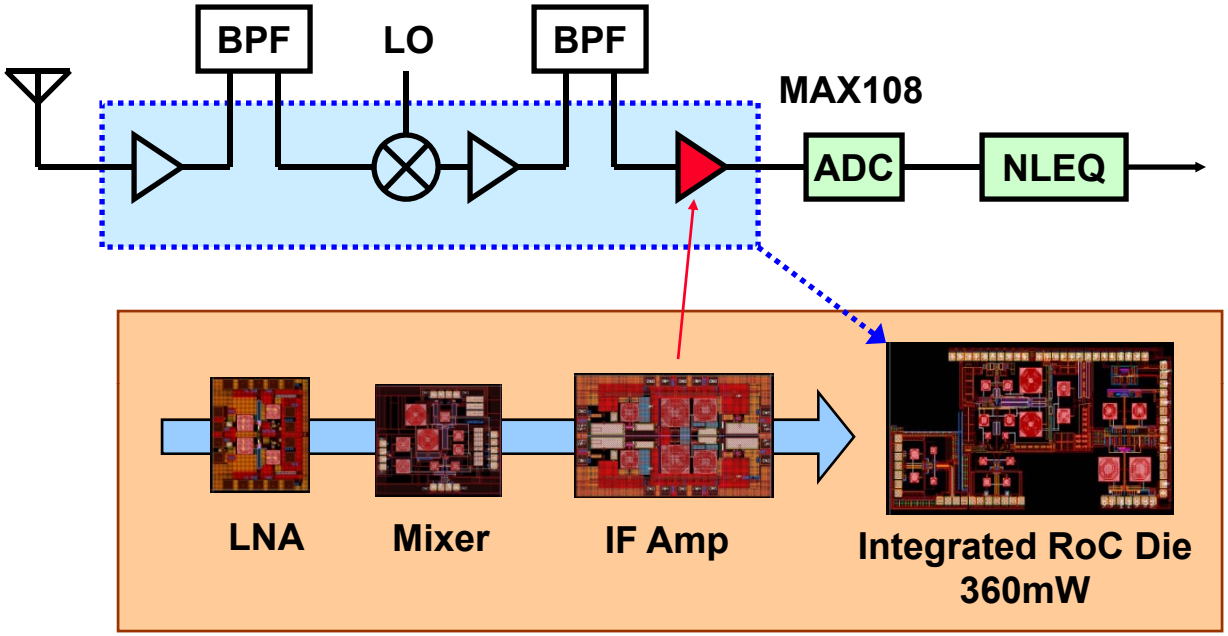


Maxim 109

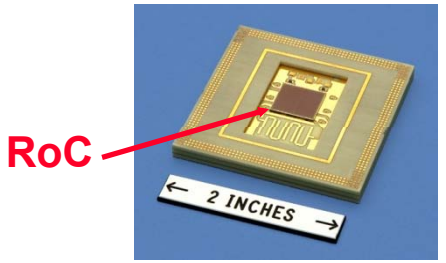


LTC 2209

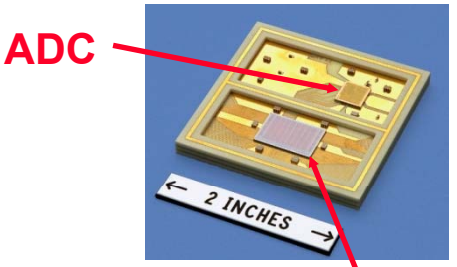
X-Band Receiver-on-Chip (RoC) Development Based on NLEQ DSP



Top View



Bottom View



- Linear dynamic range limited by the final IF amplifier
  - NLEQ DSP to linearize the amplifier and ADC
- High performance and low power achieved with new analog/digital co-design paradigm
- Single die receiver implementation being explored

Summary

- Linearity enhancement required by DoD/commercial sensor/receiver applications
  - Phased array sensors/receivers
  - Frequency channelized sensors/receivers
- MIT LL has developed high-throughput low-power nonlinear equalization signal processor ICs
  - Massively parallel systolic architecture
  - Polyphase distributed arithmetic processing
  - Block floating point residue number arithmetic
  - Full custom low-threshold-voltage dynamic logic
- Successful demonstration results
  - >20 dB linearity improvement
  - NLEQ4000
    - Up to 4GSPS, <1.25W
    - Up to 12 bit ADCs
  - NLEQ500
    - Up to 500MSPS, <0.25W
    - Up to 18bit ADCs