

# Nonlinear Equalization Processor IC for Wideband Receivers and Sensors

<sup>1</sup>William S. Song, <sup>1</sup>Joshua I. Kramer, <sup>1</sup>James R. Mann, <sup>1</sup>Karen M. Gettings, <sup>2</sup>Gil M. Raz, <sup>1</sup>Joel I. Goodman, <sup>1</sup>Benjamin A. Miller, <sup>1</sup>Matthew Herman, <sup>1</sup>Thomas B. Emberley, <sup>1</sup>Larry L. Retherford, <sup>1</sup>Albert H. Horst  
<sup>1</sup>Lincoln Laboratory, Massachusetts Institute of Technology, Lexington, MA 02420  
{song, joshua.kramer, jmann, karen.gettings, jgoodman, bamiller, mherman, temberley, retherford, horst} @ll.mit.edu  
<sup>2</sup>GMR Research & Technology, Inc., 1814 Main Street, Concord, MA 01742-3819  
raz@gmrtech.com

## Introduction

Many commercial and military receiver and sensor applications such as communications, radar, signal intelligence, and electronic warfare systems require high linear dynamic range to detect small signals in presence of high level interference signals such as interference, clutter, and jammer. High level interference signals cause generation of nonlinear spurious signals in receivers and analog-to-digital converters (ADCs) which can interfere with small signal detection. For important classes of applications including digital phased arrays and digitally channelized receive systems, linearity of the radio frequency (RF) and ADC is much more important than the signal to noise ratio (SNR) for enhancing system dynamic range. This is because digital signal combining in digital arrays and digital frequency channelization processes enhance SNR, but do not suppress the nonlinear spur levels compared to the signal levels.

## Nonlinear Equalization Algorithm

Digitally implemented nonlinear equalization (NLEQ) algorithms can suppress these undesired spurs while preserving the signals to be detected. MIT Lincoln Laboratory (MIT LL) and GMR Research and Technology have collaborated to develop algorithms capable of linearity enhancement over a wide spectrum of instantaneous bandwidths from 1 MHz to 500MHz [1, 2]. The Figure 1 illustrates the measured performance improvements obtained when the NLEQ is applied to Maxim's MAX108 ADC operating at 1.5 billion samples per second (GSPS) with input passband of 500 MHz. The Figure 1a shows the frequency-domain response of MAX108 with 3-tone analog input without nonlinear equalization. The Figure 1b shows 21-dB improvement obtained over the 500 MHz receiver passband using the NLEQ algorithm. This linearity enhancement would be significant for many communications receiver and sensor applications. In linearity driven digital phased array or digitally frequency channelized systems, the 21 dB linearity improvement can correspond to a 21 year advance given historical commercial ADC dynamic range improvement rate of approximately 1 dB per year. With narrower passband signal bandwidths, linearity improvement up to 30 dB has been demonstrated. The NLEQ algorithm has also demonstrated significant linearity enhancements when

applied to other ADCs and complete receiver systems that included RF receivers and ADCs. Further experiments demonstrated that the NLEQ approach is robust with respect to temperature variation as long as the linearity enhancement coefficients are updated according to the temperature.

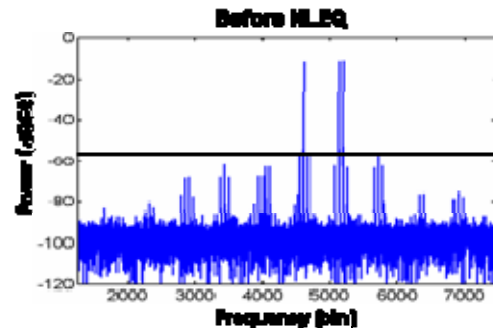


Figure 1a: MAX108 3-Tone Data without NLEQ.

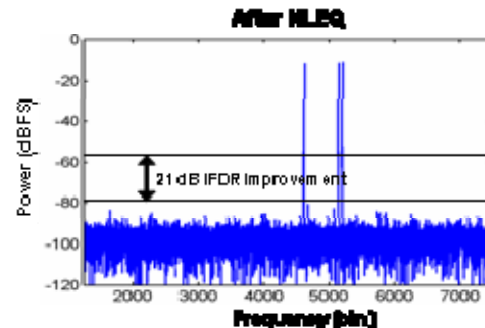


Figure 2b: MAX108 3-Tone Data with NLEQ.

## VLSI Implementation

Implementing the NLEQ algorithms on wide bandwidth (500MHz, 1.5-GSPS) signals in real time can require close to a trillion arithmetic operations per second (TeraOPS). In addition, for many applications that are limited in size, weight, and power, it is desired that such nonlinear signal processor to be implemented on a single IC and consume no more than a watt or two. To meet the challenge, MIT LL has developed a specialized signal processor chip based on systolic distributed block floating point residue arithmetic and full custom low threshold voltage dynamic logic circuitry. The processor is heavily based on systolic architecture [3] where identical processing elements are used with nearest neighbor communications. Using relatively small identical processing elements in the array

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architecture enables high level of performance optimization. Small processor size enables high level optimization in clock rate, computational throughput, small die area, and low power consumption with reasonable design effort. The nearest neighbor communication enables high-speed low-power communication necessary to keep up with very high data rates.

In order to reduce the algorithmic unit complexity, block floating point arithmetic is used instead of floating point arithmetic. The numbers of mantissa and exponent bits were varied depending on the signal processing functions in order to maximize the throughput density and minimize the die area and power consumption while keeping the algorithm performance nearly identical to the floating point arithmetic. In order to expand the numerical dynamic range with minimum hardware, the residue number arithmetic was used where large dynamic ranges were required. In order to push the performance boundary even further, many of the architectural features were co-optimized with NLEQ algorithm itself by multi-disciplinary design team.

In order to maximize the digital processor circuit performance, full custom circuit designs were used over compiled standard cell based designs with all the transistors and interconnects designed, sized, laid out, and optimized manually. Because the processing elements were relatively small, high number of design iterations could be used to maximize the performance while minimizing the area and power consumption. In addition, dynamic logic circuitries were used whenever appropriate to optimize the performance and minimize the power. To reduce the power consumption even further, low threshold voltage transistors were used in the dynamic logic circuits, which enabled lowering of the power supply voltage significantly without sacrificing the clock speed. However, low threshold voltage transistors made the dynamic charge storage nodes much more susceptible to leakage and transient failures due to signal path coupling, power supply bounce, substrate coupling, charge sharing, etc. Special attention was given in order to design robust dynamic logic circuitry, minimize coupling effects, and provide sufficient charge refresh rates.

The NLEQ4000 signal processor IC is designed to work with advanced high speed ADCs with sampling rates up to 4-GSPS. The computer aided design (CAD) tool drawing of the IC and the picture of the packaged part are shown in Figure 2. The IC was manufactured on a 0.25-micron bulk CMOS process. It accepts up to 12-bit input and produces output up to 16 bits. Input and output can be demultiplexed 2 or 4 ways. The overall die size is 6mm x 6mm and the computational core size is 2.6mm x 3.3mm. At 1.5-GSPS, it consumes 453mW of power with the core power consumption excluding I/O of 266mW. At 4-GSPS, it consumes 1219mW with the core power consumption of 706mW. At 4-GSPS, the processor IC performs approximately 1.5 TeraOPS resulting in 2-TeraOPS/W core power efficiency. As shown in Figure 1, the IC provides approximately 21dB of linearity enhancement on MAX108 running at 1.5-GSPS.

The NLEQ500 is the narrower bandwidth version of the NLEQ processor IC. It is designed to work with the ADCs up to 500-MSPS. The picture of the die and the BGA

package are shown in Figure 3. The IC was also manufactured on a 0.25-micron bulk CMOS process. It accepts up to 18-bit input and produces output up to 22 bits. The overall die size is 2.2mm x 2.2mm with the core size of 0.65mm x 1.4mm. The power consumption at 500-MSPS is 243mW with the core power consumption of 122mW. At 100-MSPS the IC can run on reduced power supply voltage of 0.6 volt rather than 1.2 volt and consumes only 25mW with 6mW core power consumption. The small core size and ultra-low core power consumption could enable this core to be easily embedded in ADC dies in the future. .

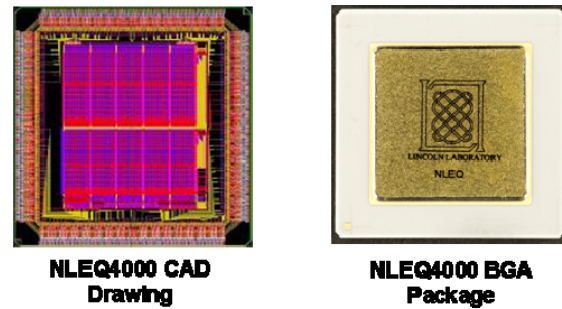


Figure 3: NLEQ4000 Ultra-Wideband NLEQ Processor IC.

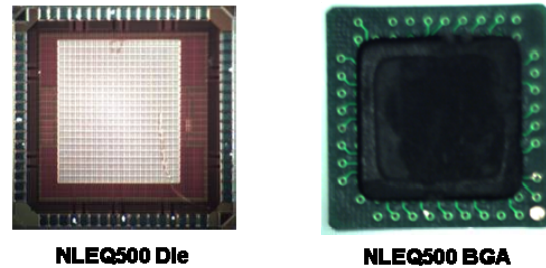


Figure 3: NLEQ500 Wideband NLEQ Processor IC.

## References

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