Heterogeneous Processing Solutions for the IBM BladeCenter™

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Introduction

The WILDSTAR™ 5 for IBM BladeCenter is the newest member of Annapolis Micro Systems' WILDSTAR™ family of FPGA-based computing products. Recognizing the increased demands for high-performance computing, Annapolis Micro Systems has selected and targeted their WILDSTAR™ 5 Blade Architecture for the IBM BladeCenter computing platform. With this approach, system designers can complement traditional microprocessor blades such as the IBM Cell Processor, IBM PowerPC, AMD Opteron, etc., with FPGA and Multicore processor computing blades in proportions that make sense given the algorithms required and the processing time specfied. This type of "hybrid computing" will ultimately accelerate the processing of complex applications. Multiple WILDSTAR 5 Blades can be installed into one or more IBM BladeCenter chassis to provide the wide scaling necessary to help solve computational intensive problems.

FPGA Blade Architecture

The WILDSTAR 5 FPGA Blade architecture is best illustrated in terms of Computational Processing Elements (CPEs) and I/O Processing Elements (IOPEs) as shown in Figure 1. The IOPE supports up to three external DDR2 DRAM memory ports, while each CPE supports up to seven external memory port options of either DDR2 DRAM, DDR2/QDR2 SRAM, or SIO/CIO RLDRAM. Up to six CPE Pluggable Modules (CPMs) can be populated on the FPGA Blade baseboard. FPGA, Multicore, Network, or general-purpose processor CPMs can be used interchangeably on the WILDSTAR 5 FPGA Blade.

The FPGA Blade architecture includes three Serial Gigabit I/O (SGIO) switches. First, a high-speed, protocol agnostic Crossbar switch allows for high-bandwidth, full-duplex communication paths between all processing elements, front-panel I/O, and the IBM BladeServer Midplane. Secondly, a standard PCI-Express Gen 2 switch is also on-board for PCIe switched protocol connectivity between all CPEs and three PowerPC embedded processors. Finally, a Gigabit Ethernet Switch allows for gigabit Ethernet switched protocol connections between the PowerPCs and the IBM BladeServer Midplane. All three SGIO switches are software configurable via the Host PowerPC embedded processor running Linux.

In addition to the Host Block PowerPC processor, two additional embedded PowerPCs are also available for user applications running Linux. These embedded processors with their direct connection to their respective IOPEs could be used to process complex protocols such as Infiniband.

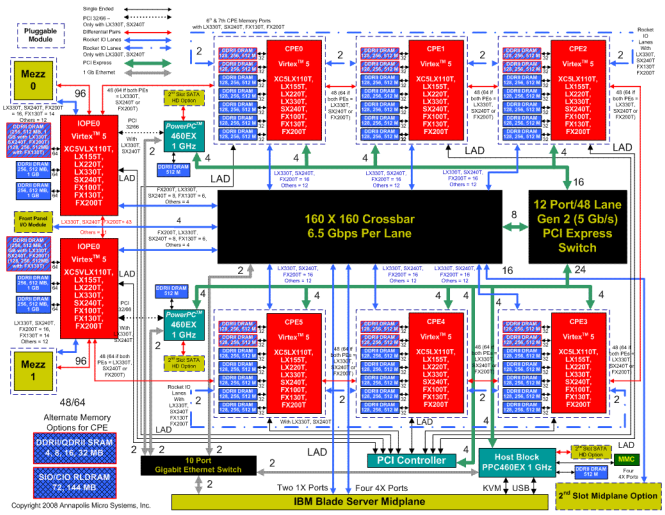

Figure 1: WILDSTAR 5 FPGA Blade Block Diagram

Radar Receiver Application

Figure 2 illustrates a dual-channel FPGA-based Radar Receiver implemented on the Annapolis WILDSTAR 5 FPGA Blade. It highlights the key functional blocks required to implement such a real-time processing system. Two front panel A/D mezzanine cards are used to digitize the incoming RF channels up to a sampling rate of 2 GSps. The next stage includes a Digital Down Converter (DDC) necessary to convert the digitized real signal to a basebanded complex signal centered at zero frequency. Downstream from the DDC, low-pass FIR filters pass only the desired signal and perform anti-aliasing filtering prior to decimation.

In parallel, time-domain overlapping FFTs can be performed along with a threshold detection operation that is used to implement a signal detection function. Fixed-length or variable-length FFT cores can be instantiated to allow frequency resolution to be traded for a faster detection response. For instance, when a signal detection FFT is configured for 4K points, the core can perform 50,000 4K point FFTs per second. For 16K points, 12,000 16K point FFTs can be calculated per second. In addition, fast ultra-long FFTs can be implemented using the Cooley-Tukey algorithm, reducing the algorithm to two smaller FFT cores (N1 x N2), Corner-Turn functions utilizing Matrix Transpose IP cores and external DDR2 SRAM banks all resident on a single Virtex™-5 CPM.

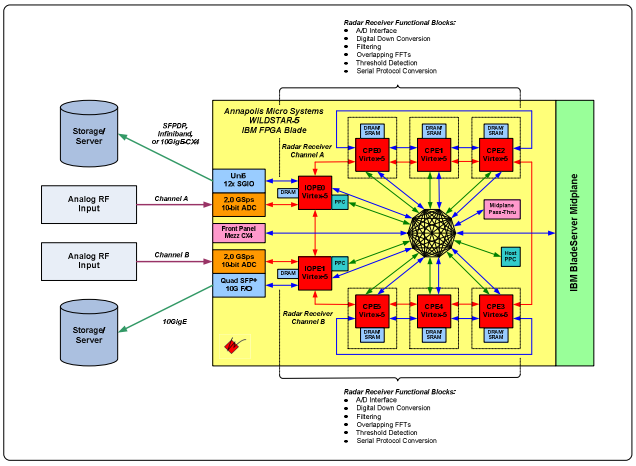

Figure 2: FPGA Blade Radar Receiver Application

Networking Services Application

Figure 3 illustrates a Networking Services Application implemented on the Annapolis WILDSTAR 5 IBM Blade using Tilera™ Multicore Processor CPMs. Ingress Networking functions include Serial Protocol Conversion, L4/L7 Deep Packet Classification, Policy Engine, and Packet (Payload) Buffering. Front panel Serial Gigabit I/O cards accepts incoming packets, over copper or fiber mediums, via standard network protocols from either Multi-Protocol WAN Switches or 10 Gigibit Ethernet Switches.

Tilera Multicore processors (up to 64 general purpose cores per CPM) can be user programmed to perform L4 through L7 deep packet classification. Packet classification is the process of categorizing packets into "flows". For example, all packets with the same source and destination IP addresses may be defined to form a flow. Generally, packet classification on multiple fields of the packet header is a difficult problem. Several different algorithms can be employed such as basic search algorithms, geometric algorithms, and heuristic algorithms. The algorithm suitable may be different for different types of packets. The Tilera Multicore processor is programmable in ANSI C/C++. It also has enough compute power that allows for multiple classification algorithms to be programmed on a single chip.

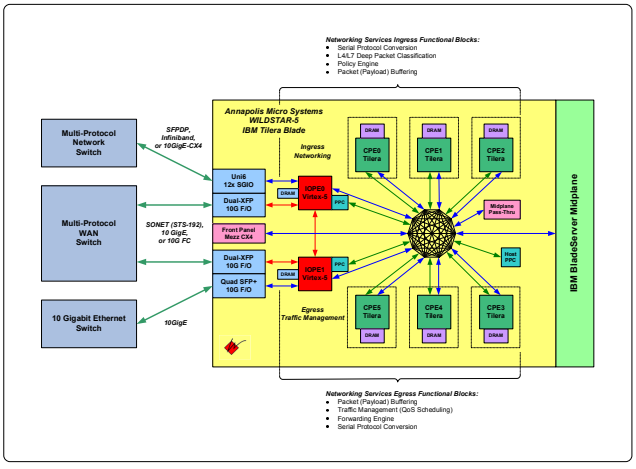

Figure 3: Tilera Blade Networking Services Application

Heterogeneous Processing Application

Figure 4 illustrates a Heterogeneous Processing Application implemented on the Annapolis WILDSTAR 5 IBM Blade using both FPGA and Tilera Multicore CPMs. This flexibility allows for real-time processing functions and multicore processing functions to be performed concurrently on the same baseboard occupying a single BladeCenter chassis slot.

Real-time signal processing applications could include Radar, SIGINT, EW, Image Processing, etc. that require complex computations and high-throughput where the amount of processing remains constant for such IP logic as ultra-long FFTs and multi-tap FIR filters. Either, Virtex-5 LXT, SXT, or FXT FPGA CPMs can be populated on a single Blade baseboard to further enhance the capabilities of the FPGA Blade.

Multicore processing applications such as Intrusion Detection, Network Monitoring, etc. that require complex computations on lower-rate data where the amount of processing required is not constant such as packet capturing, filtering, and decoding, can be shared on the same Blade. The WILDSTAR 5 for IBM Blade allows for a truly scalable platform that that can meet the needs for a broad range of real-time and multicore processing applications.

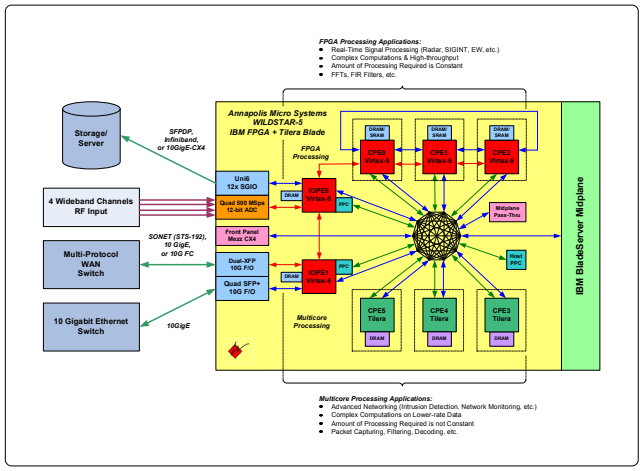

Figure 4: Heterogeneous Processing Application

Conclusions and Looking Ahead

Annapolis' IBM Blade product roadmap commitment will allow next generation FPGAs and Multicore technologies to be employed on today's WILDSTAR 5 for IBM Blade baseboard. Other processing technologies might include Graphics Processing Units (GPUs), General Purpose or Application Specific Processors (ASPs). No other platform available today provides this flexibility

System designers today can already make use of the BladeCenter's high speed midplane to mix and match the WILDSTAR 5 FPGA/Multicore Blades with any other board that fits in the IBM BladeCenter, to create one of the most powerful and well orchestrated heterogeneous processing platforms on the market.