# Floating Point Synthesis From Model-Based Design

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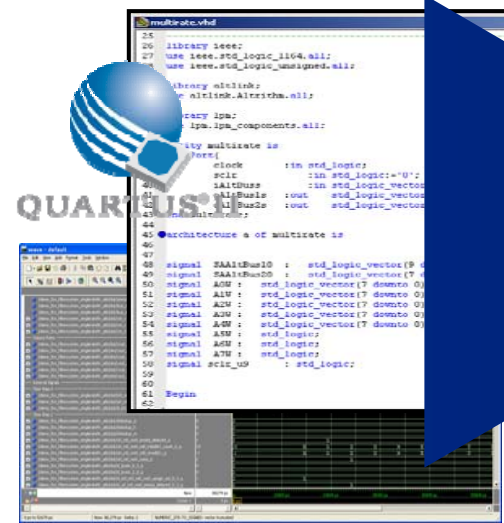
Floating Point On FPGA

- **Many new applications require floating point dynamic range performance;** *e.g.*
  - **Beam-forming, large FFTs, DPD feedback, …**
- **FPGAs can deliver:**
  - **A powerful mix of fixed and floating point performance**
  - **Extensive hard DSP capabilities**
    - **IEEE754 single and double precision specifically supported**
      - 100s 36x36 multipliers
      - ~100 54x54 multipliers
  - **Superior computational density per Watt than other solutions**
  - **Sustained peak performance**
- **Tools Enable:**
  - **Schematic design entry using operator blocks**
  - **Fused data-path compilation**
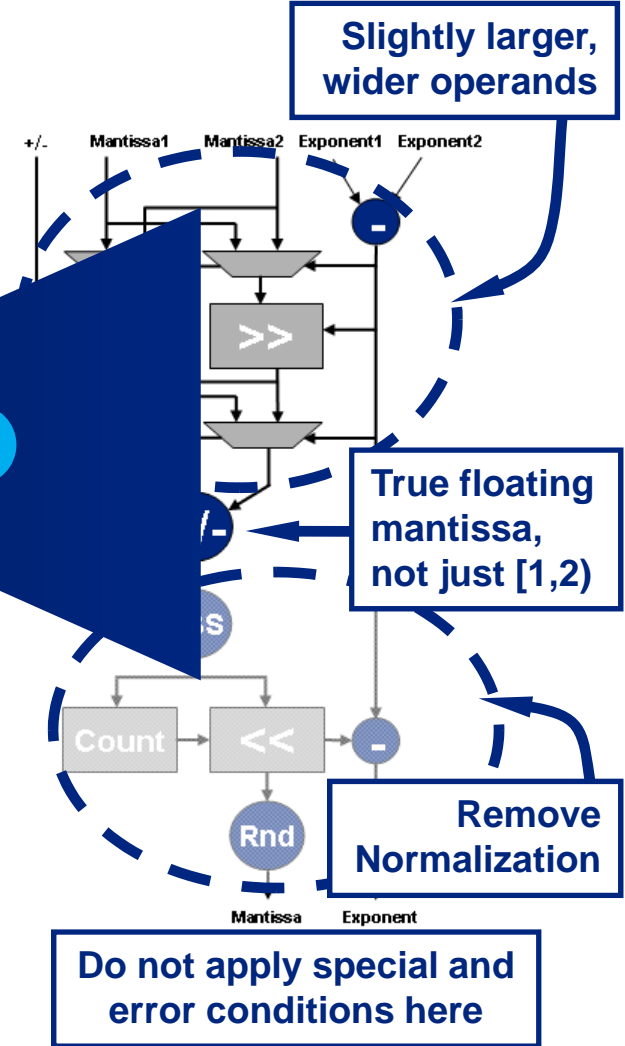
DSP Builder / Floating Point Compiler
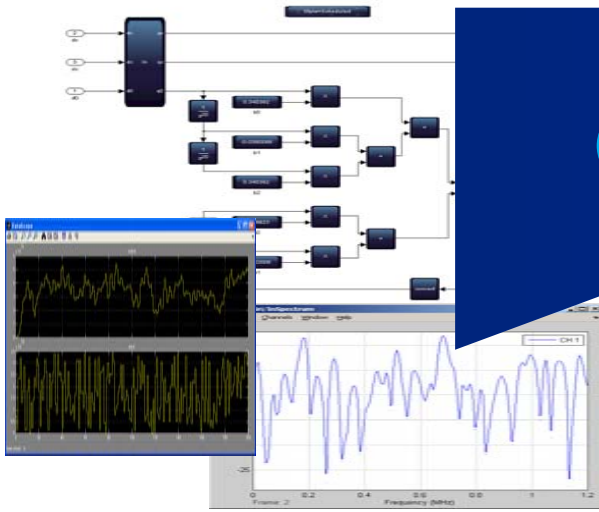
1 Develop & design schematically with primitive, math.h & core functions; in fixed and floating point domains

2 Tool applies global data-path optimizations to floating point domains and many fixed-point domain optimizations

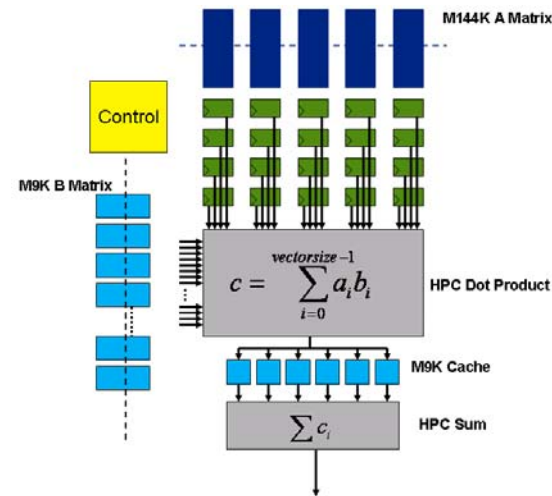**3** Tool generates integrated and optimized high-performance HDL on each simulation

Slightly larger, wider operands

True floating mantissa, not just [1,2)

Remove Normalization

Do not apply special and error conditions here

Density and Flexibility

Compiler Advantages

- **Fused data-path synthesis allows maximum density at 250MHz system performance**
  - **No system degradation for floating point**
  - **50% device logic resources available for system design**
- **Over 600 single precision operators can be supported in a mid-range device**
- **Optimized MATH.H library in development**
  - **Multiplier based algorithms give low latency, high performance, consistent results**
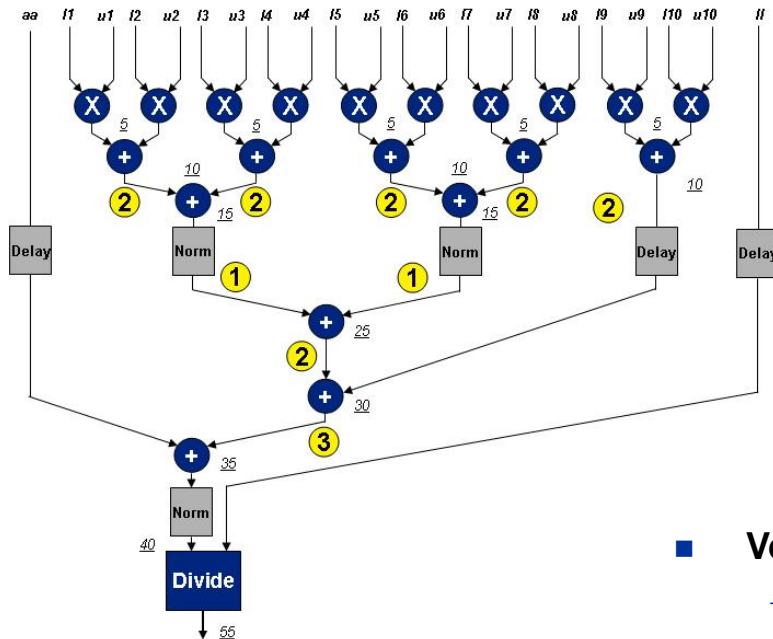 - **EXP, LOG, SQRT, INVSQRT, SIN, COS available now**

Floating Point IP

- **Matrix Multiplier Core**
  - **Parameterized**
- **Example design:**
  - **200 single precision operators, 295 MHz fit, 100 GFlops**
  - **¼ mid range device**

Control

M144K A Matrix

M9K B Matrix

$$c = \sum_{i=0}^{vectorsize-1} a_i b_i$$

HPC Dot Product

M9K Cache

$$\sum c_i$$

HPC Sum

ALTERA

Compiler vs. Cores

- **Compiled Data-path Example**
  - Matrix Decomposition

- **Compiled data-path is about 50% the size of core based design**
  - DSP resources same
- **Latency also 50%**

Matrix Size	Logic	DSP	Vector Logic	Core Logic
12x12	5197 (sp) 8652 (dp)	75	4587 (sp) 7855 (dp)	7800 (sp) 9000 (dp)
64x64	21457 (sp) 27346 (dp)	283	20681 (sp) 26004 (dp)	41600 (sp) 48000 (dp)

- **Vector Logic:**
  - *compiled data-path*
- **Logic:**
  - *compiled data-path + application*
- **Core Logic:**
  - *equivalent data-path constructed from discrete cores*