Altera FPGAs deliver:
- A powerful mix of fixed and floating point performance
- Extensive hard DSP capabilities
  - IEEE754 single and double precision specifically supported
  - 100x 36x36 multipliers
  - ~100x 54x54 multipliers
- Superior computational density per Watt than other solutions
  - In a recent National Science Foundation benchmark, a Stratix IV FPGA delivered 1T GFLOPS, and was the clear overall leader in high-GFLOPS/Watt.
- Sustained peak performance

**Devices**

- Floating point density largely determined by hard multiplier density  
  - Altera Multipliers efficiently support floating point mantissa sizes

**Compiler vs. Cores**

- Abstracted data-path design in DSPB  
  - DSP B building block points mapped to FPC blocks
  - FPC restructures data-path to avoid overflows and balance
- FPC optimizations applied independently of DSP Builder fixed-point optimizations
- Compiled data-path is about 50% the size of the equivalent core-based design
  - DSP resources saved
- Latency also 50%
- Corresponding power reduction
- Most of the data path dynamically powers down in soft logic, not multipliers
- Allows 100% of a device’s floating point capability to be used at still under 2000 MHz

**Example: LU Matrix Decomposition**

- Example: LU Matrix Decomposition

**Floating Point Model-Based Design**

- Fused data-path optimizations typically achieve 50% reduction in soft logic & latency - allowing 100% utilization of a device’s floating point capability at fixed-point speeds

**Tools: Floating Point Compiler (FPC)**

- Conventional Wisdom: IEEE754 system level design too complex for FPGAs
  - Floating Point core based design more soft logic than a fixed point FPAI supports
- But IEEE754 data-path inefficient: functional redundancy between operators
  - Required for processors – untutored operation combinations
- Arithmetic unit requires all inputs and outputs to be a known format
  - Not required for data-path – a priori knowledge of inter-operator relationships
- Data-path unit requires all inputs and outputs to be IEEE754 format
  - Internal format only has to guarantee that casting to and from IEEE754 is correct

- Build an FPC tool that exploits a priori knowledge of inter-operator relationships & has freedom to apply data-path level optimizations

**Tools: DSP Builder Advanced / FPC Integration**

- Effortless FPGA Implementation
  - Automatic pipelining to meet required Fmax, data path performance as optimized NDL
  - Easy timing closure - fewer transistors Floating Point blocks
  - Compile synthesized fixed point optimized data path

- Fast Design Space Exploration
  - Integrated design exploration and generation
  - Automatic generation of control plane logic

**Examples: Floating Point IP using FPC**

- Programmable Cholesky Decomposition
  - 100% multiplier usage with fraction of logic usage
  - Can fill the device with floating point operations and still achieve pushfit
  - 300 ALUT / 400 register per operator pair
  - Less than half of core methodology