RAPID:
A Rapid Prototyping Methodology for Embedded Systems

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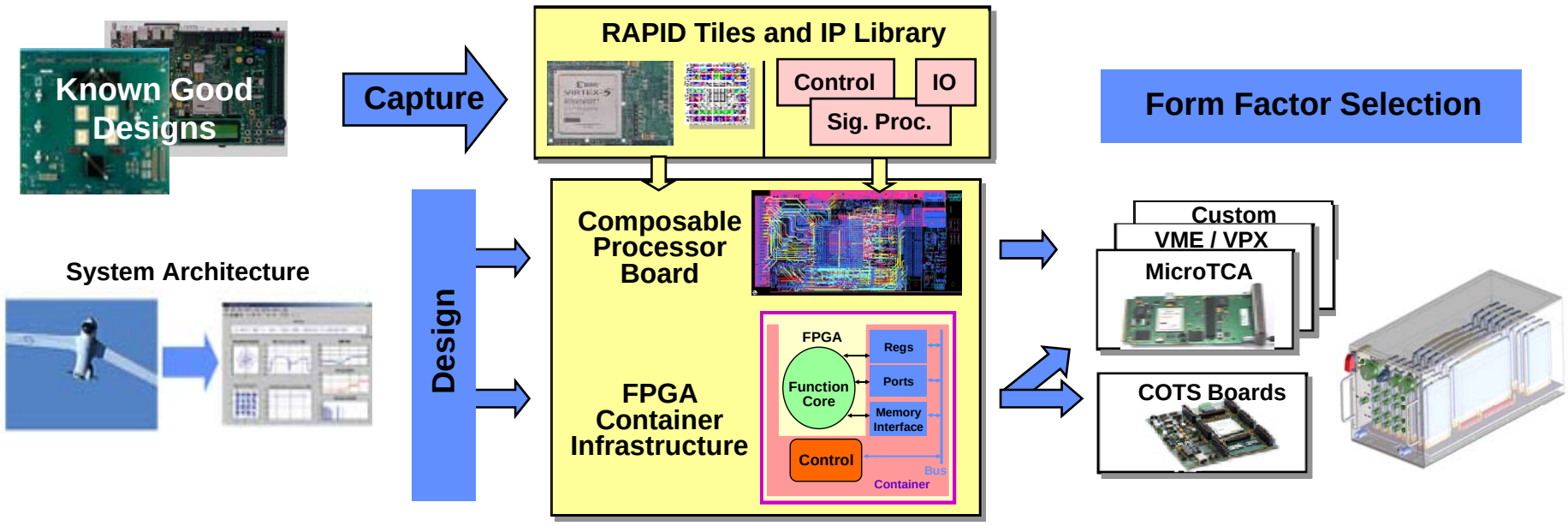
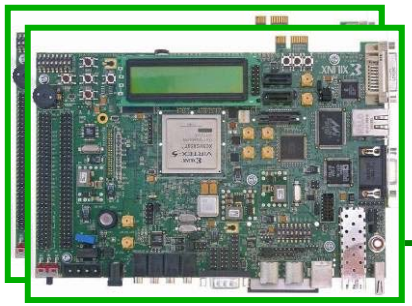
RAPID - Rapid Advanced Processor In Development



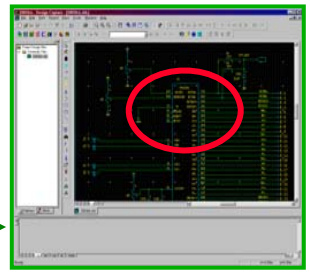
Main features of RAPID:

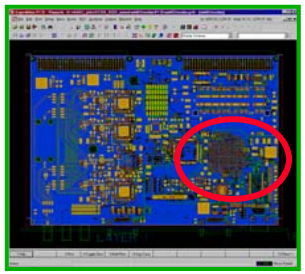
- **Composable board design process**
  - **Custom processor composed of tiles extracted from known-good boards**
    - **Form factor highly flexible**
  - **Tiles accompanied with verified firmware / software for host computer interface**
- **Container framework allowing co-design of boards and IPs**
  - **Portable FPGA Container Infrastructure with on-chip control infrastructure, off-chip memory access, and host computer interface**
  - **Surrogate board can be used while target board(s) are being designed or purchased**

Composable Board Design Flow



Known Good Boards

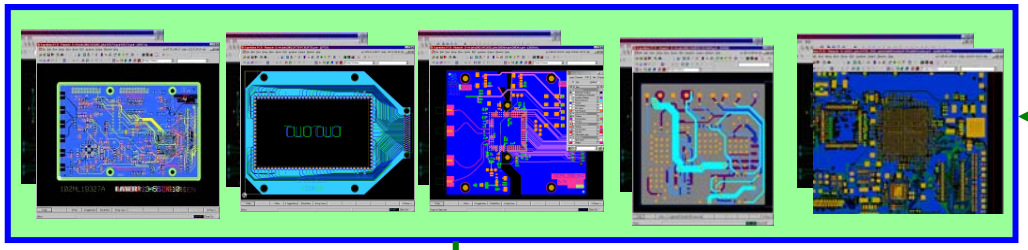


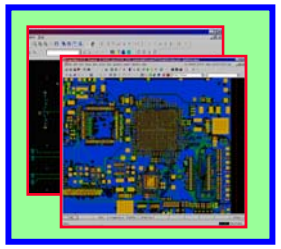


Extract circuit block of interest (Known Good Circuit)

Physical Design Reuse tool

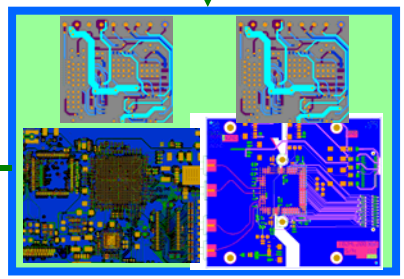
Tile Re-use Library





Hierarchical Composite "Known Good Tile"

Verify



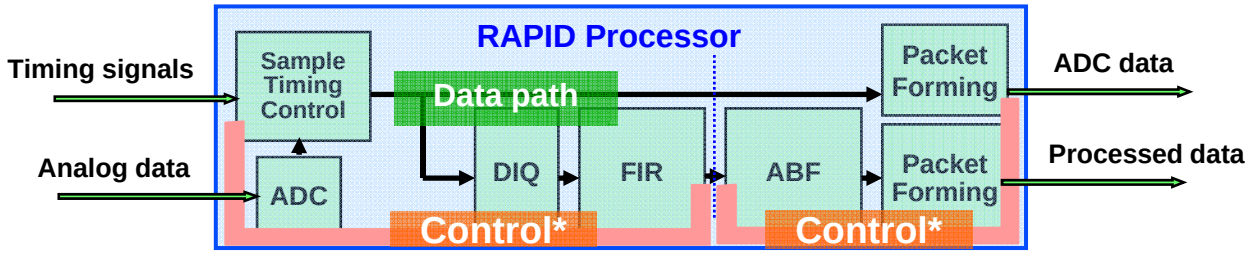
RAPID Design Board

Board design time

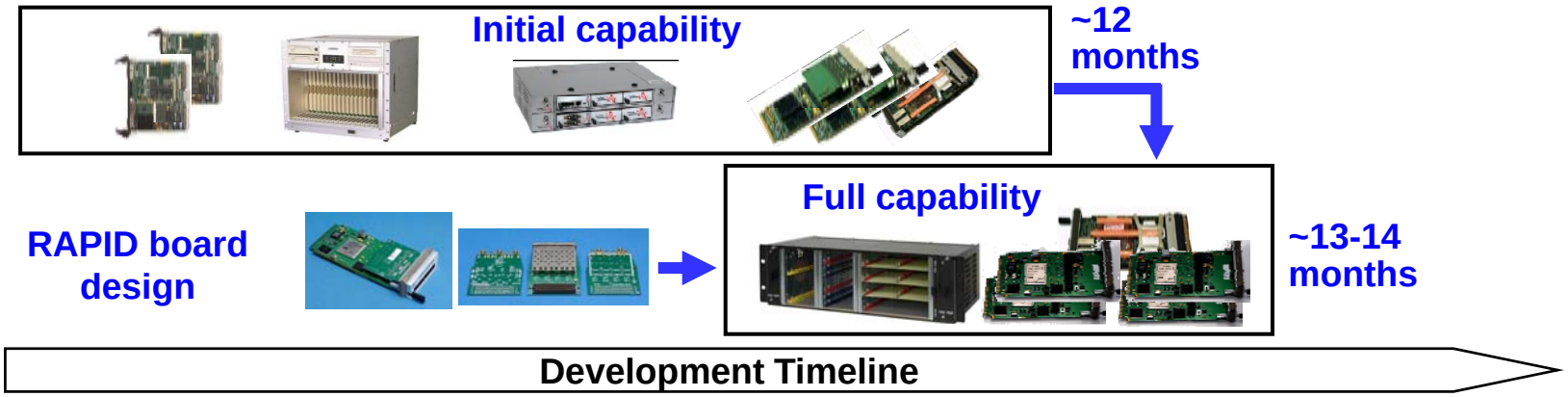
Approach \ Duration	Schematic	Layout	Manufacture	Test & Debug	Total (mos.)
Start from scratch	3-6	2-4	1-2	1-2	7-14
Known Good Board	1-3	1-3	1-2	1-2	4-10
Known Good Tiles	0.5-1	0.5-1	1-1.5	1-1.5	3-5

Reduces time 50% to 66% as well as increases probability of first-spin success

RAPID System Development



- 6 months head start on surrogate system
  - Overlapping of FPGA and board design
  - Standardized control interface allows smooth porting to objective system
- 2 months saved in system debug and integration
  - *Incremental integration* with local storage for data path source / sink



*A. Heckerling, T. Anderson, H. Nguyen, et.al., An Ethernet-Accessible Control Infrastructure For Rapid FPGA Development, HPEC 2008.