# RAPID – A Rapid Prototyping Methodology for Embedded Systems

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## Introduction

RAPID (rapid advanced processor in development) is a rapid prototyping methodology that systematically reuses known-good hardware, firmware, and software designs to compose application-specific embedded systems. This methodology mitigates many risk factors associated with unknown performance from the design process so there is a higher chance of first pass success. In the development of a high-performance custom FPGA-based embedded processor for a radar application, a reduction by half in development time has been demonstrated.

## Motivation

The asymmetric warfare aspect of GWOT (global war on terrorism) has added new challenges to the development of high-performance embedded processors. Besides stringent SWaP (size weight and power) constraints, new hardware and software capabilities often have to be developed in a very short time (e.g., 6 months vs. the conventional 12-24 months). In theory, COTS (commercially off-the-shelf) products can be leveraged to reduce the embedded processor development time. In practice, as many of these rapid capability applications also demand the use of latest technologies (e.g., the largest and fastest FPGAs) to meet their SWaP requirements, adequate COTS products are either unavailable (under development) or immature. Also, COTS products, since they are designed to target a broad market, may not provide a perfect match (form factor, power consumption, memory capacity, data rate, etc.) to the application. It is also easy to either overdesign or underdesign with new COTS products, as their true performance (vs. marketing performance) can only be determined by performing application-specific benchmarking. Developing custom processor boards is a viable alternative. However, custom boards are not a panacea as they still have issues similar to those in COTS products. Industry has many anecdotes of board development budget and schedule overruns.

## LOTS Approach

The Embedded Digital Systems Group of Lincoln Laboratory has been developing embedded processors with a LOTS (Lincoln Off-the-shelf) approach. The possibility of reusing a known-good custom processor board design is explored when a new project begins. As the processor board has been previously used, its capability is well-understood. The board is then adopted to meet the new program requirements. An example of this LOTS approach is the rapid prototyping of a high-performance processor for a sensor application [1]. After determining that the use of COTS boards would present a high risk to the project schedule, a custom processor board, previously developed for a different functionality, was quickly adopted for the new application. Despite the need to go through a PCB (printed circuit board) modification and manufacturing cycle to accommodate the new ADCs (analog to digital converters) that operate 4 times faster than the old ADCs, the development of this processor was successfully completed in one year. The same board was further leveraged a few more times for other applications. Each time a high performance product was delivered in a very fast turn-around time (as short as 6 months).

## RAPID Approach

The LOTS approach has its important benefits. A significantly faster turn-around time is achieved by leveraging previous NRE (non-recurring engineering) investments and team experience. As the baseline processor board has been thoroughly characterized, the chance of first pass success is very high. However, risks and issues similar to those of COTS still exist. Upgradability is a big issue as new technologies (e.g., new FPGAs) must be incorporated. In addition, the approach still lacks the flexibility to meet the GWOT challenges.

Lincoln Laboratory has recently further developed the LOTS approach into a RAPID prototyping methodology, which systematically reuses known-good hardware, firmware, and software designs to develop embedded processor systems. The baseline idea is the creation of a composable processor board as shown in Figure 1.

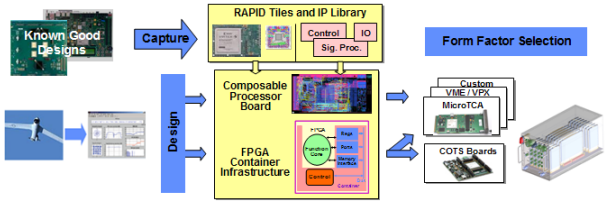


Figure 1: RAPID prototyping methodology.

The RAPID prototyping methodology consists of two components. The first component is a library that contains reusable circuit board tiles and IPs (intellectual properties) verified in previous designs. For example, the schematic and layout of a memory block and its interface to an FPGA in a known-good design can be extracted and stored in the library for future uses. The creation of reusable firmware IPs with an open-interface container concept was described in [2]. A host computer uses the open-interface container to communicate with the

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functional IP cores residing in an FPGA. Each functional core (or a group of cores) can be individually addressed, configured, controlled, and tested. The open interface significantly enhances the IP core portability, allowing them to be developed in parallel to board development.

In addition to previous in-house designs, a good source of library elements is the evaluation boards available from the component vendors. Component vendors routinely develop and sell evaluation boards that integrate their latest products (e.g., FPGAs, ADCs, etc.), IP cores (e.g., interface), and other common peripheral devices (e.g., memory, Ethernet interface, etc.) so that customers can perform their own application-specific benchmarking. These evaluation boards are excellent surrogates for developing and benchmarking IPs while the custom circuit boards are being developed, thus converting a sequential design process into a parallel one. Furthermore, the schematic and layout of the evaluation circuit board are often included as part of the evaluation package. A designer can thus populate the reusable library by extracting reusable tiles from the evaluation board design. This approach provides an easy path to keep the library in synchronization with state-of-the-art technologies.

The second component is the RAPID design flow. Tiles and IPs represented in CAD format are selected from the library to develop the target application. The tiles are integrated using PCB CAD tools to compose a new circuit board. This process requires the CAD tool to have the capability to merge two or more previous designs together, modify the result, and create a new circuit board. A number of commercial circuit board design tools have started to support this type of enhanced reusability.

The result board layout is then mapped to a desired form factor (e.g., MicroTCA, VPX, custom, etc.). The capability to create a non-standard custom form factor circuit board is extremely beneficial in applications such as those to be implemented on mini-UAVs. The design can be custom-fitted into a small and irregular enclosure. Note, as shown in Figure 1, the RAPID prototyping methodology does not exclude the use of COTS boards, especially those successfully used in previous projects, in the design process.

## Results

Figure 2 shows a high performance FPGA processor board in MicroTCA form factor and a number of FMC (FPGA Mezzanine Card) boards created with the RAPID methodology. The FPGA board leverages the design of an evaluation board which was chosen from the repertoire of an FPGA vendor. Based on a Virtex-V FPGA operating at a peak frequency of 550 MHz, the processor provides a throughput of 100 to 200 GFLOP/second and consumes 25 W. The board also has 1 GB of RAM operating at 3.2 GB/s and 8 MB of SRAM at 0.8 GB/s. The external I/O data rate is 5 GB/s per direction.

The FMC boards include a dual LTC2209 ADC board, an I/O board, and a control board. Although this was the pilot test run of the RAPID prototyping methodology so extra time was spent in tool configuration and verification, the FPGA processor was checked out in 5 months. After the design team has gained more experience, we expect a design of similar complexity will take only 3 months.

Figure 2: A radar frontend FPGA processor and its FMC boards.

Using the open interface container approach, the design of FPGA firmware (a 4 channel adaptive digital beamformer) was started at the same time of the processor board design. The firmware was verified on a surrogate COTS processor with only a quarter of the required throughput. The result is a 6 month head start on the development of FPGA firmware. When the target processor was ready, the team spent merely 3 weeks to port the design from the surrogate to the target platform and demonstrated a seamless migration of FPGA functionality from a surrogate to a target system.

In summary, the RAPID prototyping methodology delivers two major advantages. First, being able to selectively and systematically reuse known-good designs, the design time of a high-performance processor board can be significantly reduced (typically in half). Second, the adoption of an open interface container infrastructure for FPGA IPs allows the overlapping of board and FPGA firmware design steps. Reuse has also proved to provide savings in the efforts of integration, verification, and documentation.

## Ongoing Development

The RAPID prototyping methodology is currently being extended into a laboratory wide infrastructure. In order to maximize its benefits, design tutorials, examples, and workshops are being created to facilitate the adoption of RAPID in the embedded processor design community. In addition, a “match-making” service between new and previous applications is being developed.

## Reference


[1] M. Vai et al, “Rapid Prototyping of a Real-Time Range Compression Processor,” HPEC 2005.

[2] A. Heckerling et al, “An Ethernet-Accessible Control Infrastructure for Rapid FPGA Development,” HPEC 2008.