Signal/Data Processor Implementation and Algorithms for Realtime Wide-Angle Ultra-Wideband SAR Image Formation

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Background

The U.S. Army Communications and Electronics Command Intelligence and Information Warfare Directorate and Lockheed Martin Integrated Systems and Solutions have developed a dual-band VHF/UHF Synthetic Aperture Radar (SAR) that provides all-weather, day/night capabilities to detect stationary targets in several deployed conditions: buried, obscured by foliage and camouflage, and in the open. This system, the Tactical Reconnaissance and Counter Concealment Enabled Radar (TRACER), is designed to operate on the Extended Range/ Multi Purpose Unmanned Aerial Vehicle System (ER/MP UAS) and is also designed to be 90% form, fit and function compatible with the MQ-9 Reaper UAS. In order to fulfill its mission TRACER must perform SAR image formation and other post-processing computations onboard in realtime and still stay within the power/weight budget available on the ER/MP air vehicle. The signal data processor hardware must also be able to tolerate the relatively harsh temperature and vibration environment of the ER/MP and MQ-9. Currently the TRACER SAR is being flown onboard a manned aircraft to demonstrate system performance. This paper describes the signal processing software and hardware that has been developed to perform the realtime onboard VHF/UHF SAR image formation processing and will also present a summary of some of the lessons learned during the development of the hardware and software.

VHF/UHF SAR image formation for the TRACER SAR is a difficult challenge. The TRACER system includes a VHF SAR with ~ 7m resolution and a single polarization channel (HH), and a UHF SAR with ~ 0.75m resolution and up to four polarization channels. The transmit waveforms must be notched to avoid interference with a number of Federal Aviation Administration navigation and air traffic control systems that operate at VHF/UHF. On receive, digital Radio Frequency Interference (RFI) suppression algorithms are required to eliminate high-power in-band RFI sources. At VHF/UHF, coherent integration angles of 40 to 50 degrees are required to achieve even modest resolution, which results in significant range migration during the coherent integration. This range migration is so large that the conventional polar format algorithm is not suitable. At the TRACER SAR's maximum ranges the coherent integration time is three to five minutes or more. A tightly coupled inertial/GPS measurement system is required to provide accurate motion measurement over the long coherent integration times. The very long synthetic aperture also results in very large memory requirements and large inter-processor communication bandwidths.

System Implementation

In order to meet the challenging memory and throughput requirements of the TRACER system, Lockheed Martin has chosen reconfigurable hardware manufactured by SRC Computers for the airborne Signal Data Processor (SDP). The SDP is comprised of a spray-cooled multi-MAP® SRC-6. The system size is 21"W x 17"D x 10.5"H, it weighs 80 pounds, and consumes less than 900 watts of power. The SDP is capable of operation to at least 25,000 feet in an unpressurized environment and contains one dual socket Intel Xeon® microprocessor, four Series E MAPs (SRC's reconfigurable processor) and 80 GBytes of memory in five Global Common Memory (GCM) banks connected by a Hi-Bar® switch.

The system architecture is built upon a low latency, high bandwidth 16-port Hi-Bar switch. The microprocessor motherboard is connected to the Hi-Bar switch via the SNAP™ interface that plugs into a pair of DIMM slots on the motherboard. Each connection to the Hi-Bar switch can support a payload bandwidth of 1.4 Gbytes/sec.

Figure 1: Front view of the SDP Chassis

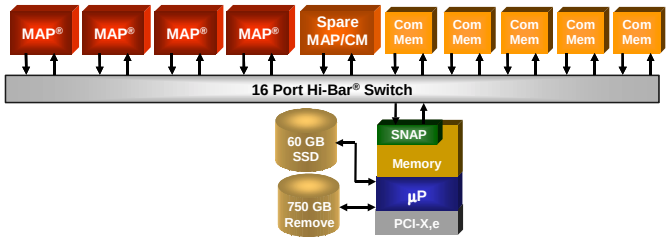

Figure 2: SDP Architecture

Application Porting

This was no small kernel or algorithm that was being ported. The "application" consisted of six major stages of computation and comprised over 250,000 lines of C. The stages in the application were Stage 0, Matched Filter, Stolt Interpolation, Azimuth Compression, Autofocus and Change Detection.

The application had a pthread running on the microprocessor that read radar data from disk and loaded it into a GCM bank. Each application stage execution was divided up across multiple MAPs each sharing access to an Input and Output GCM Bank. Another microprocessor task signaled a set of pthreads that controlled the execution of the MAP tasks.

SRC's Carte™ Programming Environment compiles C and Fortran codes into FPGAs. The compilation process seamlessly integrates microprocessor code and code targeted for the MAP into a single Unified Executable.

An initial port of the application to use MAPs took three programmers about three months. The optimization process then started and took advantage of a set of Carte programming features and SRC-6 system features. A highlight of the features used in the porting effort is shown in Table 1.

Architectural Feature	Algorithm Benefit
Multiple User Logic Chips	The large algorithm codes needed the logic space of two FPGAs
Use of GCMs	The large data volumes used 16 GBytes to store input and output data
Streams	Stream data as it is computed in one compute loop and consume it in a subsequent compute loop. This provides the ability to do these loops in parallel and not to store the computed data in memory
Streaming DMAs	Stream the input data directly into compute loops without needing to store data in local memories and/or stream out computed data
Specialized DMAs	Used the Corner Turn and 2D Sub-array forms of DMAs
Streaming FFTs	These forms of FFT will stream multiple vectors of data into and out of the FFT at a rate of one point per clock

Table 1:

Porting Lessons Learned

This was the first time the Lockheed Martin programmers used Carte and SRC systems. As in any porting effort there are always lessons learned such as:

- Get code running on the MAP as soon as possible in the development process. It was found to be better to get the data flow working and then add and verify small pieces of the algorithm at a time.
- Use fixed point processing wherever possible for the best performance. You can get many more fixed-point operations per FPGA versus using IEEE Floating Point.
- Create a data flow template that can be used (and reused) as a starting point. A template that was created as the starting point for all of the SAR processing stages just read in lines of data, passed them through to the secondary chip, back to the primary chip and back to GCM.
- Write logs to circular buffers in OBM. Since OBM persists after a MAP call, it can be inspected to show a "trace" of the previous MAP call. This was useful for debugging code.
- Take advantage of a set of tools that can be used to peek/poke OBM/GCM. The tools allow you to specify GCMs/MAPs/OBM banks and addresses, and read/write data.

Summary

The SDP system has demonstrated performance equivalent to 100 Power PCs and has a 10x reduction in power consumption. This system is using COTs hardware that is meeting airborne MIL specs. The application code base is portable to other SRC-6 and SRC-7 systems and is already being used for additional unnamed programs.