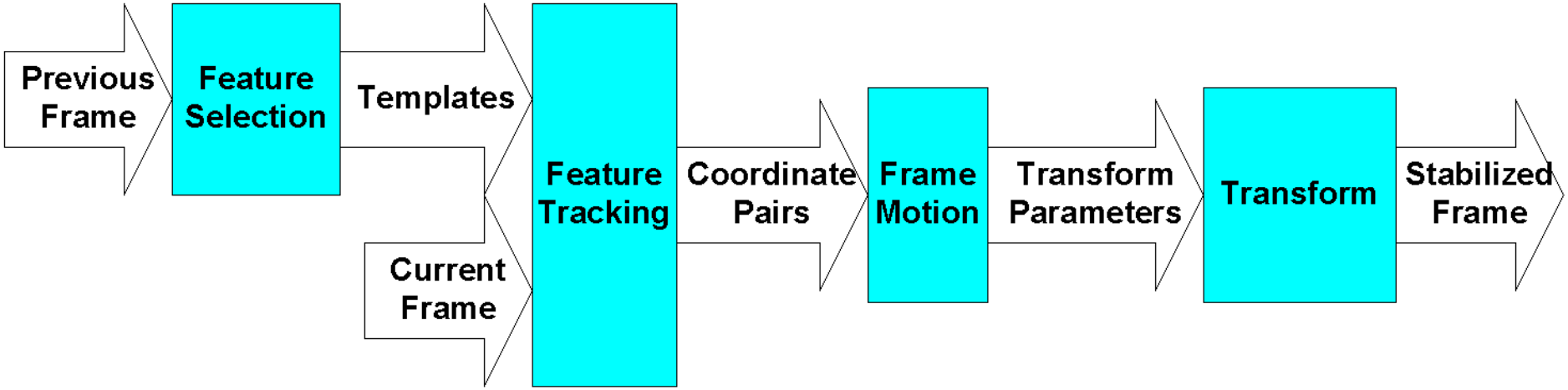
UAV Video Image Stabilization on the SRC MAP® Processor

William Turri, University of Dayton Research Institute (UDRI)
William.Turri@udri.udayton.edu

David Pointer, SRC Computers, LLC
dpointer@srccomputers.com

Airborne Video Stabilization Processing Overview



Performance Results

86x Performance @ 60 Watts

Nehalem i7 920 Quad Processor
CPU clock: 2.67 MHz
Level 2 cache: 4x 256 KB
Level 3 cache: 8 MB

82.238 seconds/frame (0.01 fps)
11,180 Watts (86 processors)

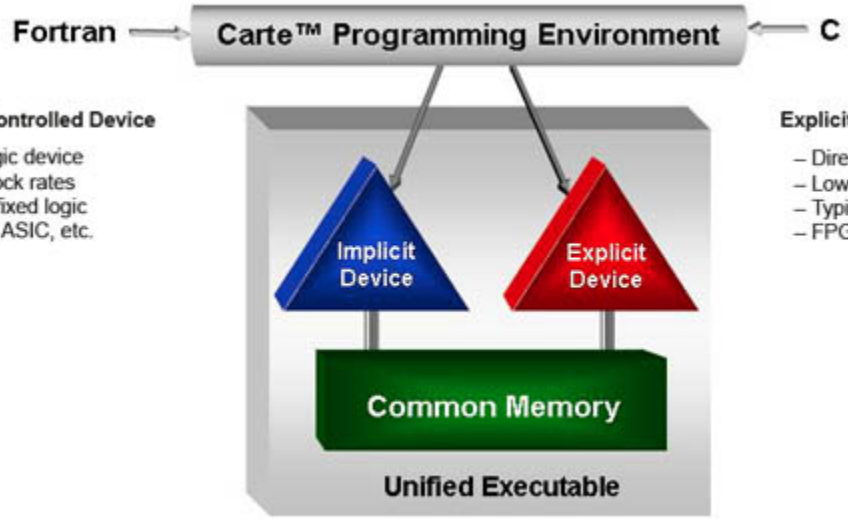
Series H MAP Processor
2x Altera EP2S180 FPGAs
FPGA clock: 150 MHz
On-Board Memory: 64 MB
Global Common Memory: 2x 1 GB

0.948 seconds/frame (1.06 fps)
60 Watts (1 processor)

Video frames: 2816x2112 (6 MP) 8bpp

SRC-7 MAP Form Factors

- Two Altera FPGAs with 16 SRAM banks are connected to the x86-based system via the SDRAM memory bus
- Two 1 GB banks of DRAM
- 3.6 GB/s sustained throughput per port
- ANSI C and Fortran programming interface
- Tower, 2U server, or Embedded form factors



Conclusions

- Research has broad applicability to other image registration algorithms
- Results are noteworthy for a first-pass solution
- We hope you will visit our poster presentation today!