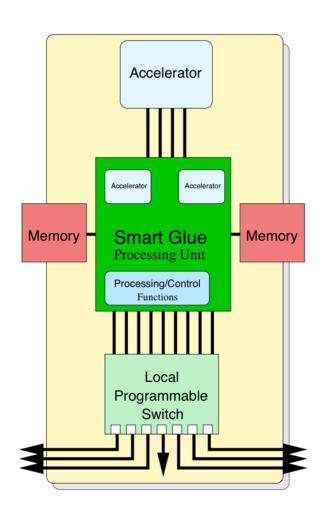
PetaFlops Router

Zachary Baker, Justin Tripp, Matt Stettler

Methods

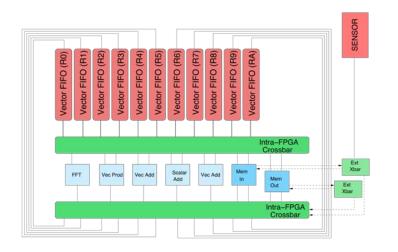
Smart Glue: Self-guided computation

- Achieving high performance does not require explicit design-time decisions
 - Hardware decides how to implement computation, on-the-fly
 - Automatic extraction of available parallelism
 - Automatic stream pipelining if possible
- Allows for efficient parallel computation
 - Allows scientist end-users to design
- Provides failure robustness through awareness of system state
 - If a link or node fails, system routes around the failure transparently



Methods, continued

- Functional demo of PFRouter system
 - FFT-based signal processing engine
 - Streaming, automatically pipelined
 - One solution every 8.3 ns
 - Similar to Threat Reduction-style applications
 - Process:



- Code is assembled into byte code
- Byte code is processed by SmartGlue
 - FPGA Crossbar is configured according to byte code
 - With no unmet dependencies, parallel streaming is enabled

Results and Accomplishments

- SmartGlue running on a single FPGA node, controlled by embedded processor
 - Crossbars, FIFO structure functional
 - Interprets byte-code programs generated by assembler
 - Automatic pipelining of stream operators
- Delivery of first hardware
 - Populated with fast serial optics, crossbar, and FPGA

SmartGlue General Structure

