Aerospace Data Storage and Processing Systems

High-performance Heterogeneous and Flexible Computing Architecture for Spacecraft Internet Protocol Communication and Payload Processing

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SEAKR Engineering, Inc.

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Motivation

- **Mission requirements increasing**
  - **Higher resolution data acquisition driving processing and storage**
  - **Onboard processing and/or downlink often the system bottleneck**
  - **Increased need for autonomous functionality**
  - **System flexibility sought to limit NRE**
- **Design challenges keeping pace**
  - **SWaP limitations on payloads not relaxing**
  - **Multiuse systems and payloads desired**
  - **Use of Commercial-Off-The-Shelf (COTS) devices**
    - **"Rad-hard" components less cost-effective for high-performance apps**
    - **Improved performance with mitigation to achieve fault tolerance**
  - **System heterogeneity and increased complexity**
    - **Reconfigurable computing devices provide flexibility and improved perf/Watt for amenable application classes**
    - **General-purpose processors well suited to control and database apps.**
    - **Special-purpose procs provide app. specificity with reduced dev. cost**

HPEC with Flexibility

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Application Independent Processor (AIP) Features

- Mixture of general-purpose processors and RCCs
- Reconfigurable on-orbit
- Flexible, scalable architecture
- Usage of open standards
- SEE Tolerant system
- Flexible I/O architecture

Designed for Responsive Space

- Low cost, high performance
- Rapid deployment through adaptability
- Designed for multiple missions

ARTEMIS Configuration of AIP

AIP System Architecture

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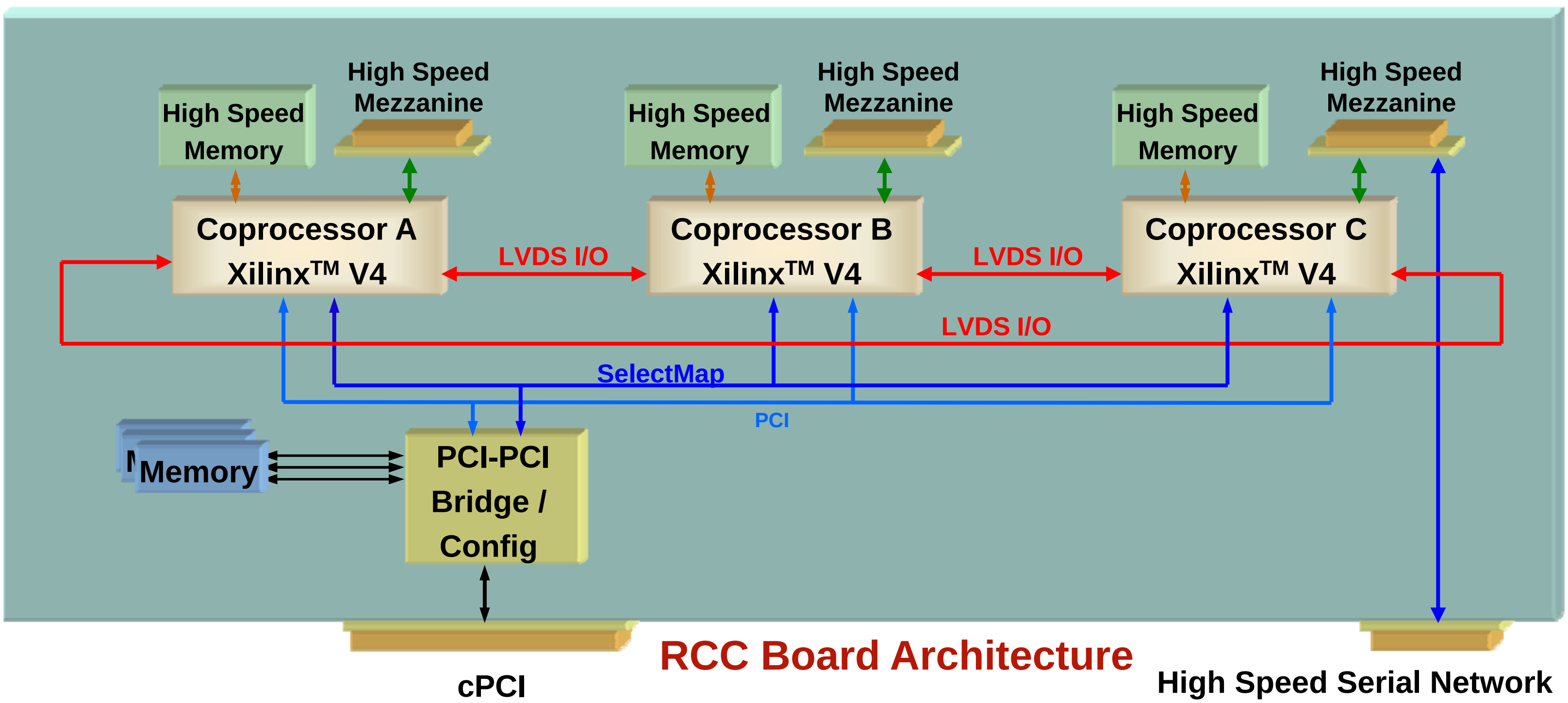
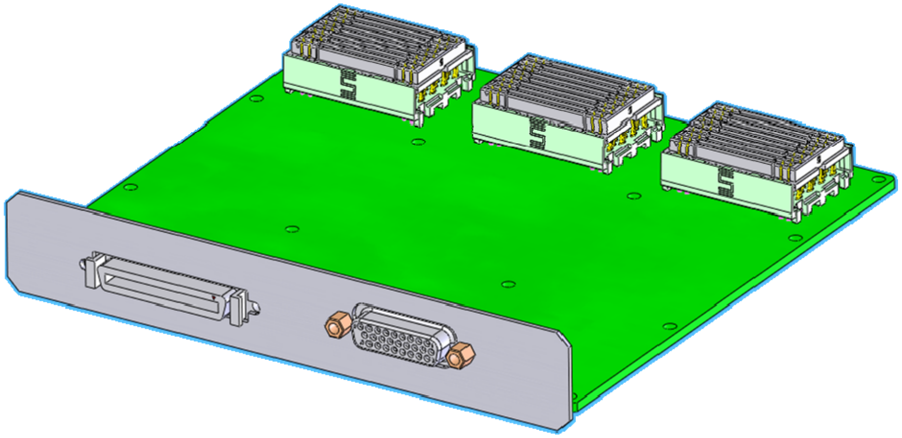
- Xilinx® Reconfigurable Computer Board(s)
- COTS PowerPC™–based SBC(s)
- Memory and I/O personality mezzanine cards
  - Flash memory, camera link, analog, digital developed to date
- Flexibility to incorporate other system control and I/O capability



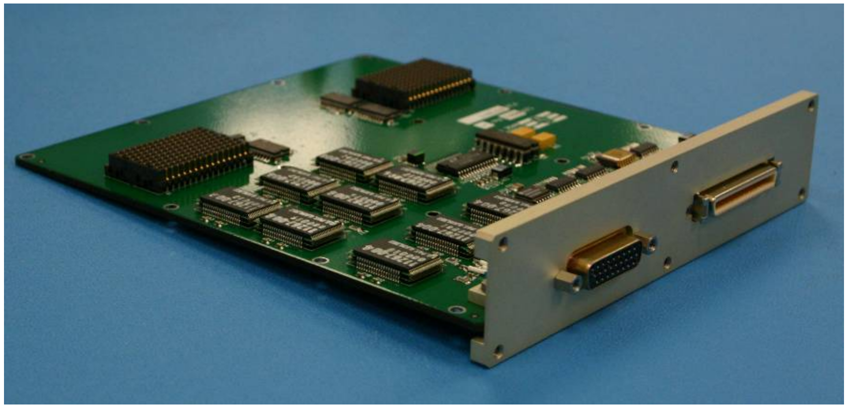
RCC Board Architecture

AIP Personality Mezz. Card

- Personality Mezzanine for application- specific functionality
  - Lower risk/cost, quick development
  - I/O and unique I/O connectors
  - Memory, Logic, TMR mitigation
  - Analog circuitry ADC/DAC
- High speed mezzanine connectors
  - 170 high speed I/O
  - Symmetrical Design to all FPGAs
- Fault tolerance options
  - "Rad hard" voter on the mezz.
  - Partial TMR
  - SEAKR replay capability provides temporal redundancy
  - Combinations



AIP Mezzanine Concept



ARTEMIS Mezzanine

AIP Deployments

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- **AFRL TacSat-3 Responsive Space mission**
  - **Raytheon's Advanced Responsive Tactically Effective Military Imaging Spectrometer (ARTEMIS)**
- **Cisco's Internet Router In Space (IRIS)**
  - **Space Internet Protocol Router (SIPR)**
  - **Programmable Space IP Modem (PSIM)**
- **AFRL Plug and Play Satellite project**
  - **Programmable Space Transceiver (PST)**
- **SEAKR's Reprogrammable Space Network Interface Card (RSNIC) interconnect adaptor**
- **Orion Vision Processing Unit (VPU) for NASA**
- **JPEG2K image compression**

Responsive Space

- "<u>Responsive Space</u> refers to the ability to rapidly achieve a specific objective through the use of space with rapidly being the operative word. The AFRL Office of Force Transformation suggested that the goal for fielding a new payload is weeks and months and not decades." [1]
- Tactical Satellite (TacSat) program building competency to achieve the Responsive Space challenge [2]
  - Joint AFRL and NRL demonstration program
  - Goal to develop capability to field inexpensive space systems in time of crisis to augment and reconstitute existing capabilities or perform entirely new tactical theater support missions
  - Key success criteria include
    - Develop low cost ($20 million or less) mission-specific spacecraft
    - Rapid deployment with on orbit activation within six days of call up
    - Provide between six to twelve months of reliable mission operations

[1] Lanza, et. al., "Responsive Space Through Adaptive Avionics, Responsive Space Conference, Los Angeles, CA, April 19-22, 2004.
[2] J. Raymond, et. al., "A TacSat Update and the ORS/JWS Standard Bus," Responsive Space Conference, Los Angeles, CA, April 25-28, 2006.

TacSat-3 – Tactical Ops

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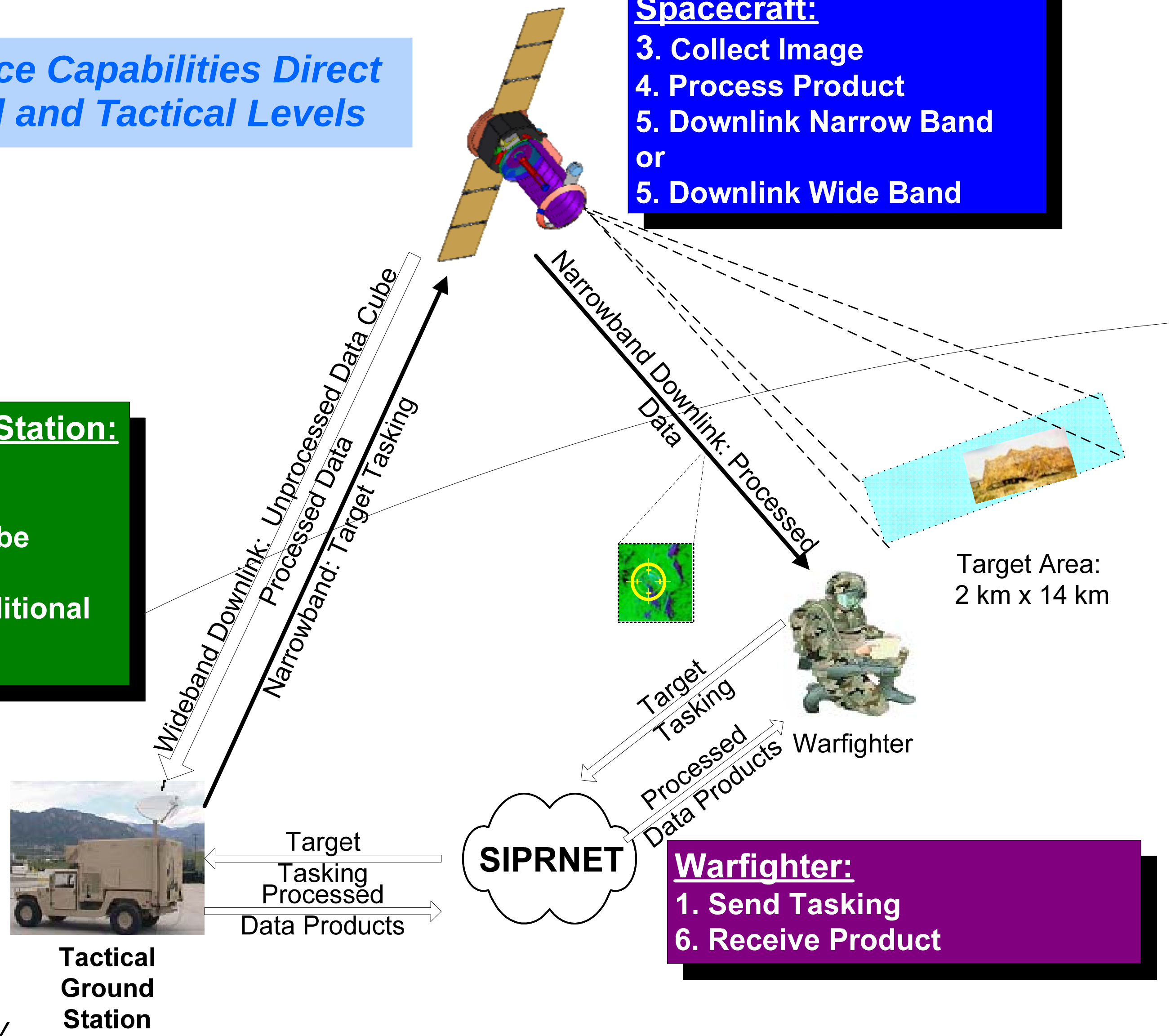
Dedicated Space Capabilities Direct to Operational and Tactical Levels

Spacecraft:
3. Collect Image
4. Process Product
5. Downlink Narrow Band
or
5. Downlink Wide Band

Tactical Ground Station:
2. Uplink Tasking

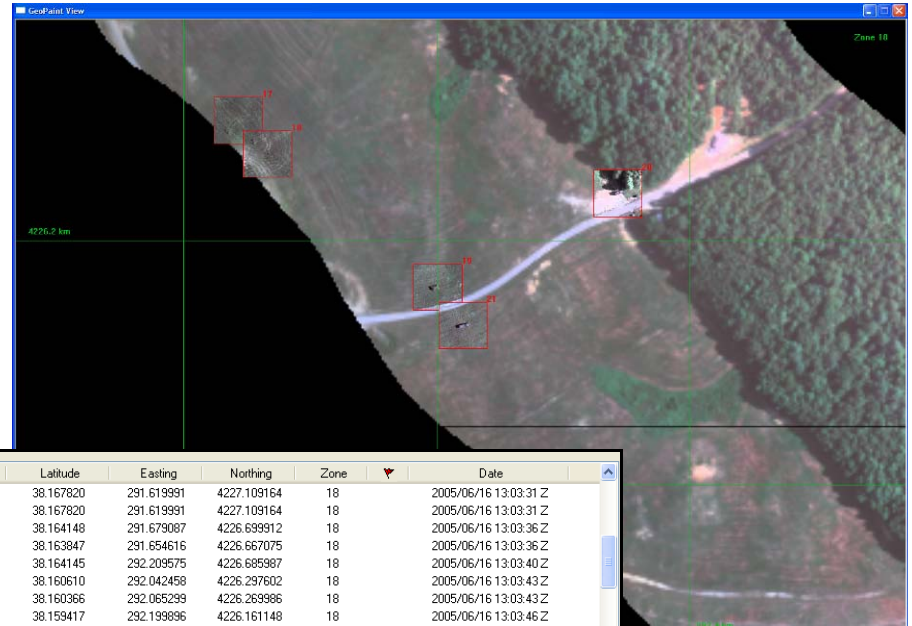
6. Receive Data Cube Image
7. Disseminate Additional Data Products

Warfighter:
1. Send Tasking
6. Receive Product



Display and Target Cue Products Generated by OBP

- **Geo-registered false color HSI**
  - **Supports GeoPaint™ display**
- **Target cue reports (text data)**
  - **Date, time, filter ID**
  - **Scan, frame, pixel indices**
  - **Lat,Lon and UTM geolocation**



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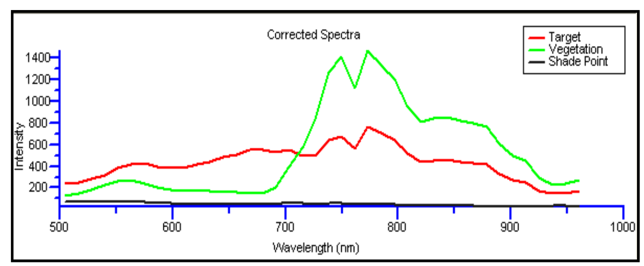
- **Target chips**
  - **ROI centered on detection**
  - **Georegistered and fused false-color HSI and HRI**
  - **Target spectra**



TacSat-3 Architecture

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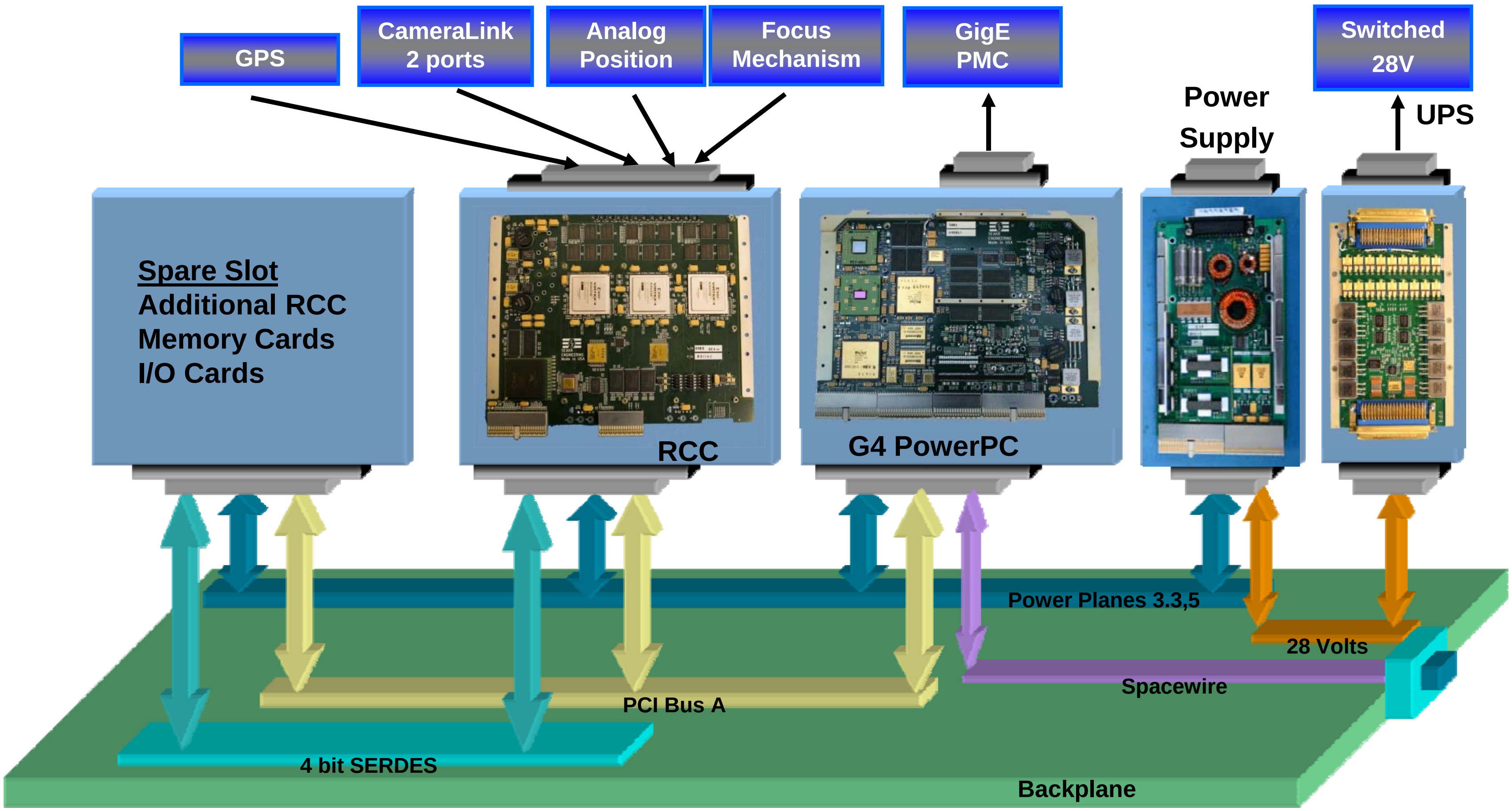

IRIS Project Overview

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- **First full-featured IP router in space**
- **Supported by Joint Capability Technology Demonstrations and commercially funded**
- **First generation spacecraft will host one C-band and two Ku-band beams IP routing between all bands and beams**
- **20 months from ATP to integration on spacecraft**
  - **Spacecraft integration testing completed January 2009**
  - **IS-14 launch scheduled for Q3 2009**
- **Additional generations planned with increasing capabilities**
- **SEAKR designed, developed IRIS hardware and was the prime integrator for Cisco's IRIS payload**

Intelsat 14 c/o SS/Loral

Background

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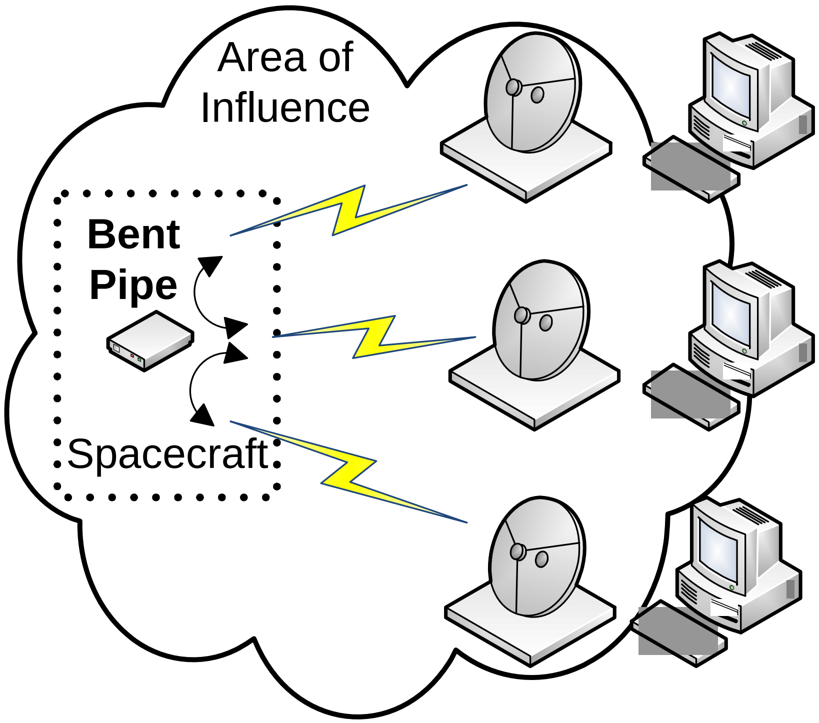
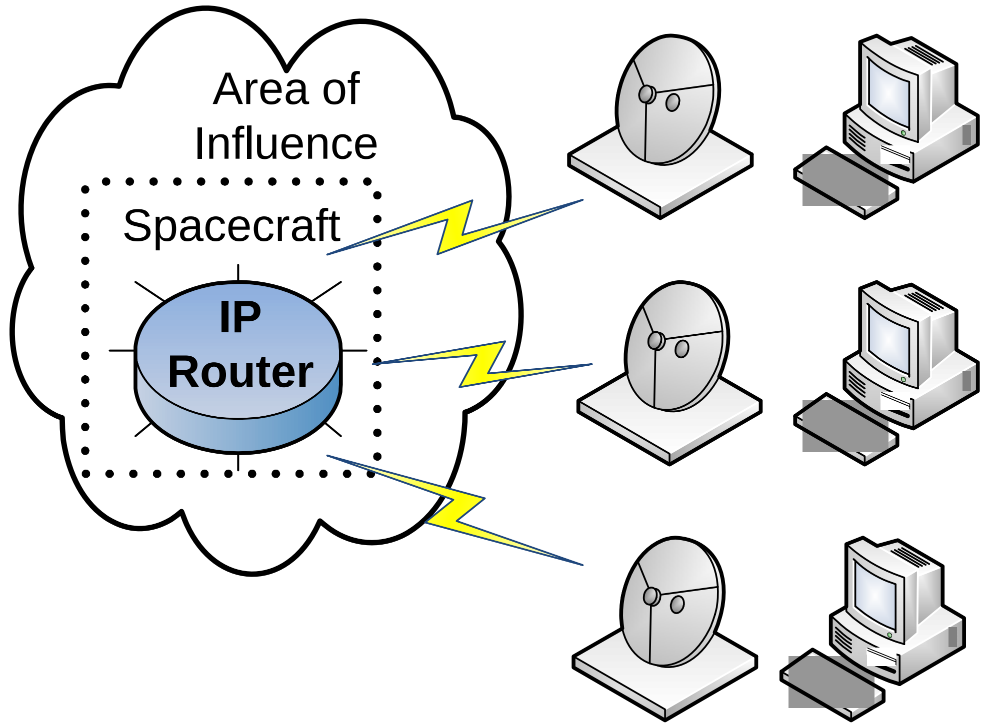


Bent Pipe Comms Satellite System



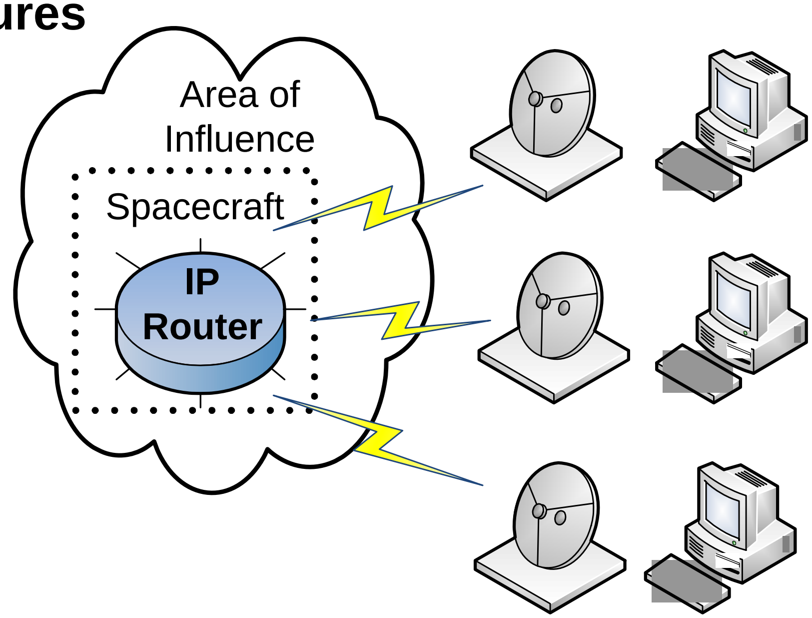
IP-based Comms Satellite System

- **Communication systems require high performance with limited faults**
- **Bent-pipe comms typically less processing complexity with limited decision making and ground-side modem often included in the overall system design**
- **IP-based systems built upon ground-based standards requiring complex routing decisions to be made onboard**

Background

☐IP-based network advantages

- Standardized protocols (above physical)
  - Built-in QoS, security and EDAC features
  - Ubiquitous and extensively deployed
  - Well understood and time tested
- Virtual circuit philosophy
  - Improves scalability and throughput
  - Decentralized multicast
  - Fine-grained QoS easy to implement
- Cost-effective test and integration
  - Numerous commercial components
  - Mature test strategies and methods



IP-based Comms Satellite System

IP in Space Challenges

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☐ Onboard Processing

- High bandwidth MODEMS and Routers require significant processing
- On-board routed payloads have advantages but come at a cost
- High performance processing on a satellite is non-trivial and costly
  - Becomes more attractive with each new processor generation

☐ Security

- Supporting Type 1 comm. while retaining IP feature set on the spacecraft
  - Packet header encryption?
  - Source/destination or packet type security
  - QoS in the face of encryption?

☐ Ground Infrastructure

- Large investment to provide upgraded facilities (but benefits are great)
- Several MODEM protocols fielded (some proprietary) for tactical users

Mission System

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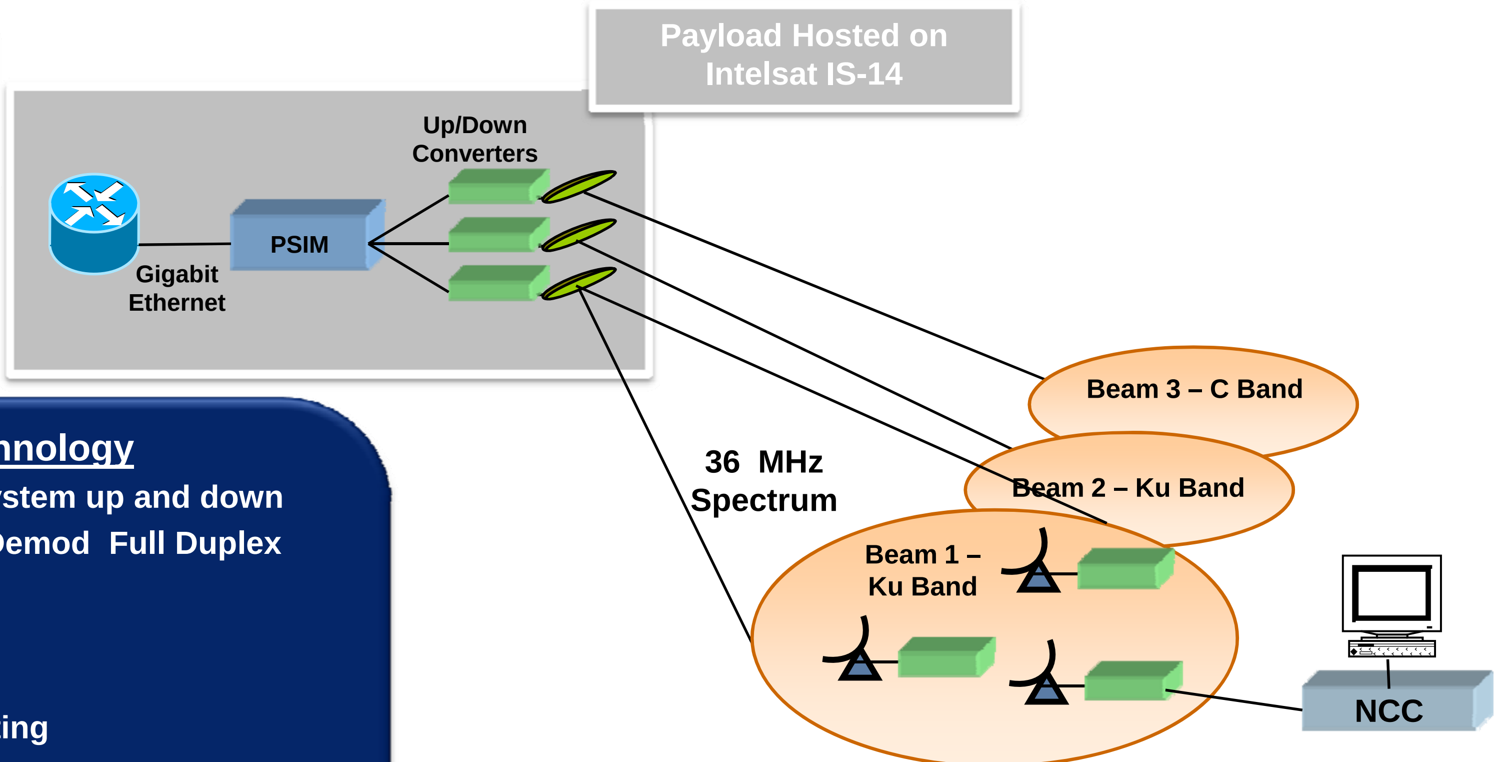
Router

- OS
- BGP



Modem Technology

- MF TDMA System up and down
- QPSK Mod/Demod Full Duplex
- Multi-Carrier
- Multi-Rate
- Multi-Cast
- Layer 3 Routing
- QOS
- Class based queuing
- Dynamic Bandwidth allocation
- RIPV2
- Processes 108 MHz of RF bandwidth
- IP based
- Supports SCPC Waveform

Completely Reconfigurable On-orbit

Performance enhancements

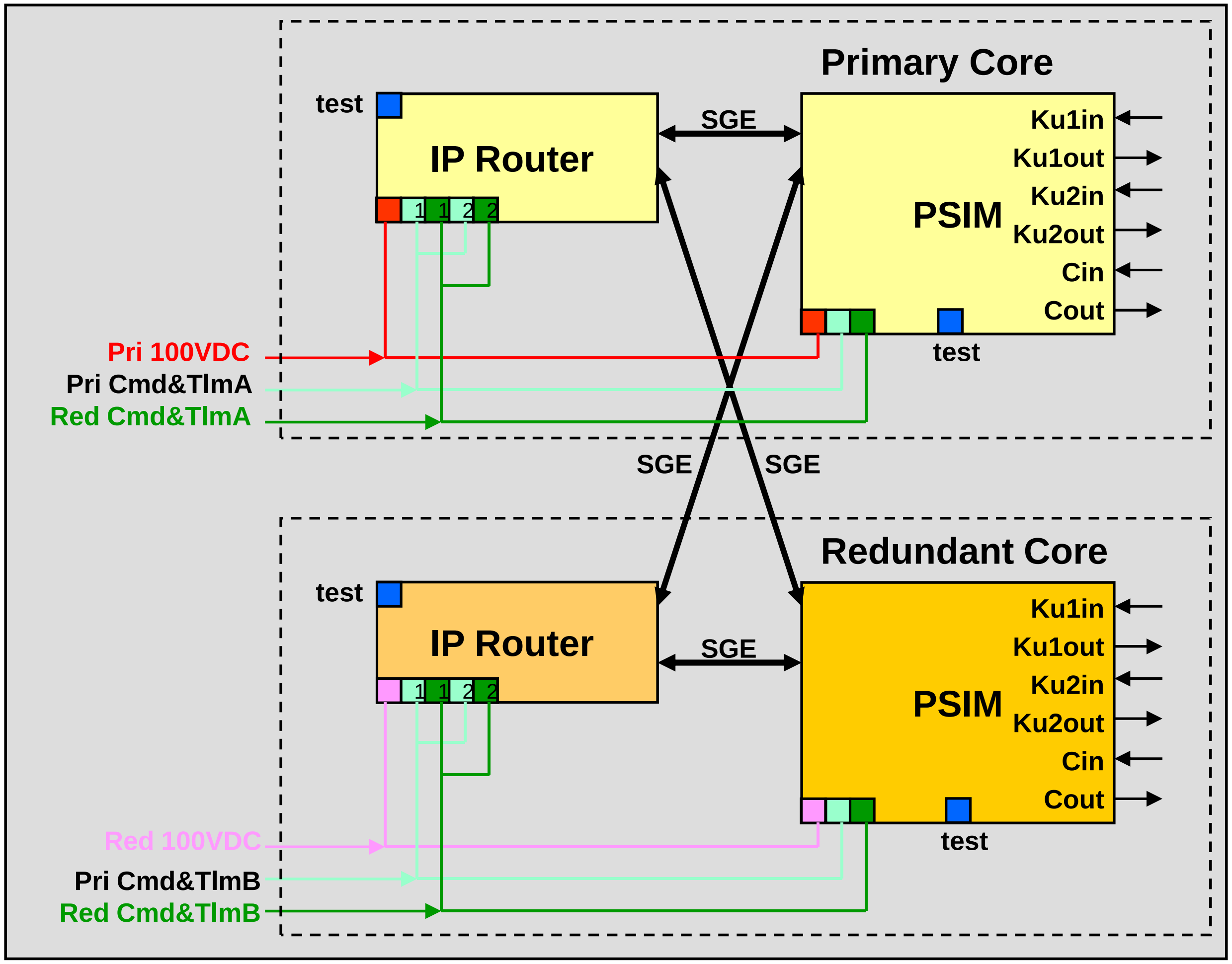
New waveform

New application code

New OS

New Router software

System Architecture



- **Box-level redundancy with per-unit fail over**

IRIS Flight Hardware

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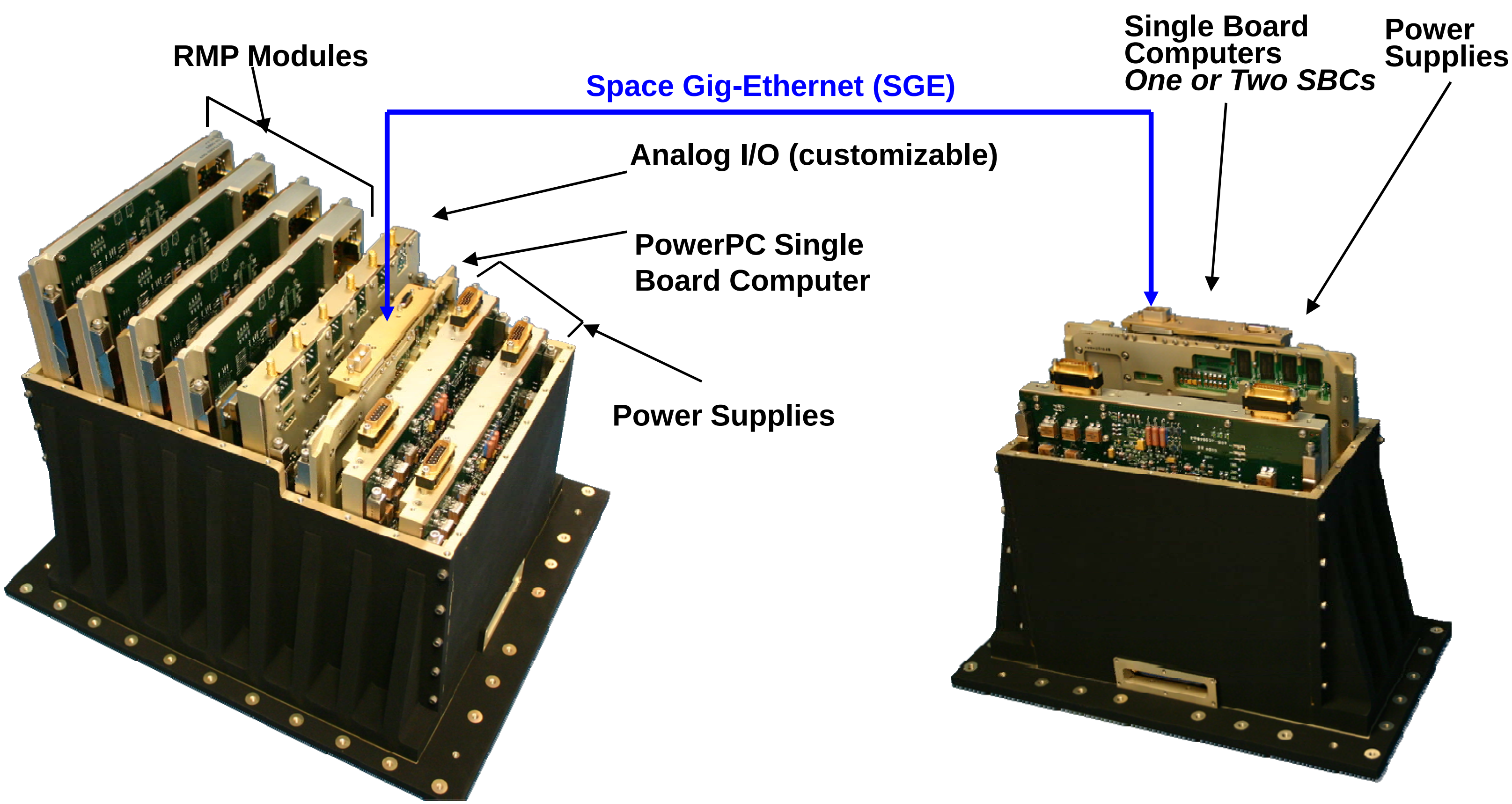
- **Combination of 2 sequential processors, 12 FPGAs and analog switch card**
  - **FPGAs provide waveform processing**
  - **Processors provide Ethernet interfaces, packet switching**
  - **Leveraging the advantages of each type of component**



IRIS Hardware Flexibility

☐Waveform and beam agile

- Design can leverage PST features for frequency agility

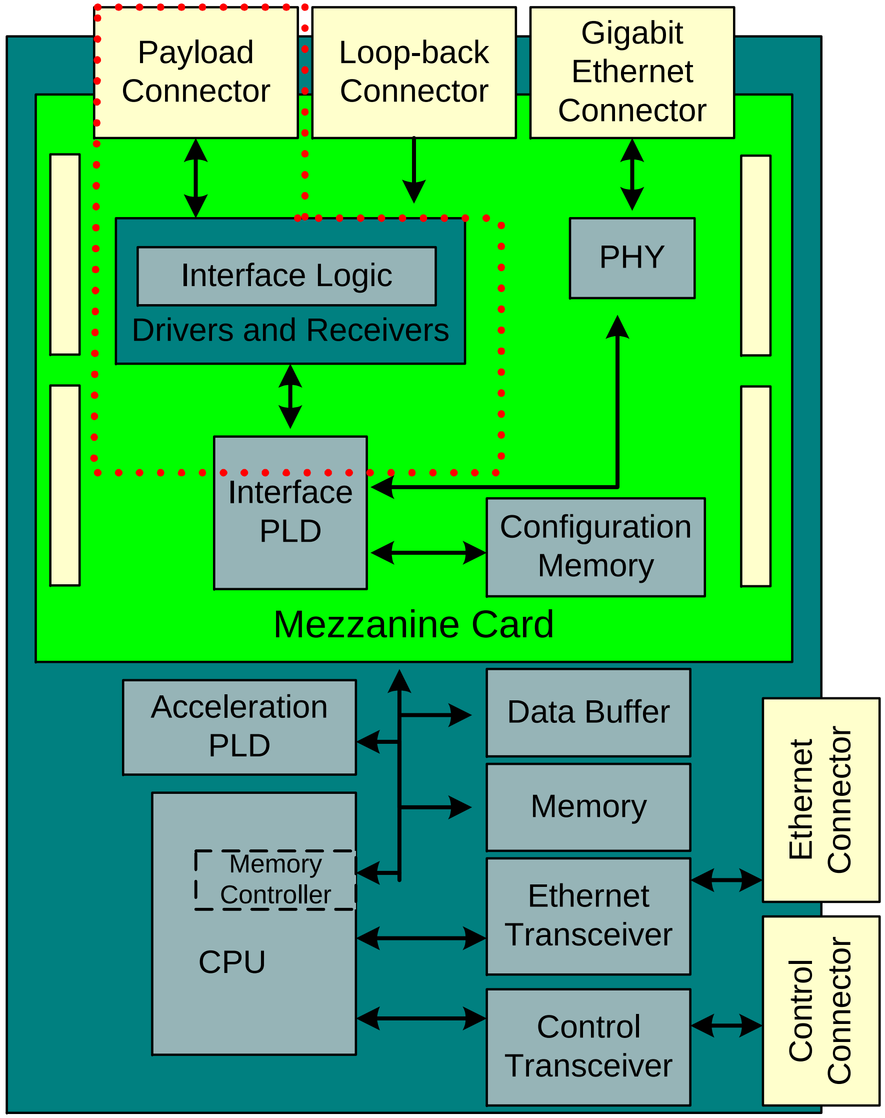
☐Numerous SEE mitigation options

- Box-level redundancy with failover
- Device-level redundancy with voter
- Intra-device full or partial redundancy
- Configuration scrubbing

☐On-orbit software reconfiguration planned as part of the mission to update routing features

RSNIC Design

- SEAKR's SGE forms the basis for the Reprogrammable Space Network Interface Card (RSNIC) payload concept
- Merging of programmable logic and general-purpose microprocessor for network interconnect "normalization"
- All functionality required for protocol translation encapsulated with the single board plus mezzanine card
- Mezzanine card designs largely stay unchanged with only the interface-specific portions requiring augmentation



RSNIC Prototype

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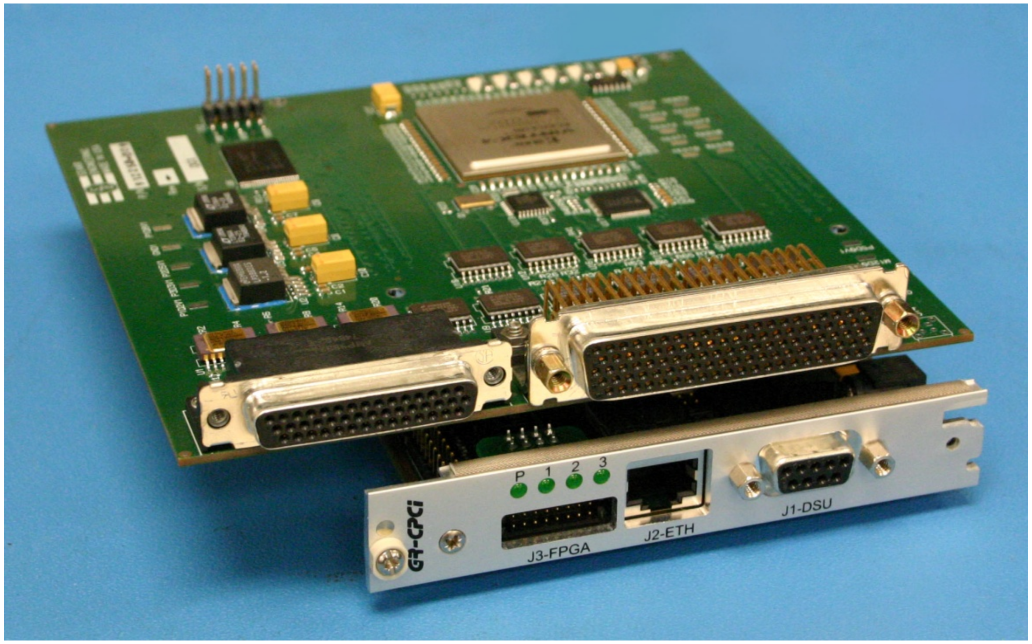
- RSNIC prototype boards developed and verified
- Ethernet and payload interfaces confirmed to be operational via loopback and PC generated traffic
  - Currently supports 300Mbps bandwidth measured using IP/UDP protocol transfers
- SSR Tech. Demonstration
  - Translated data and command traffic for the EM version of SEAKR's two-channel SSR used in NASA's Gamma-ray Large Area Space Telescope
  - Demo completed in 2008



RSNIC Prototype

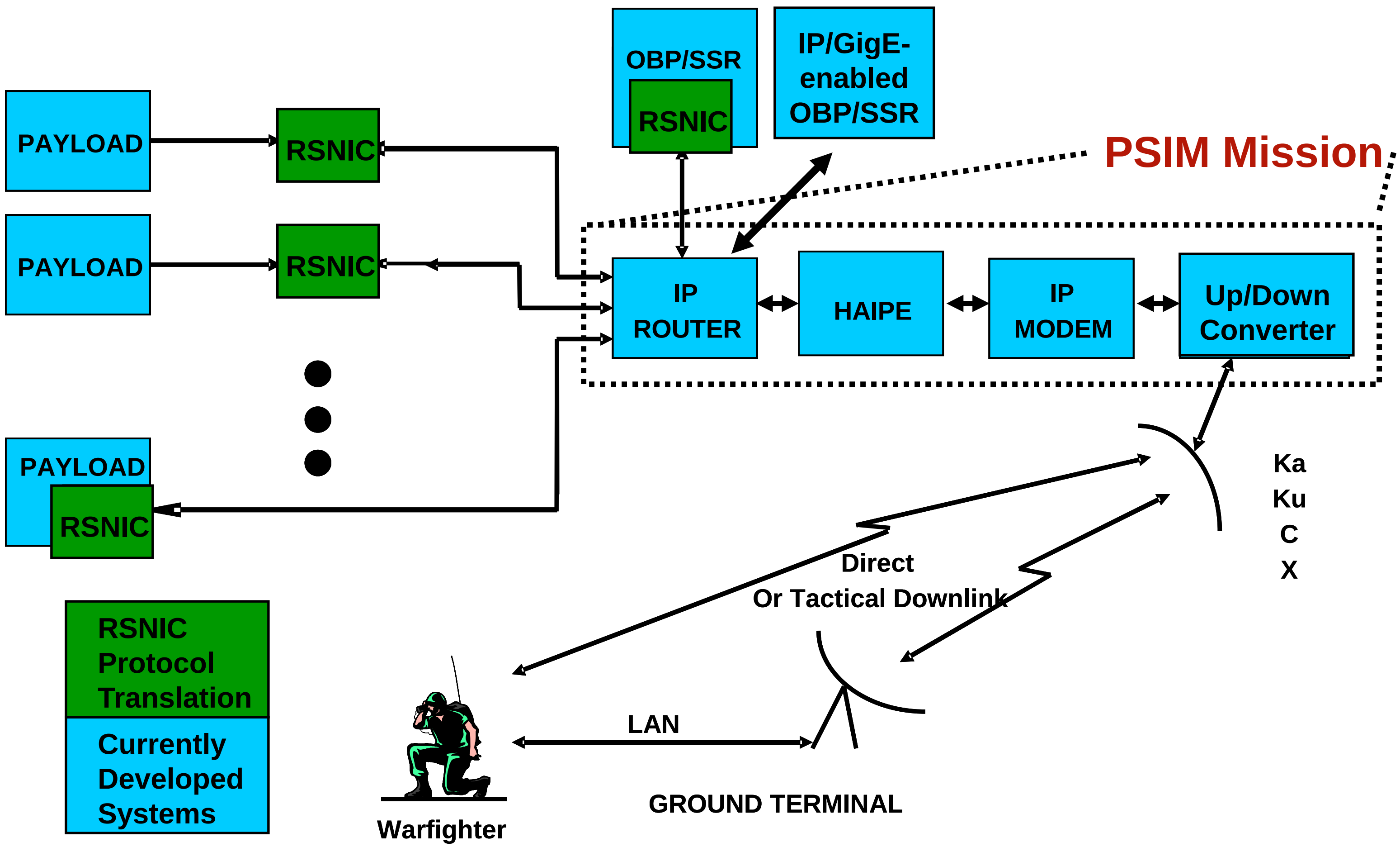
PST Mission Summary

- Programmable Satellite Transceiver (PST) provides frequency agile sat. comm.
  - Each band continuously tunable
  - Programmable on the ground and/or in flight
- AFRL Enhanced Phase-II SBIR with EM delivered Q2'08

PST Configuration of AIP

- Receiver/Uplink
  - L-Band 1760 to 1840 MHz
  - S-Band 2025 to 2120 MHz
- Transmitter/Downlink
  - S-Band 2200 to 2300 MHz
- Space Ground Link System (SGLS)
  - FSK-AM Command Uplink (1 kbps, 2 kbps)
  - Subcarrier BPSK Telemetry Downlink (256 kbps)
- Universal S-Band (USB)
  - Subcarrier BPSK Command Uplink (<= 4 kbps)
  - Subcarrier BPSK Telemetry Downlink (256 kbps)
- Future Waveforms in development
- Partnered with RT Logic

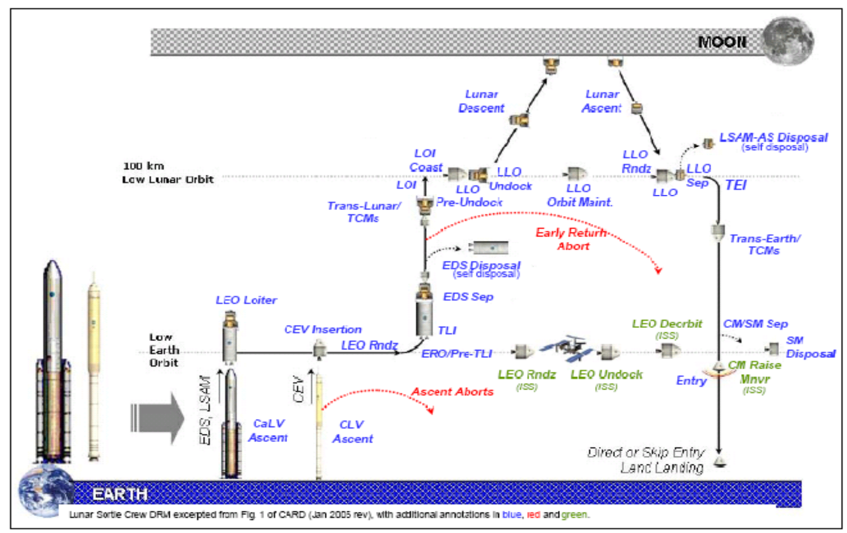
IP-enabled Payload



- **Legacy protocol to IP/Ethernet translation to improve performance and scalability and enable plug-and-play payload design**

Orion-VPU Mission Summary

- ☐ **VPU provides a reconfigurable hardware platform for processing image algorithms**
  - **Pose Estimation**
  - **Optical Navigation**
  - **Compression/Decompression**
- ☐ **Receives image data from various Relative Navigation Sensors**
  - **Star Tracker**
  - **Vision Navigation Sensor**
  - **Docking Camera**
  - **Situational Awareness Camera**
- ☐ **Supports rendezvous, proximity operations, docking and un-docking for ISS and Lunar missions**



Images c/o Orion Program Office, NASA-Glenn

ORION-VPU Highlights

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☐ Combination of sequential processor and RCC

- Xilinx® FPGAs deployed in TMR for critical sensor algorithms
  - Video processing algorithms (i.e. feature recognition, graphical overlay, tiling, etc.) and video compression video
- Microblaze™ core coordinates algorithm cores and processor communication
- LEON™ SBC dedicated to system coordination, error handling, RCC configuration and oversight and interconnect control
  - Time-Triggered Gigabit Ethernet PMC and RS422

☐ Mezzanine card provides sensor interfaces

- LVDS interfaces with access to all three FPGAs for flexibility in video stream selection and mitigation schemes

☐ Configuration scrubbing and TMR for RCC SEU mitigation

- Corrects control path corruptions

Conclusions

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- Application Independent Processor developed for space
  - Supports the responsive space mission (e.g. TacSat-3)
  - Reconfigurable on-orbit
  - Flexible, scalable architecture
- Mission performance reqs driving the use of commercial devices
  - Low cost, high performance
  - Designed for multiple missions
- Several disparate missions demonstrate design's flexibility
  - Various high-performance onboard processing
  - Spacecraft communications systems (waveform and IP routing)
- Incorporating time-tested commercial protocols into space systems can provide cost-effective performance improvements

Contact Information

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