# Rad Hard By Software for Space Multicore Processing

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# Outline

- Rad Hard By Software Overview
- ST8 Dependable Multiprocessor
- Next-Generation Dependable Multiprocessor Testbed
- Performance Results
- Conclusions and Future Work

# Why Rad Hard By Software?

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- Future payloads can be expected to require high performance data processing

- Traditional component hardening approaches to rad hard processing suffer several key drawbacks
  - Large capability gap between rad hard and COTS processors
  - Poor SWaP characteristics vs. processing capacity
  - Extremely high cost vs. processing capacity
  - Dissimilarity with COTS technology drives high-cost software development units

- Honeywell Rad Hard By Software (RHBS) approach solves these problems by moving most data processing to high performance COTS single board computers
  - Leading edge capability
  - Software fault mitigation = less hardware = reduced SWaP
  - Inexpensive
  - No difference between development and flight hardware
  - COTS software development tools and familiar programming models

# DM Technology Advance: Overview

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- **A high-performance, COTS-based, fault tolerant cluster onboard processing system that can operate in a natural space radiation environment**

**NASA Level 1 Requirements (Minimum)**

- **high throughput, low power, scalable, & fully programmable >300 MOPS/watt (>100)**
- **high system availability >0.995 (>0.95)**
- **high system reliability for timely and correct delivery of data >0.995 (>0.95)**
- **technology independent system software that manages cluster of high performance COTS processing elements**
- **technology independent system software that enhances radiation upset tolerance**

**Benefits to future users if DM ST8 experiment is successful:**

- 10X – 100X more delivered computational throughput in space than currently available
- enables heretofore unrealizable levels of science data and autonomy processing
- faster, more efficient applications software development
  - robust, COTS-derived, fault tolerant cluster processing
  - port applications directly from laboratory to space environment
    - MPI-based middleware
    - compatible with standard cluster processing application software including existing parallel processing libraries
- minimizes non-recurring development time and cost for future missions
- highly efficient, flexible, and portable SW fault tolerant approach applicable to space and other harsh environments
- DM technology directly portable to future advances in hardware and software technology

# Next Generation DM Testbed

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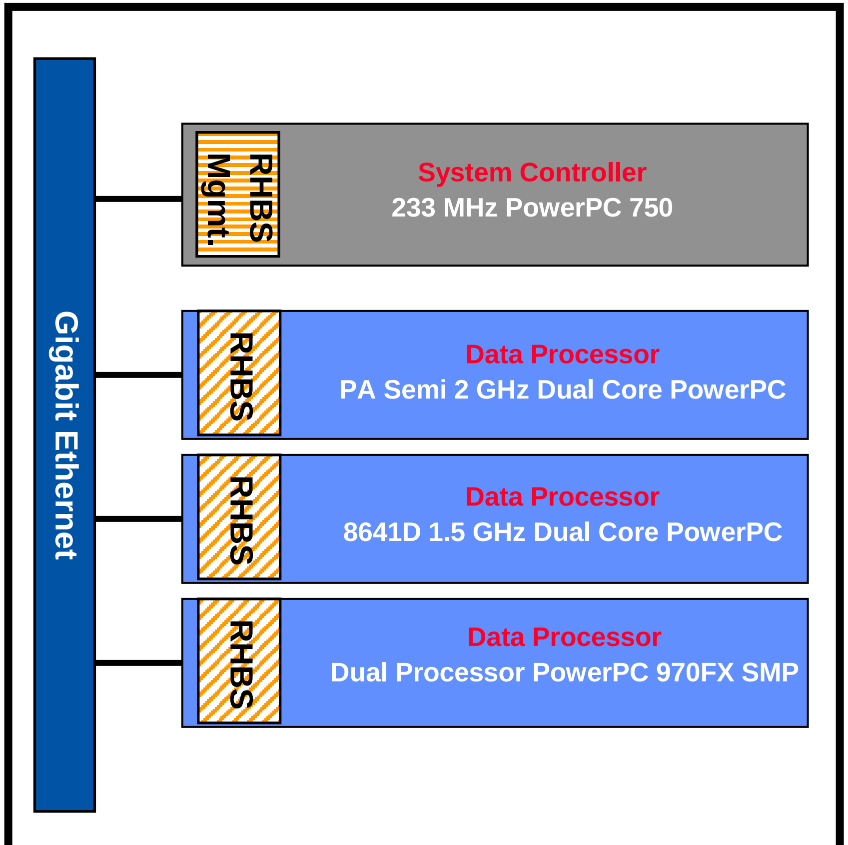
- Dependable Multiprocessor (DM) is Honeywell's first-generation Rad Hard By Software technology
- Coarse-grained software-based fault detection and recovery
  - Similar to the way modern communication protocols detect errors at the packet level rather than the byte level
  - Rad Hard By Software detects errors at the "operation" rather than the instruction level
- Typical system
  - One low-performance rad-hard SBC for "cluster" monitoring and severe upset recovery
    - Could also serve as spacecraft control processor
  - One or more high-performance COTS SBCs for data processing
    - Connected via high-speed interconnects
  - One or more fault-tolerant storage/memory cards for shared memory
  - Dependable Multiprocessing (DM) software stack



Honeywell Next-Generation DM Testbed

*This work applies DM to multicore/multiprocessor targets including the PA Semi PA6T-1682M, Freescale 8641D, and IBM 970FX*

# DMM Software Stack

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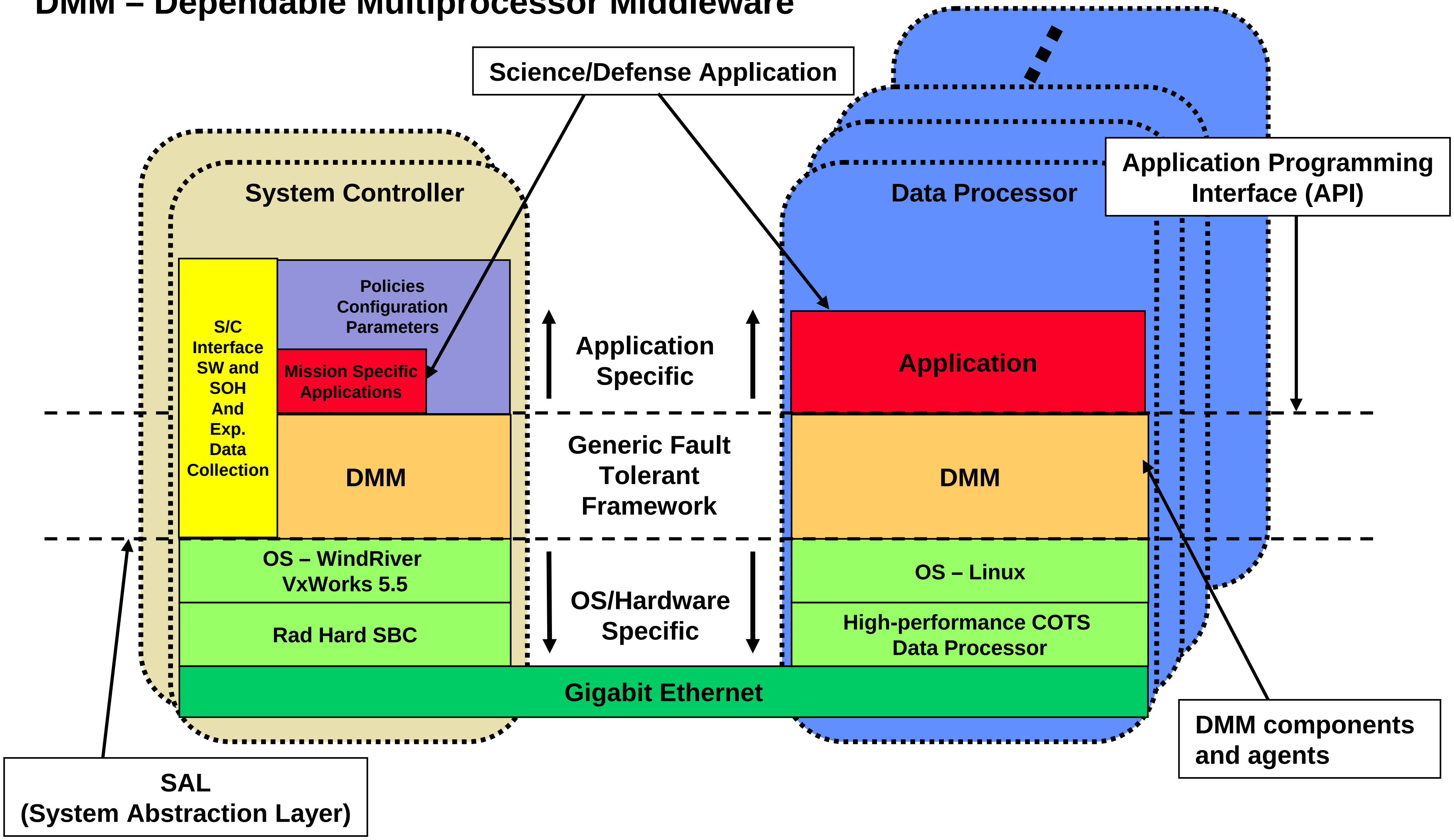
## DMM – Dependable Multiprocessor Middleware



# Application Benchmark Overview

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- FFTW
  - 1K-, 8K-, or 64K-point radix-2 FFT (FFTW1K, FFTW8K, FFTW64K)
  - Single-precision floating point
  - Supports multi-threading via small alterations (~5 lines) to application source code and linking multi-threaded FFTW library
- Matrix Multiply
  - 800x800 and 3000x3000 variants (MM800/MM3000)
  - Single-precision floating point
  - Uses ATLAS/BLAS linear algebra libraries
  - Supports transparent multi-threading by linking the pthreads version of the BLAS library
- Hyper-Spectral Imaging (HSI) detection and classification
  - 256x256x512 data cube
  - Single-precision floating point
  - Uses ATLAS/BLAS linear algebra libraries
  - Supports transparent multi-threading by linking the pthreads version of the BLAS library

# Application Performance Results

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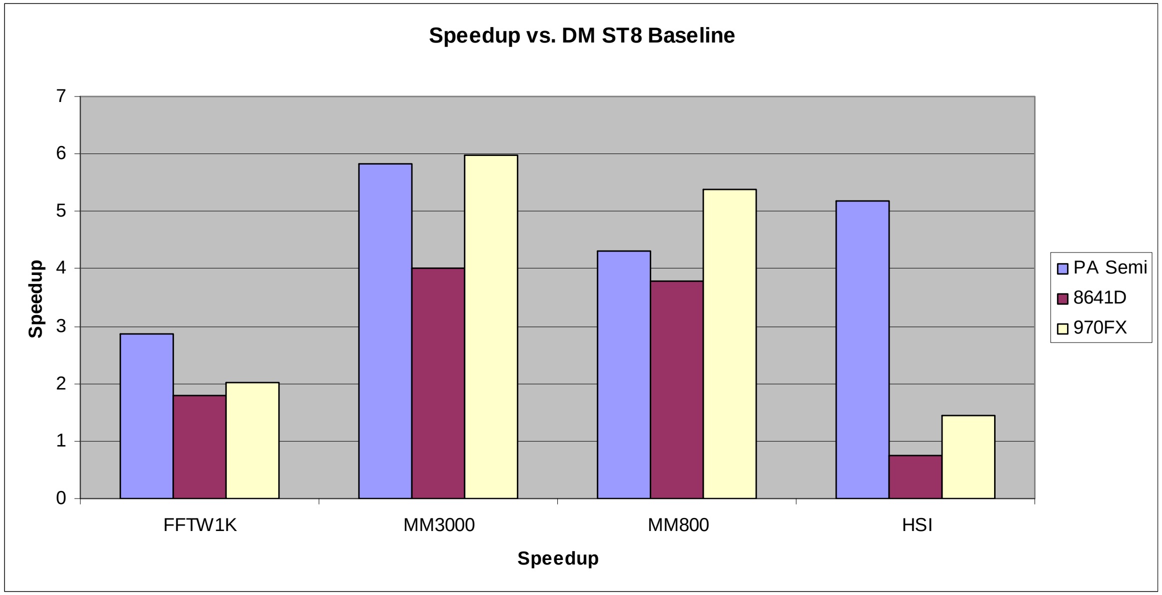
- Next-gen architectures provide significant performance improvement over existing DM 7447A (ST8 Baseline) for each application
- Largest speedups on large matrix multiply
  - Best exploits parallelism in multi-core architectures
- FFTW does not efficiently exploit both processor cores, limiting speedup
- PA Semi provides 5x performance of DM ST8 baseline for HSI application
  - Advantage over 8641D and 970FX for HSI largely due to custom-built ATLAS 3.8.2 BLAS library for PA Semi vs. 3.5.1 precompiled binary library for others



# One-Thread vs. Two-Thread PA Semi Results

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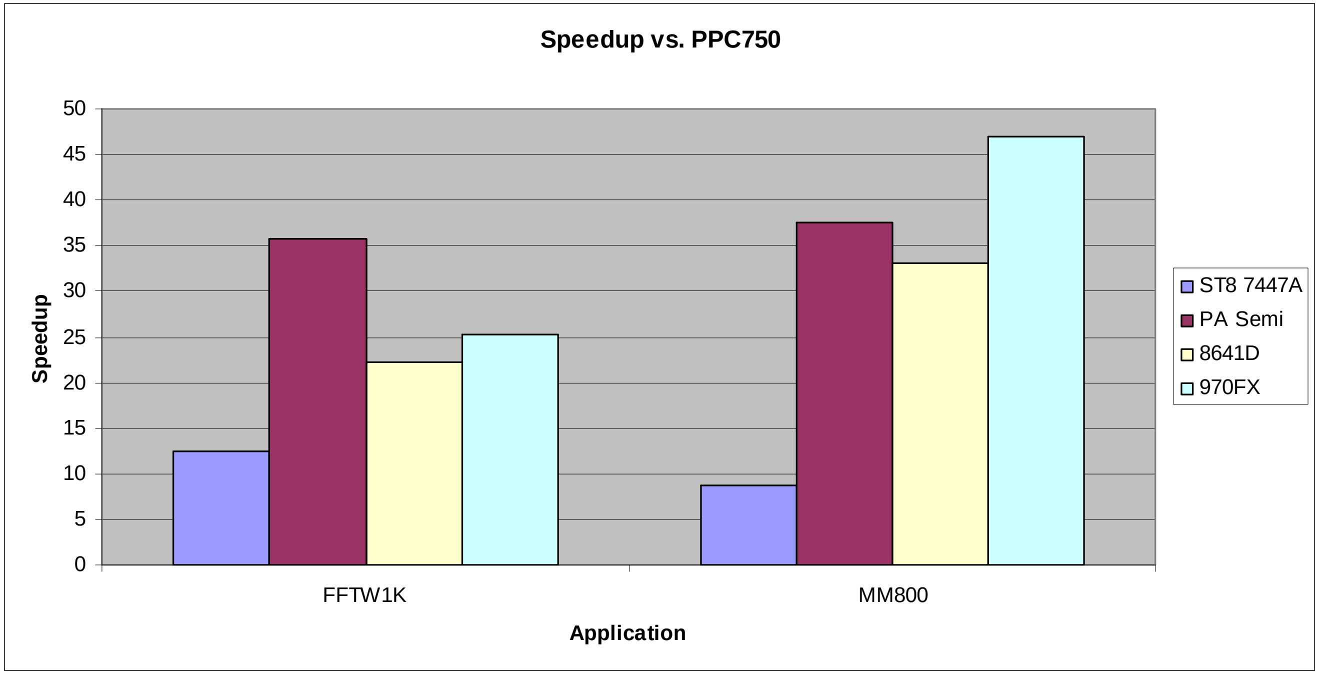
- Nearly 2x speedup provided for 3000x3000 matrix multiply
  - Smaller matrix multiply suffers due to dataset size
- HSI application speedup limited to 1.63x by highly serialized Weight Computation stage
  - Autocorrelation Sample Matrix (ACSM) and Target Classification stages take advantage of both cores fairly efficiently
- FFTW actually slowed down for multi-core implementations
  - Suspect likely due to inefficiencies in fine-grain parallelization of 1D FFT, expect much better performance for 2D FFTs with coarse-grain parallelization
- Similar trends observed on 8641D (and 970FX SMP with 2 processors)

| Dual-Threaded PA Semi Speedup (Slowdown) vs. Single-Threaded PA Semi | | | | | |
|---|---|---|---|---|---|
| MM800 | MM3000 | HSI | FFTW1K | FFTW8K | FFTW64K |
| 1.64 | 1.93 | 1.63 | (6.10) | (1.41) | (1.05) |

# Comparison to "State-of-the-Art" for Space



- Reference architecture is a 233 MHz PowerPC 750 with 512 KB of L2 cache
- Base DM system provides ~10x speedup over PPC750 for FFTW and MM800
- More modern architectures improve upon this speedup by 2-4x
- Other applications did not run on PPC750 due to memory limitations



# Estimated Throughput Density

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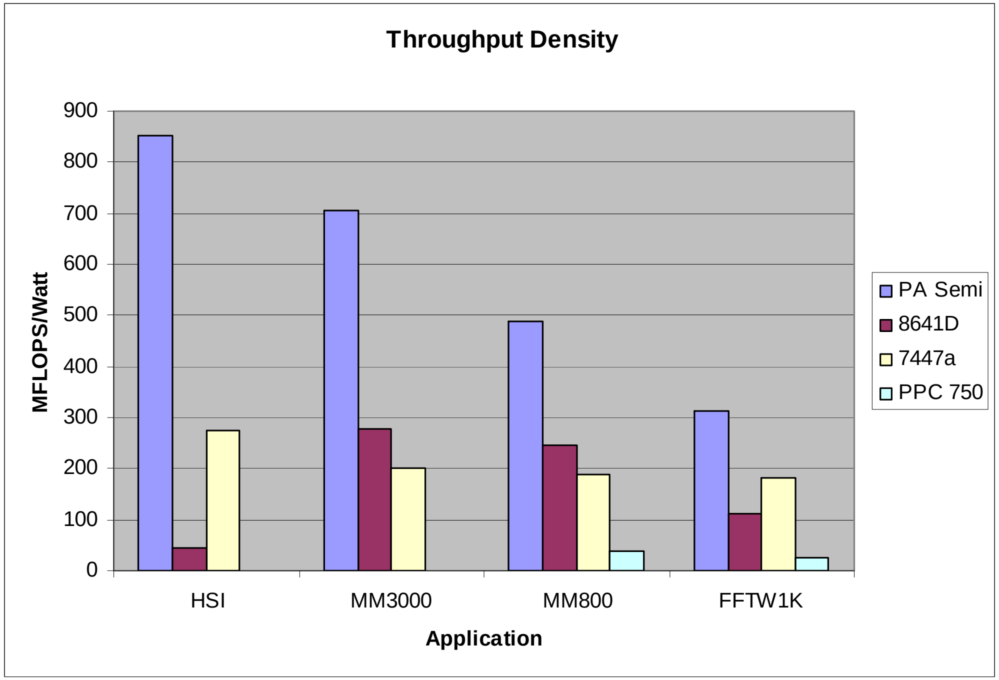
- **PA Semi provides significant throughput density enhancements vs. 8641D and ST8 7447a**
- **All architectures provide 1+ order of magnitude throughput density enhancement vs. PPC 750**
- **HSI throughput density conservative in most cases**
  - **Op count only includes ACSM stage which accounts for ~90% of execution time, but time includes all compute stages**
  - **8641D version still suffers due to older ATLAS library**

- **Assumes:**
  - **12W for 7447A board**
  - **20W for PA Semi board**
  - **35W for 8641D board**
  - **7W for 233 MHz PPC 750 board**
- **970FX not appropriate for space systems and not included**



# Summary

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- **DM provides a low-overhead approach for increasing availability and reliability of COTS hardware in space**
  - **DM easily portable to most Linux-based platforms**
  - **7447a processing platform selected near start of NASA/JPL ST8 program (DM), but better options now exist**

- **Modern processing platforms provided impressive overall speedups for existing DM applications *with no additional development effort***
  - **~5-6x speedup vs. existing 7447a-based DM platform**
    - **Leverages optimized libraries for SIMD and multiprocessing**
  - **~2-3x gain in throughput density (MFLOPS/W) vs. existing DM solution**
  - **~20-40x performance of state-of-the-art rad hard by process solutions**

- **Potential future work**
  - **Exploration of high-speed networking technologies with DM**
  - **Enhancements to DM middleware for performance/availability/reliability**
  - **Explore options for using additional cores to increase reliability**

- **Explore additional general purpose multicore next-generation processing engines**
  - **Purchase of PA Semi by Apple potentially makes it a less attractive solution**
  - **New Freescale 2- and 8-core devices at 45nm are a possible alternative**

- **Explore port of DM to advanced multicore architectures**
  - **Tilera TILE64**
  - **Cell Broadband Engine**
  - **Further evaluation of future processing platforms (rad testing, etc.)**

***DM enables high-performance space computing with modern COTS processing engines***