Fixed and Reconfigurable Multi-Core Device Characterization for HPEC

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Outline

• Background
• RC Taxonomy
• Reconfigurability Factors
• Computational Density Metrics
• Internal Memory Bandwidth Metric
• Results & Analysis
• Future Work
• Conclusions
Background

- Moore’s law continues to hold true, transistor counts doubling every 18 months
  - But can no longer rely upon increasing clock rates ($f_{\text{clk}}$) and instruction-level parallelism (ILP) to meet computing performance demands

- How to best exploit ever-increasing on-chip transistor counts?
  - Architecture Reformation: Multi- & many-core (MC) devices are new technology wave
  - Application Reformation: focus on exploiting explicit parallelism in these new devices
Background

• What MC architecture options are available?
  o **Fixed MC**: fixed hardware structure, cannot be changed post-fab
  o **Reconfigurable MC**: can be adapted post-fab to changing problem req’s

• How to compare disparate device technologies?
  o Need for taxonomy & device analysis early in development cycle
  o Challenging due to vast design space of FMC and RMC devices
  o We are developing a suite of metrics; two are focus of this study:
    o **Computational Density per Watt** captures computational performance and power consumption, more relevant for HPEC than pure performance metrics
    o **Internal Memory Bandwidth** describes device’s on-chip memory access capabilities
Devices with segregated RMC & FMC resources; can use either in stand-alone mode.
Reconfigurability Factors

Datapath
- Register + Register
- Register × Register
- Register

Device Memory
- 64 KB × 64
- PE

PE/Block
- 8 × 8 MAC (Processing Element)
- 24 × 24 Multiply (Processing Element)

Interface
- RC Device
- RLDRAM Memory Controller
- RLDRAM SDRAM

Mode
- PE1 Prg-A
- PE2 Prg-A
- PE3 Prg-A
- PE4 Prg-A

Power
- PE
- PE
- PE
- PE
- PE
- PE
- Performance
- Power

Interconnect
- PE
- MEM
- PE
- MEM
## Metric Overview

- **Metric Description**
  - Computational Density (CD)
    - Measure of computational performance across range of parallelism, grouped by process technology
  - Computational Density per Watt (CDW)
    - CD normalized by power consumption
  - Internal Memory Bandwidth (IMB)
    - Describes device’s memory-access capabilities with on-chip memories
- **CD & CDW Precisions (5 in all)**
  - Bit-Level, 16-bit Integer, 32-bit Integer, Single-Precision Floating-Point (SPFP), and Double-Precision Floating-Point (DPFP)
- **IMB**
  - Block-based vs. Cache-based systems

### Devices Studied (18)

<table>
<thead>
<tr>
<th>Devices Studied (18)</th>
<th>130 nm FMC</th>
<th>90 nm RMC</th>
<th>90 nm FMC</th>
<th>65 nm RMC</th>
<th>45 nm FMC</th>
<th>40 nm RMC</th>
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<tbody>
<tr>
<td></td>
<td>Raytheon MONARCH</td>
<td>Raytheon MONARCH</td>
<td>Xilinx Virtex-4 LX200</td>
<td>Xilinx Virtex-5 LX330T</td>
<td>Intel Atom N270(^2)</td>
<td></td>
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<tr>
<td></td>
<td>Tilera TILE64</td>
<td>Xilinx Virtex-4 SX55</td>
<td>Xilinx Virtex-5 SX95T</td>
<td>Xilinx Virtex-5 SX95T</td>
<td>Altra Stratix-IV EP4SE530</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Freescale MPC8640D</td>
<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
</tbody>
</table>

\(^1\) Preliminary results based on limited vendor data (Ambric)
\(^2\) Limited Atom cache data, not included in IMB results
**Metric Methodology**

- **CD for FPGAs**
  - **Bit-level**
    - $f_{\text{max}}$ is max device frequency, $N_{\text{LUT}}$ is number of look-up tables, $W_i$ & $N_i$ are width & number of fixed resources
  - **Integer**
    - Use method on right with Integer cores
  - **Floating-point**
    - Use method on right with FP cores

\[
CD_{\text{bit}} = f_{\text{max}} \times \left[ N_{\text{LUT}} + \sum_i W_i \times N_i \right]
\]

**Overhead** - Reserve 15% logic resources for steering logic and memory or I/O interfacing

**Memory-sustainable CD** – Limit CD based on # of parallel paths to on-chip memory; each operation requires 2 memory locations

**Parallel Operations** – scales up to max. # of adds and mults (# of adds = # of mults)

**Achievable Frequency** – Lowest frequency after PAR of DSP & logic-only implementations of add & mult computational cores

**IP Cores** – Use IP cores provided by vendor for better productivity

- **Integer & Floating-Point Analysis**
  - Determine maximum amount of logic resources & maximum amount of special on-chip resources (e.g. DSP multipliers), for device
  - Determine resource utilization & maximum achievable frequency for one instance of core using DSP resources; repeat using logic-only resources
  - Determine number of simultaneous cores, $O_{\text{DP}}$, that can be instantiated until all DSP resources are exhausted; repeat for logic-only resources to determine $O_{\text{LOGIC}}$
  - Achievable frequency $f_{\text{achievable}}$ is lower of frequencies determined in step 2 above
  - Iterate through combinations of DSP and logic-only cores to find an equal balance of addition and multiplication operations
Metric Methodology

- CD for FMC and coarse-grained RMC devices
  - Bit-level
  - Integer
  - Floating-point

- CDW for all devices
  - Calculated using CD for each level of parallelism and dividing by power consumption at that level of parallelism
  - CDW is critical metric for HPEC systems

\[
CD_{\text{bit}} = f \times \left[ \sum_i W_i \times N_i \right]
\]

\[
CD_{\text{int/FP}} = f \times \sum_i \frac{N_i}{CPI_i}
\]

- For all RMC
  - Power scales linearly with resource utilization

- For FPGAs
  - Vendor tools (PowerPlay, Xpower) used to estimate power for maximum LUT, FF, block memory, and DSP utilization at maximum freq.
  - Maximum power is scaled by ratio of achievable frequency to maximum freq.

- For all FMC
  - Use fixed, maximum power from vendor documentation

symbols:
- \( W_i \): width of element type \( i \)
- \( N_i \): # of elements of type \( i \), or # of instructions that can be issued simultaneously
- \( f \): clock frequency
- \( CPI_i \): cycles per instruction for element \( i \)
**Metric Methodology**

- **Internal Memory Bandwidth (IMB)**
  - Overall application performance may be limited by memory system
  - **Cache-based systems (CBS)**
    - Separate metrics for each level of cache
    - Calculate bandwidth over range of hit rates
  - **Block-based systems (BBS)**
    - Calculate bandwidth over a range of achievable frequencies
    - For fixed-frequency devices, IMB is constant
    - Assume most parallel configuration (wide & shallow configuration of blocks)
    - Use dual-port configuration when available

\[
IMB_{\text{cache}} = \%\text{hitrate} \times \sum \frac{N_i \times P_i \times W_i \times f_i}{8 \times CPA_i}
\]

\[
IMB_{\text{block}} = \sum \frac{N_i \times P_i \times W_i \times f_i}{8 \times CPA_i}
\]

- **%hitrate** - Hit-rate scale factor
- **\( N_i \)** - # of blocks of element \( i \)
- **\( P_i \)** - # of ports or simultaneous accesses supported by element \( i \)
- **\( W_i \)** - width of datapath
- **\( f_i \)** - memory operating frequency, variable for FPGAs
- **\( CPA_i \)** - # of clock cycles per memory access
### Maximum memory-sustainable CD is shown above (in GOPs)

- CD scales with parallel operations
- Various devices may have their highest CDs at different levels of parallelism
- Top CD performers are highlighted
- RMC devices perform best for bit-level & integer ops, FMC for floating-point
- Memory-sustainability issues seen when many, small registers are needed

<table>
<thead>
<tr>
<th>Device</th>
<th>Bit-level</th>
<th>16-bit Int.</th>
<th>32-bit Int.</th>
<th>SPFP</th>
<th>DPFP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Arrix FPOA</td>
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<td>6144</td>
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</tbody>
</table>

- **RMC**
- **FMC**
• RMC devices (specifically FPGAs) far outperform FMC devices
  • High bit-level CD due to fine-grained, LUT-based architecture
  • Low power
  • Power scaling with parallelism (area)

• **EP4SE530 (Stratix-IV) is best overall**
  • 65 nm FPGAs are all strong performers
  • V4 LX200 top performer of 90 nm devices
  • Coarse-grained devices (both RMC & FMC) show poor performance
RMC devices outperform FMC
- Low power
- Power scaling with parallelism (area)
- Requires algorithms that can take advantage of numerous parallel operations
- Ambric (130 nm) shows promising prelim. results despite older process

Virtex-4 SX55 is best performer in 90 nm class
- Strong performance from ECA-64 due to extremely low power consumption (one Watt at full utilization), despite low CD
- FPOA gives good, moderate performance due to high CD, but with higher power requirements
- **Virtex-5 SX95T (65 nm) is best overall with Stratix-IV EP4SE530 (40 nm) a close second**
RMC devices outperform FMC
- Low power
- Power scaling with parallelism (area)
- Requires algorithms that take advantage of numerous parallel operations
- Ambric (130 nm) shows promising prelim. results despite older process

For high levels of exploitable parallelism, the Virtex-4 SX55 is best in 90 nm class
- Strong performance from ECA-64 due to extremely low power consumption
- **Virtex-5 SX95T (65 m) is best overall**
- SX devices benefit from low power consumption due to high DSP-to-logic ratio
**SPFP CDW**

- RMC devices (specifically FPGAs) outperform FMC devices
  - Low power, especially FPGAs with large amount of DSP multiplier resources (consume less power than LUTs)
  - Power scaling with parallelism (area)
  - Devices not intended for floating-point computation (i.e. not designed to compete in current form) are excluded here (e.g. FPOA, TILE, ECA, Ambric)

  Note: we expect Altera FP CDW scores to improve when their new Floating-Point Compiler is used in place of current FP cores

- CSX600 modest due to average CD, low power
- Virtex-4 SX55 leads 90 nm due to power advantage
- Cell (90 nm) has large CD advantage, but very high power consumption hampers CDW capability
- **Virtex-5 SX95T (65 nm) has clear CDW advantage due to relatively high achievable frequency, high level of DSP resources, low power consumption of DSPs**
• RMC devices (specifically FPGAs) outperform most FMC devices
  • Low power, especially FPGAs with large amount of DSP multiplier resources (consume less power than LUTs)
  • Power scaling with parallelism (area)
  • Devices not intended for floating-point computation are again excluded

Note: we expect Altera FP CDW scores to improve when their new Floating-Point Compiler is used in place of current FP cores
• Block-based devices (specifically FPGAs) outperform cache-based devices
  • Many parallel paths to memory blocks
  • Can pack operands into wide data structures
  • Support for dual-port memories
  • Outperforms cache-based devices even on low frequency designs
  • IMB is constant for block-based fixed-frequency devices

• Cache-based systems (CBS)
  • MPC7447, MPC8640D perform poorly relative to most BBS devices
  • TILE64 (64 caches) does not compete with FPGAs

• Block-based systems (BBS)
  • **FPGAs dominate this metric**
  • Stratix-IV (40 nm) leads for higher-frequency designs, Virtex-5 leads for lower-frequency designs
Future Work

- Compare algorithms using Computational Intensity (CI) metric

\[ CI = \frac{\text{Arithmetic Operations}}{\text{Memory Operations}} \]

- Use CD, IMB, and CI metrics to correlate device characteristics and application characteristics

Application Metrics

- Degree of Parallelism
- Computational Intensity

Device Metrics

- Computational Density or CDW
- Internal Memory Bandwidth

Device Recommendation

Long-Term Goals

2D-Convolution (I = Image size and s = filter size)
- For I = 512; s = 3; Computational Intensity = 9.9
- For I = 512; s = 7; Computational Intensity = 8.9
- For I = 512; s = 15; Computational Intensity = 8.5

CFAR - Computational Intensity = 2.1
Radix-4 FFT - Computational Intensity = 4.7
Direct Form FIR - Computational Intensity = 4.1
Matrix Multiply - Computational Intensity = 2.0
# Summary

<table>
<thead>
<tr>
<th>Best Overall</th>
<th>Best RMC</th>
<th>Best FMC</th>
<th>Best of 90 nm &amp; larger proc.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit-level CDW</td>
<td>EP4SE530</td>
<td>EP4SE530</td>
<td>Am2045</td>
</tr>
<tr>
<td>16-bit Integer CDW</td>
<td>V5 SX95T</td>
<td>V5 SX95T</td>
<td>Am2045</td>
</tr>
<tr>
<td>32-bit Integer CDW</td>
<td>V5 SX95T</td>
<td>V5 SX95T</td>
<td>Am2045</td>
</tr>
<tr>
<td>SPFP CDW</td>
<td>V5 SX95T</td>
<td>V5 SX95T</td>
<td>Cell</td>
</tr>
<tr>
<td>DPFP CDW</td>
<td>EP4SE530</td>
<td>V5 SX95T</td>
<td>CSX600</td>
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</tbody>
</table>
Conclusions

- **RC Taxonomy & Reconfigurability Factors**
  - Provides framework for comparing RMC & FMC devices
  - Develops concepts and terminology to define characteristics of various computing device technologies

- **CD and CDW Metrics**
  - Basis to compare devices on computational performance & power
    - Large variations in resulting data when applied across disparate device suite
    - *FPGAs with many low-power DSPs* tended to have very high CDW scores, even for single-precision, floating-point operations
  - With increasing importance of energy, **CDW** becomes a critical metric

- **IMB Metric**
  - Basis to compare devices for on-chip memory access capabilities
  - Block-based systems tended to outperform cache-based systems

- **Architecture reformation & Moore’s law**
  - Explicit parallelism allows for full utilization of process technology & transistor count improvements
Acknowledgements

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- NSF I/UCRC Program (Center Grant EEC-0642422)
- CHREC members (31 industry & govt. partners)

- Altera Corporation (equipment, tools)
- MathStar Incorporated (equipment, tools)
- Xilinx Incorporated (equipment, tools)

Questions?
References

BACKUP
## FMC Device Features

<table>
<thead>
<tr>
<th>Device</th>
<th>Cores</th>
<th>Instructions Issued/Core</th>
<th>Datapath Width (bits)</th>
<th>Frequency (MHz)</th>
<th>Power (W)</th>
<th>On-chip Memory</th>
</tr>
</thead>
<tbody>
<tr>
<td>Am2045</td>
<td>360</td>
<td>3+1</td>
<td>32</td>
<td>350</td>
<td>15</td>
<td>45 brics ea. w/ 8 SRAM banks</td>
</tr>
<tr>
<td>CSX600</td>
<td>1+96</td>
<td>1</td>
<td>64</td>
<td>250</td>
<td>10</td>
<td>I, D caches, 96 32-bit banks SRAM</td>
</tr>
<tr>
<td>MPC7447</td>
<td>1+1</td>
<td>1+2 Int, 2+1 SPFP, 3 DPFP</td>
<td>32/128</td>
<td>1000</td>
<td>10</td>
<td>L1-I, L1-D: 4 words/access @ 2 cycles/access, L2: 8 words/access @ 9 cycles/access</td>
</tr>
<tr>
<td>Cell BE</td>
<td>1+8</td>
<td>2</td>
<td>64/128</td>
<td>3200</td>
<td>70</td>
<td>L1-I, L1-D, L2 (PPE), 8 128-bit LS banks (SPEs)</td>
</tr>
<tr>
<td>MPC8640D</td>
<td>2+2</td>
<td>, 1+2 Int, 2+1 SPFP, 3 DPFP</td>
<td>32/128</td>
<td>1000</td>
<td>14</td>
<td>Ea. core: L1-I, L1-D: 4 words/access @ 2 cycles/access, L2: 8 words/access @ 11.5 cycles/access</td>
</tr>
<tr>
<td>Atom N270</td>
<td>1+1</td>
<td>1</td>
<td>64/128</td>
<td>1600</td>
<td>3.3</td>
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## FPGA Device Features

<table>
<thead>
<tr>
<th>Device</th>
<th>LUTs</th>
<th>DSPs</th>
<th>Max. Frequency (MHz)</th>
<th>Min. Power (W)</th>
<th>Max. Power (W)</th>
<th>On-chip Memory</th>
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<tbody>
<tr>
<td>Stratix-II EP2S180</td>
<td>143,520</td>
<td>768</td>
<td>500</td>
<td>3.26</td>
<td>30</td>
<td>9 128-bit dual port blocks @ 420 MHz, 768 32-bit dual port blocks @ 550 MHz, 930 16-bit dual port blocks @ 500 MHz</td>
</tr>
<tr>
<td>Virtex-4 SX55</td>
<td>49,152</td>
<td>512</td>
<td>500</td>
<td>1</td>
<td>10</td>
<td>48 72-bit dual port blocks @ 600 MHz, 864 32-bit dual port blocks @ 580 MHz,</td>
</tr>
<tr>
<td>Virtex-4 LX200</td>
<td>178,176</td>
<td>96</td>
<td>500</td>
<td>1.27</td>
<td>23</td>
<td>48 72-bit dual port blocks @ 600 MHz, 1040 32-bit dual port blocks @ 580 MHz,</td>
</tr>
<tr>
<td>Stratix-III EP3SE260</td>
<td>203,520</td>
<td>768</td>
<td>550</td>
<td>2.11</td>
<td>25</td>
<td>320 32-bit dual port blocks @ 500 MHz</td>
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<tr>
<td>Stratix-III EP3SL340</td>
<td>270,400</td>
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<td>550</td>
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<td>Virtex-5 SX95T</td>
<td>58,800</td>
<td>640</td>
<td>550</td>
<td>1.89</td>
<td>10</td>
<td>488 72-bit dual port blocks @ 550 MHz</td>
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<td>550</td>
<td>3.43</td>
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<td>648 72-bit dual port blocks @ 550 MHz</td>
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<td>Stratix-IV EP4SE530</td>
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<td>600</td>
<td>3.55</td>
<td>39</td>
<td>64 72-bit dual port blocks @ 600 MHz, 1280 32-bit dual port blocks @ 600 MHz,</td>
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## Devices Studied

### Other RMC Device Features

<table>
<thead>
<tr>
<th>Device</th>
<th>PE</th>
<th>Frequency (MHz)</th>
<th>Min. Power (W)</th>
<th>Max. Power (W)</th>
<th>On-chip Memory</th>
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<tbody>
<tr>
<td>90 nm RMC</td>
<td>ElementCXI ECA-64</td>
<td>64 16-bit hetero. elements</td>
<td>200</td>
<td>0.05</td>
<td>4 16-bit memory units, 5 simultaneous operations</td>
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<tr>
<td></td>
<td>Mathstar Arrix FPOA</td>
<td>256 16-bit ALUs, 64 16x16 MACs</td>
<td>1000</td>
<td>18.82 @ 25%</td>
<td>80 32-bit dual port banks @ 1 GHz, 12 72-bit single port banks @ 500 MHz</td>
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<tr>
<td></td>
<td>Raytheon MONARCH</td>
<td>6 32-bit RISC processor cores, 12 256-bit Arithmetic Clusters</td>
<td>333</td>
<td>6.7</td>
<td>31 memory clusters, 4 memories/cluster, dual ported, 32 bits wide</td>
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<td></td>
<td>Tilera TILE64</td>
<td>64 32-bit 3 issue VLIW processor cores</td>
<td>750</td>
<td>5.11</td>
<td>64 32-bit L1 I, D caches, Unified L2 cache @ 7 cycle access</td>
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### FPGA Achievable Frequencies

<table>
<thead>
<tr>
<th>Device</th>
<th>Bit-Op</th>
<th>16-bit Int.</th>
<th>32-bit Int.</th>
<th>SPFP</th>
<th>DPFP</th>
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<tr>
<td>Stratix-II EP2S180</td>
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Stratix-III &-IV Bit-Op frequency limited by max DSP frequency