



# Converged Sensor Network Architecture (CSNA)

High-Performance Embedded Computing  
(HPEC) Conference – September 24, 2008

Dr. Ian Dunn, Michael Desrochers, Robert  
Cooper – Mercury Computer Systems, Inc.

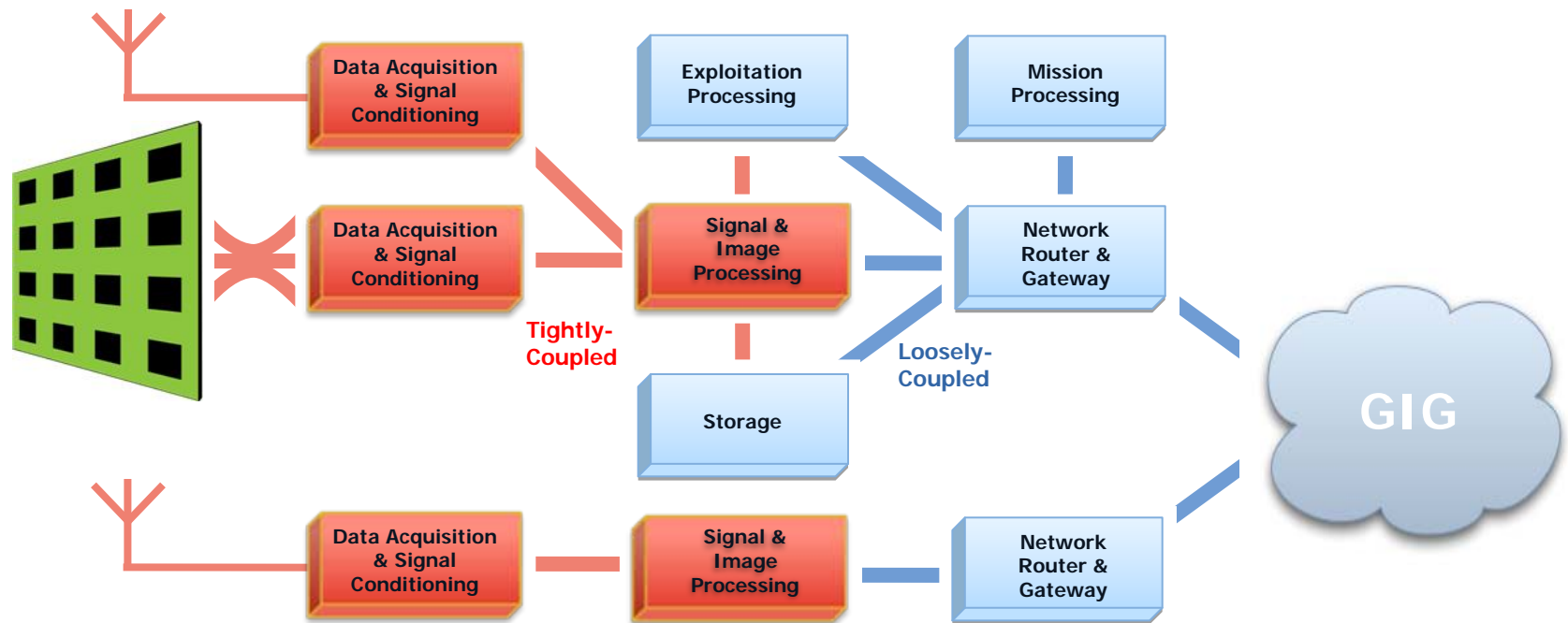
# Problem Statement

*ISR should do more "in the current conflicts while their outcomes may still be in doubt" – Sec. Gates*

<p>More Timely, More Accessible</p>	<p><b>Strategic Precision Targeting for use by a select few, to a Need for Tactical Precision Targeting for every warfighter</b></p> <ul style="list-style-type: none"><li>• Sensor data rates continue to outstrip available data link bandwidths, exacerbated by jamming</li><li>• Ground-based exploitation cells introduce too much latency for time-sensitive targeting</li><li>• Warfighters don't believe they will get appropriate sensing support when they need it</li></ul>
<p>Persistent, Accurate Surveillance</p>	<p><b>Multiple platforms are needed for persistence</b></p> <ul style="list-style-type: none"><li>• Single sensor platforms don't collect adequate target information</li><li>• Difficult targets in heavy clutter require interoperable platforms that can cooperatively find, classify and track targets (peer-to-peer)</li></ul>
<p>Size, Weight, &amp; Power Efficient</p>	<p><b>Proliferation of sensors on platforms is begetting ever more costly tradeoffs in SWaP</b></p>

# Converged Sensor Network Architecture (CSNA)

A unique approach to sensor networking that brings together signal and image processing, information exploitation, and information management into a high-performance, most productive, and cost-effective embedded compute platform



- Integrated, optimized for low latency, high throughput, and SWaP
- Designed to deliver an “embedded” Quality-of-Service that supports the convergence of processing and net-centric capabilities

# Distributed Packet Processor over RapidIO

---

- **Implemented as a layered architecture that**
  - Bridges physical layer protocols
  - Maps multiple logical layer protocols onto a bridge architecture
- **PHY: automatic termination and throttling**
- **ROUTING: programmable field lookup, routing, and prioritization**
  - Header translation and/or encapsulation
  - Traffic management
  - Software-based exception handling
- **LOGICAL: end-to-end buffer management, timeouts for robust operation**
  - Adjustable buffer watermarks per logical type (IP, ...)
  - Timeout and failover