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Implementation of a Highly Parameterized Digital PIV System On Reconfigurable Hardware

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Goal

Accelerate the performance of a highly parameterized Particle Image Velocimetry (PIV) algorithm using Field Programmable Gate Arrays

Abstract

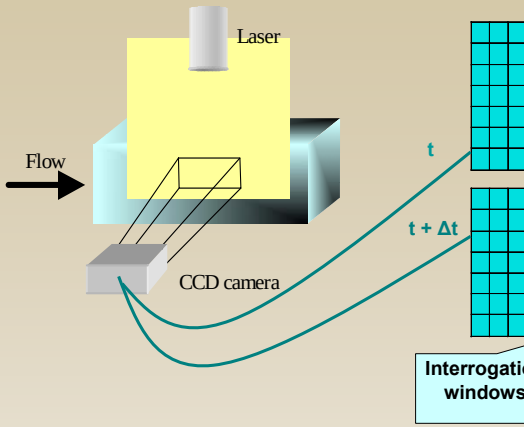
Particle image velocimetry (PIV) is used in computational fluid dynamics to obtain a detailed localized view of velocity vectors in an unsteady fluid flow. The estimated velocity field is computed from local correlations of snapshot pairs of the particle-seeded flow, obtained by high-speed cameras. Despite many improvements to PIV methods over the last twenty years, PIV post-processing remains a computationally intensive task. It becomes a serious bottleneck as snapshot acquisition rates reach O(10kHz). In this research we aim to substantially speed up PIV post-processing by implementing it in reconfigurable hardware. This implementation is highly parameterized, supporting adaptation to varying setups and application domains.

Our implementation is parameterized by the dimensions of the captured images as well as the size of interrogation windows and sub-areas. It is also parameterized by image quantization level (bits/pixel), the size of on-board memory and the overlap between interrogation windows. To the best of the authors' knowledge, this is the first highly parameterized PIV system implemented on reconfigurable hardware. For a typical PIV configuration with images of 1024×1024 pixels, 40×40 pixel interrogation windows and 32×32 pixel sub-areas, we achieved a 100-fold speedup in hardware versus a standard software implementation.

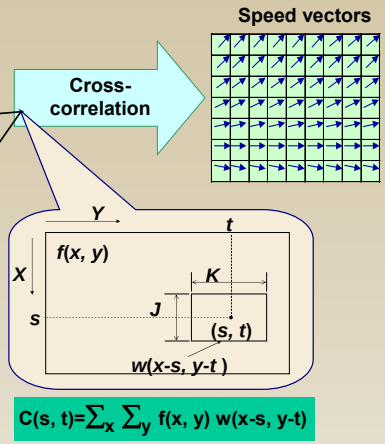
Contributions

- A highly parameterized digital PIV system:
  - Designed using VHDL
  - Implemented on an FPGA board
- A library of parameterized VHDL components for digital PIV
- A C++ implementation of parameterized PIV

Experiment



Algorithm



Examples

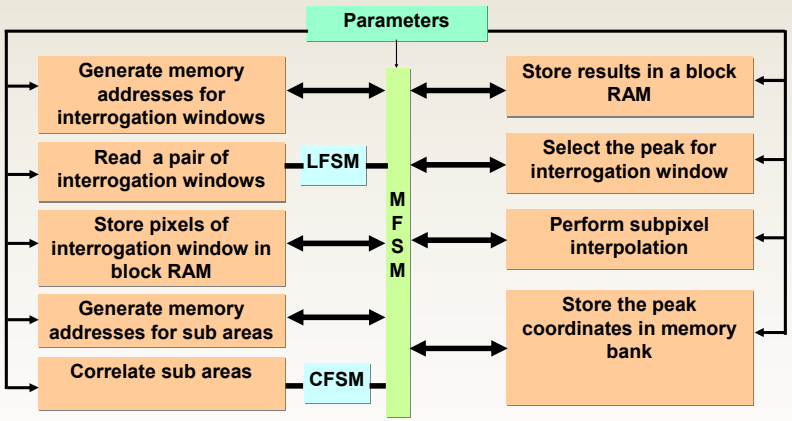
Measurement of the wake vortices of a lifting aircraft wing

http://www.innolas.com/03/p03pd_d.aspx?ID=50&MOD=pre&LANG=2

Investigation of rotor aerodynamics with respect to noise emission of various noise sources such as blade/vortex interactions

http://www.bias.com.tr/en/ur_dantecDynamics_PIV.asp

High level PIV Architecture



PIV Parameters

Parameters	Description	Circuit1	Circuit2	Circuit3
Img_width	The width in pixels of the images	1024	1200	400
Img_depth	The depth in pixels of the images	1024	1600	50
Area_width	The width in pixels of the interrogation window	40	40	50
Area_depth	The depth in pixels of the interrogation window	40	40	50
Sub_area_width	The width in pixels of the sub-areas	32	32	20
Sub_area_depth	The depth in pixels of the sub-areas	32	32	20
Displacement	Number of pixels by which a sub area is moved inside an interrogation window	1	1	1
Pixel_bits	Number of bits that represent a pixel	8	8	8
RAM_width	Number of bits in each memory address	32	32	32
Overlap	Number of interrogation windows that overlap in an interrogation window size	2	2	2

Speedup of Different Circuits

Circuits	Hardware latency	Software latency	speedup
1	0.025	3.21	128
2	0.027	3.76	139
3	0.00473	0.109	23

Future work

Use FPGA implementation in a feedback loop to control a wing standing up in a water flow.