Impact on High-Performance Applications: FPGA Chip Bandwidth at 40 nm

J. Ryan Kenny
Altera Corporation
101 Innovation Drive
San Jose, CA 95134

High-Performance Embedded Computing Workshop
23-25 September 2008
Best-in-Class Transceiver Lineage

The same analog design team improving the transceiver block through successive generations

- Stratix GX 3.125 Gbps*
- Stratix II GX 6.375 Gbps*
- Stratix IV GX 8.5 and 10 Gbps*

* All transceivers operate down to 640 Mbps

Building on a solid foundation lowers risk

Quad architecture
XAUI and GbE state machine
Pre-emphasis and equalization

Adaptive equalizer
Dynamic reconfiguration
PCI Express Gen1 and Gen2

PMA
Transmit/CDR

8.5 and 10 Gbps
PCI Express hard IP
HyperTransport support

Adaptive equalizer
Dynamic reconfiguration
PCI Express Gen1 and Gen2

Quad architecture
XAUI and GbE state machine
Pre-emphasis and equalization

PMA
Transmit/CDR

© 2008 Altera Corporation—Public
Altera, Stratix, Arria, Cyclone, MAX, HardCopy, Nios, Quartus, and MegaCore are trademarks of Altera Corporation
# 40-nm Transceiver Eye and Jitter Test Set Up

<table>
<thead>
<tr>
<th>Item</th>
<th>Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transceiver</td>
<td>$V_{OD} = 0.6 , \text{V}$</td>
</tr>
<tr>
<td>Conditions</td>
<td>Nominal voltages: $V_{CCHX} = 3.0 , \text{V}$, $V_{CCHTX} = 1.4 , \text{V}$, $V_{CCLX} = 1.1 , \text{V}$</td>
</tr>
<tr>
<td></td>
<td>Temperature: $25°C$</td>
</tr>
<tr>
<td>Data rates/pattern</td>
<td>6.375 Gbps, 8.5 Gbps, and 10 Gbps/on chip PRBS7</td>
</tr>
</tbody>
</table>

![Diagram of test setup](image-url)
40-nm Transceiver Eye Diagram at 8.5 and 10 Gbps

**Extraordinary Jitter Performance**

- **8.5 Gbps**
  - Pattern: PRBS 7
  - \( V_{OD} \): 600 mV
  - DJ: 10.3 ps
  - RJ (RMS): 1.23 ps

- **10 Gbps**
  - Pattern: PRBS 7
  - \( V_{OD} \): 600 mV
  - DJ: 10.3 ps
  - RJ (RMS): 1.35 ps

© 2008 Altera Corporation—Public
Altera, Stratix, Arria, Cyclone, MAX, HardCopy, Nios, Quartus, and MegaCore are trademarks of Altera Corporation.
Jitter Tolerance at 8.5 Gbps

Jitter tolerance, 8.5 Gbps, PRBS31

8.5-Gbps jitter tolerance curve

CEI 6G short-reach jitter mask

Jitter frequency (Hz)

Jitter amplitude (UI)

© 2008 Altera Corporation—Public
Altera, Stratix, Arria, Cyclone, MAX, HardCopy, Nios, Quartus, and MegaCore are trademarks of Altera Corporation
High-Performance Applications

**Chip-to-chip bandwidth**
- In excess of 100 Gbps
- (Mixture of 8.5 Gbps and 3.125 Gbps)

**Chip-to-backplane**
- As many as 48 lanes
- 24 up to 8.5 Gbps

**Soon: Drive optical**
- 10G optical
- (Future)