Impact on High-Performance Applications: FPGA Chip Bandwidth at 40 nm

J. Ryan Kenny
Altera Corporation
101 Innovation Drive
San Jose, CA 95134

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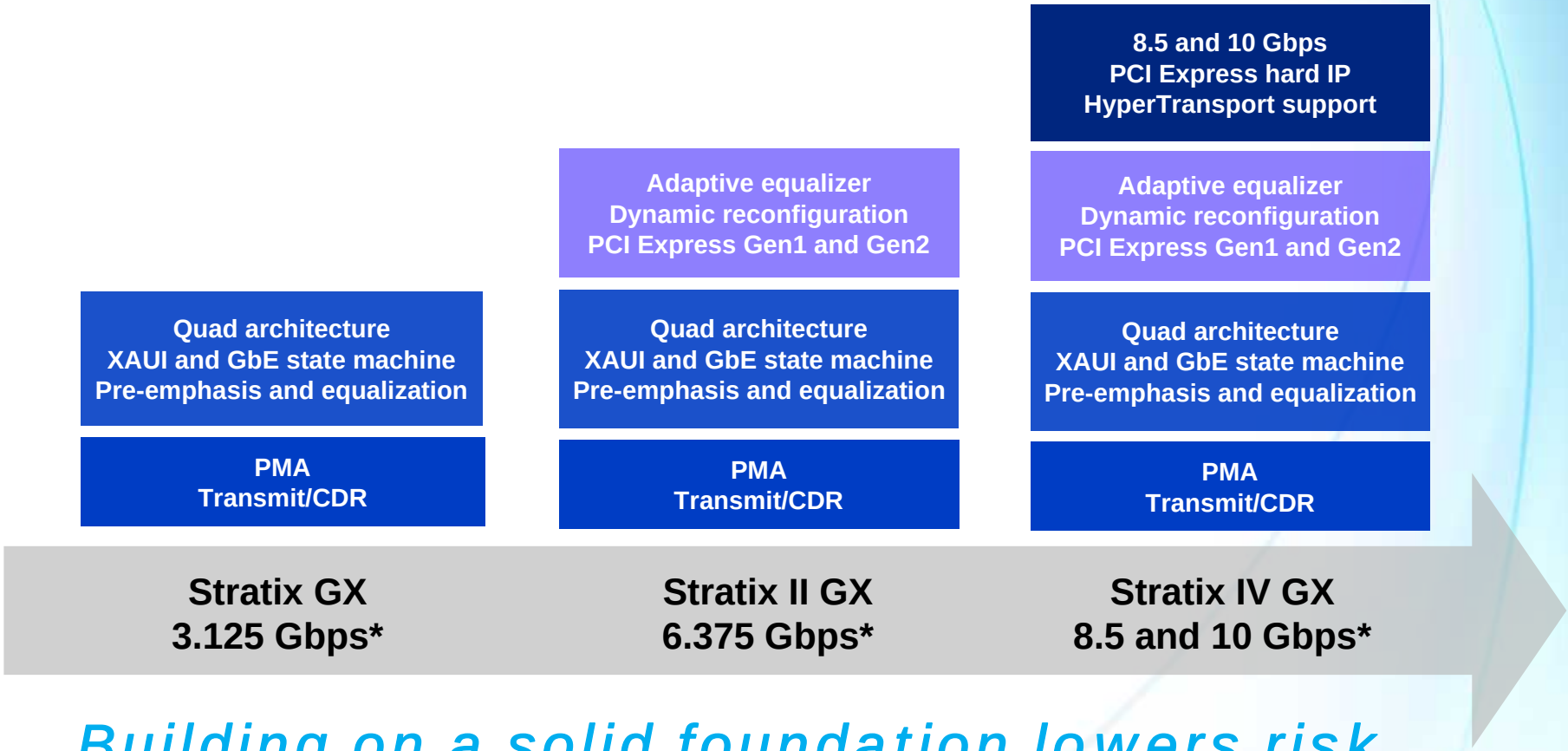
Best-in-Class Transceiver Lineage

The same analog design team improving the transceiver block through successive generations

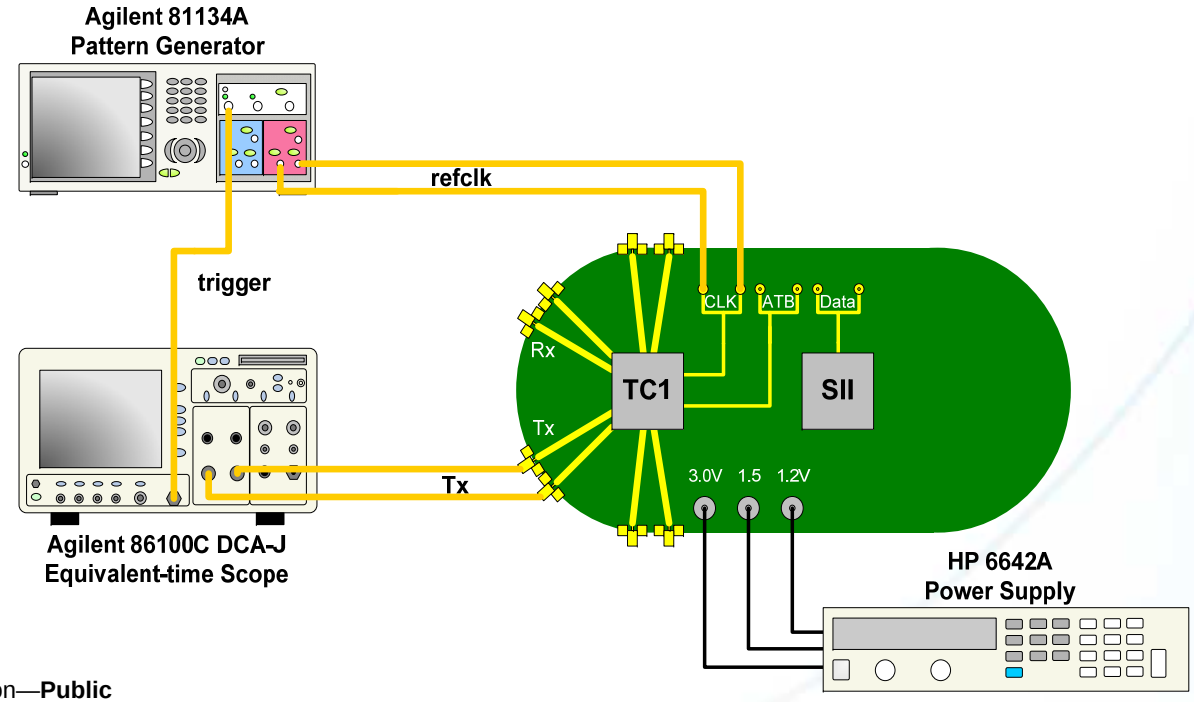


Building on a solid foundation lowers risk

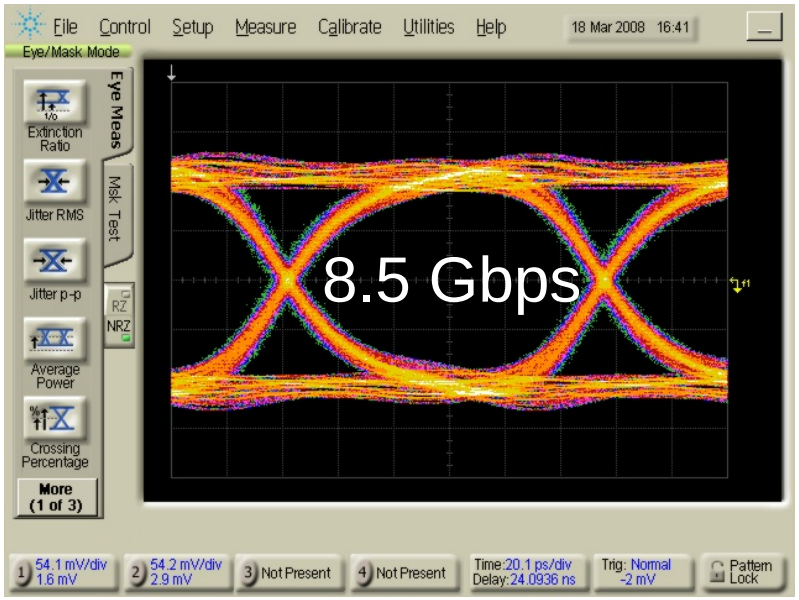
*** All transceivers operate down to 640 Mbps**

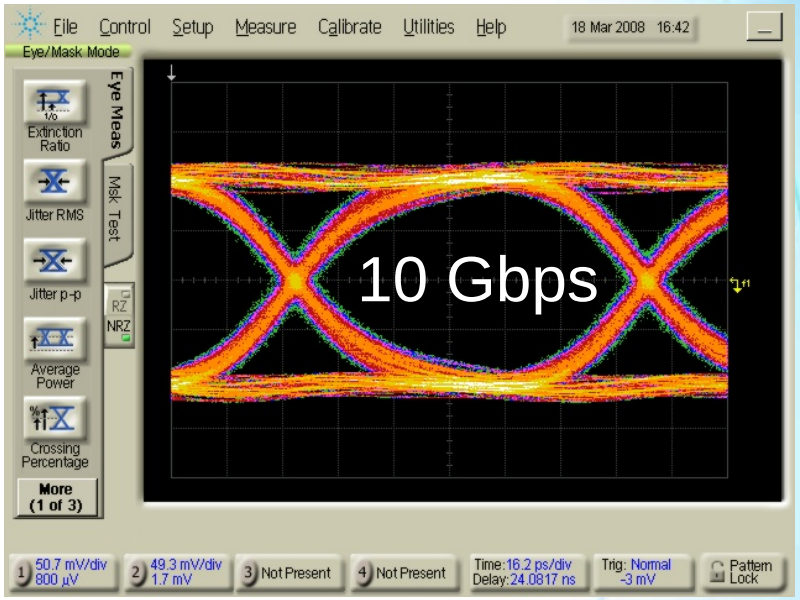
40-nm Transceiver Eye and Jitter Test Set Up

Item	Parameters
Transceiver	V_{OD} = 0.6 V
Conditions	Nominal voltages: V_{CCHX} = 3.0 V, V_{CCHTX} = 1.4 V V_{CCLX} = 1.1 V Temperature: 25°C
Data rates/pattern	6.375 Gbps, 8.5 Gbps, and 10 Gbps/on chip PRBS7



40-nm Transceiver Eye Diagram at 8.5 and 10 Gbps

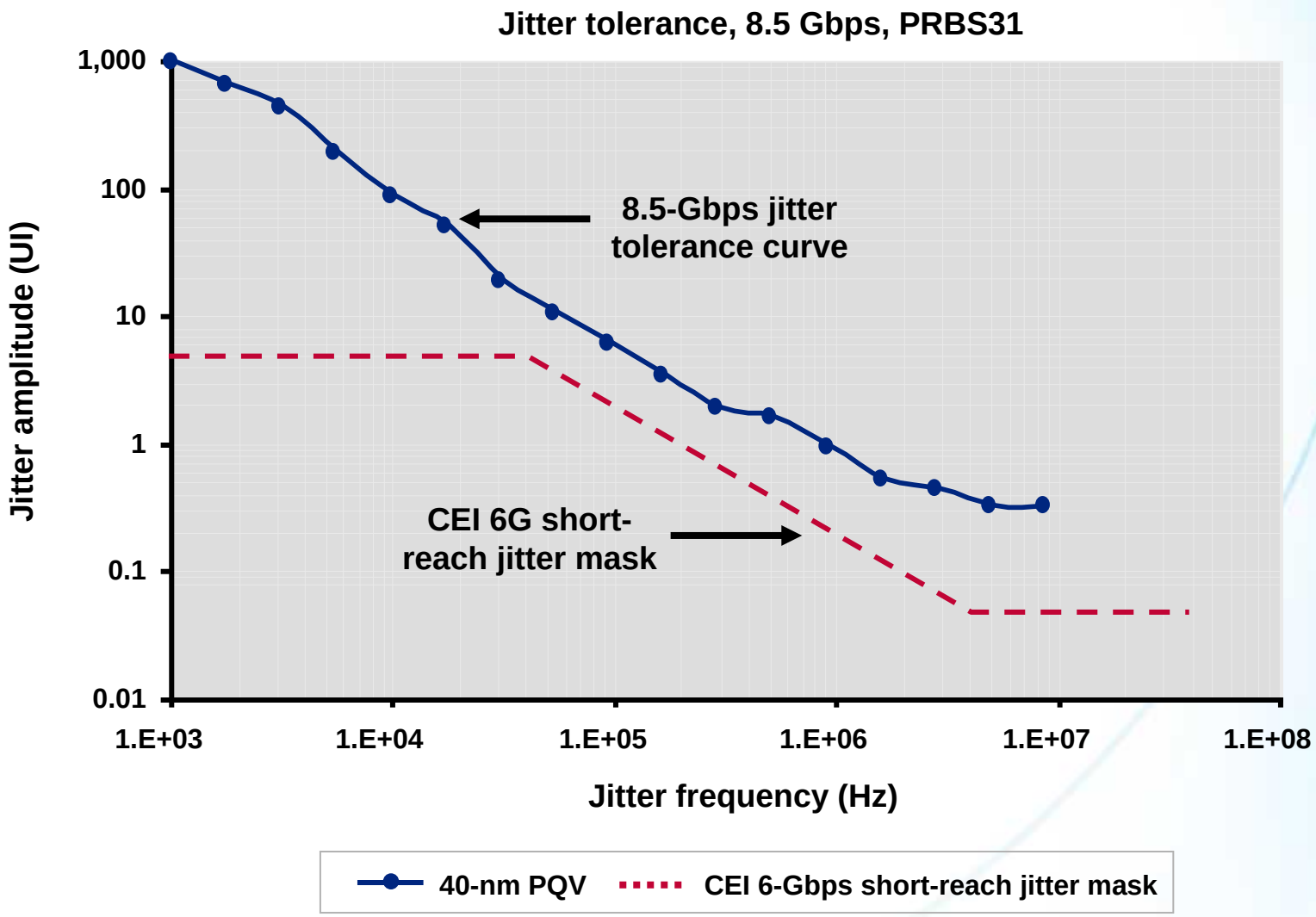




Pattern	V_{OD}	DJ	8.5 Gbps RJ (RMS)	10 Gbps RJ (RMS)
PRBS 7	600 mV	10.3 ps	1.23 ps	1.35 ps

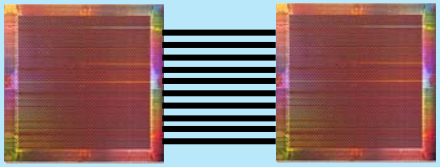
Extraordinary jitter performance

Jitter Tolerance at 8.5 Gbps



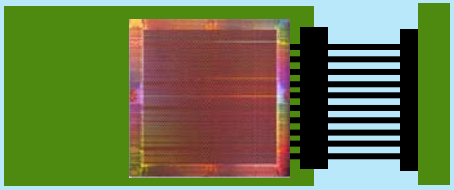
High-Performance Applications

Chip-to-chip bandwidth



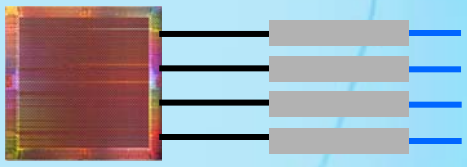
- In excess of 100 Gbps
- (Mixture of 8.5 Gbps and 3.125 Gbps)

Chip-to-backplane



- As many as 48 lanes
- 24 up to 8.5 Gbps

Soon: Drive optical



- 10G optical
- (Future)