SmartCell: Architecture, Design and Performance Analysis

for Reconfigurable Embedded Computing

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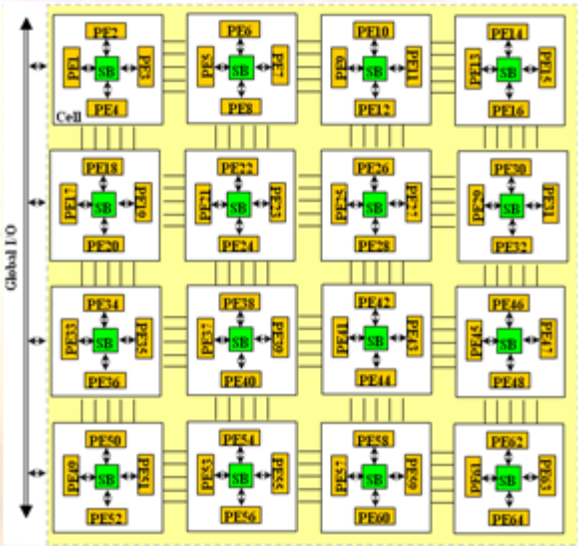
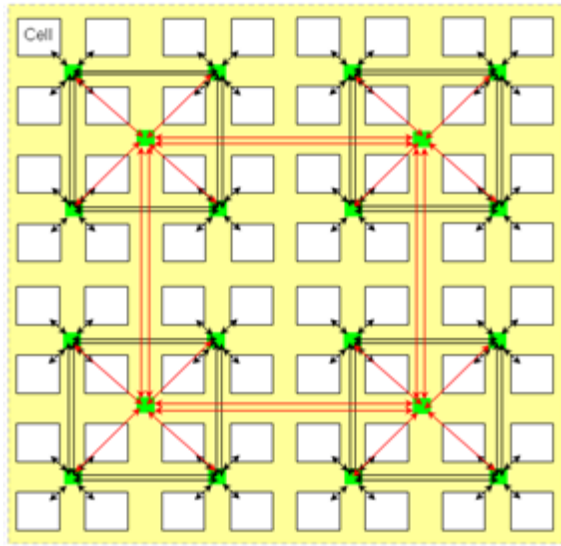
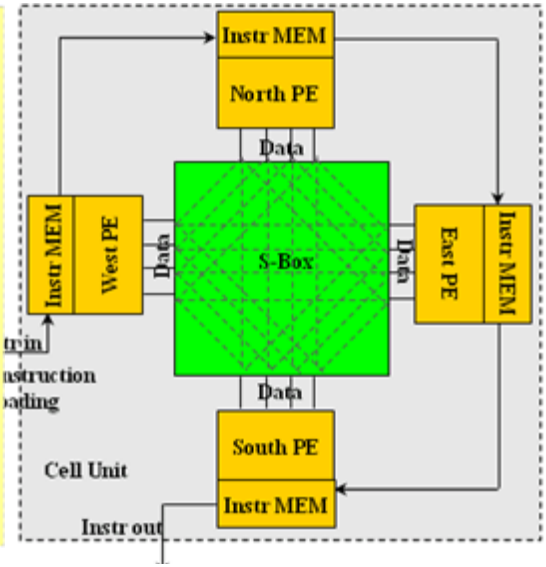
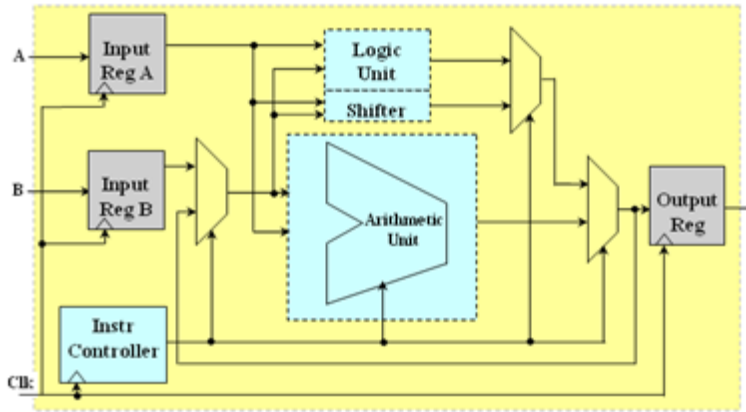
SmartCell: Tiled Architecture, Processor Design and Interconnect



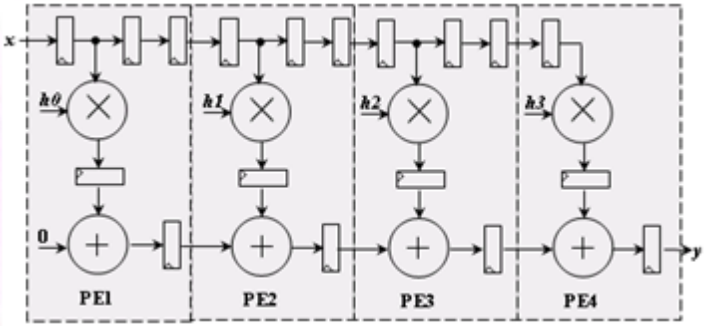




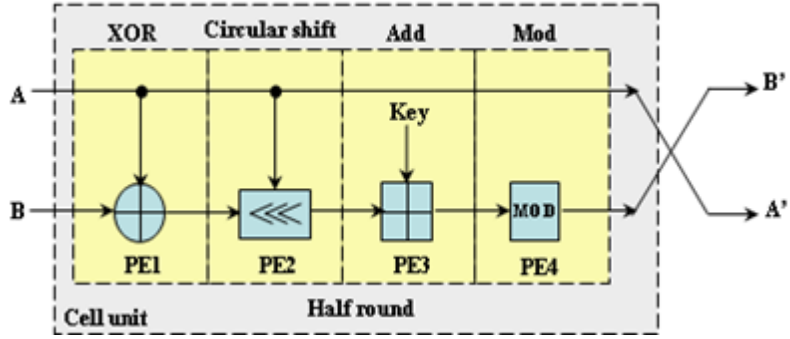
- Many cells are titled in 2D layout
- Each cell has 4 PEs (N,W,S,E)
- Simplified processor with mem
- A crossbar within the cell; on-chip interconnect uses CMesh



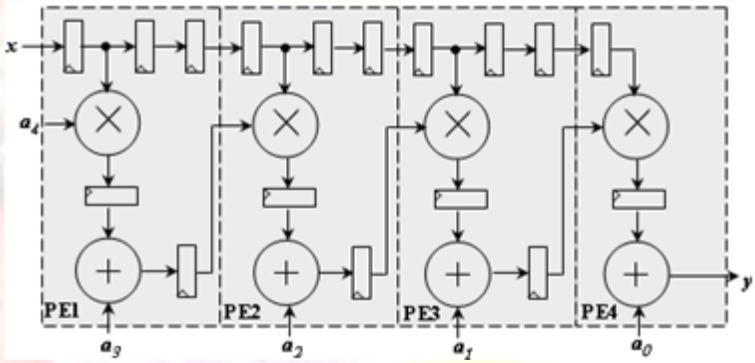
Features and Application Domain



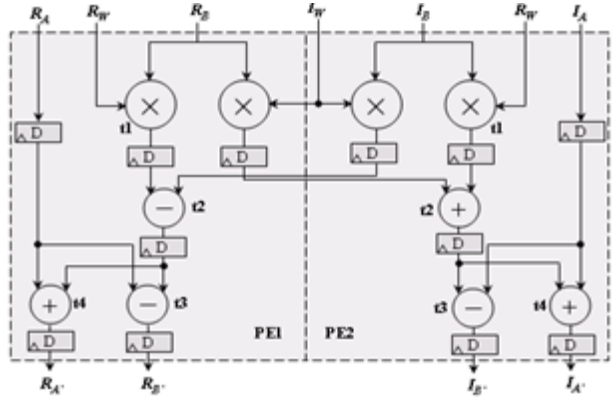
FIR filter



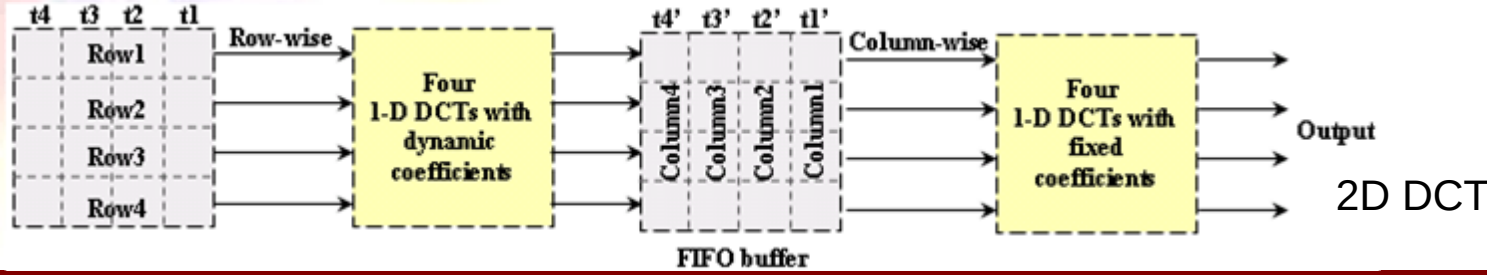
RC5 data encryption



Polynomial Evaluation



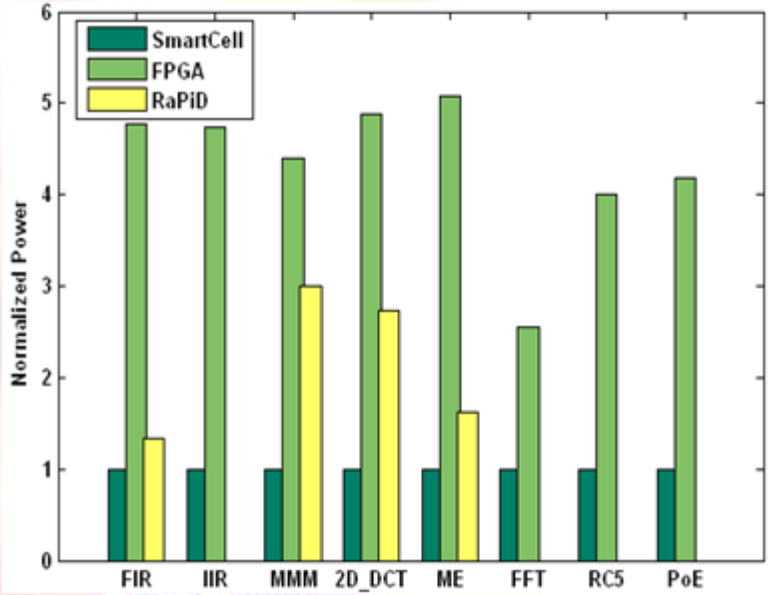
FFT Butterfly

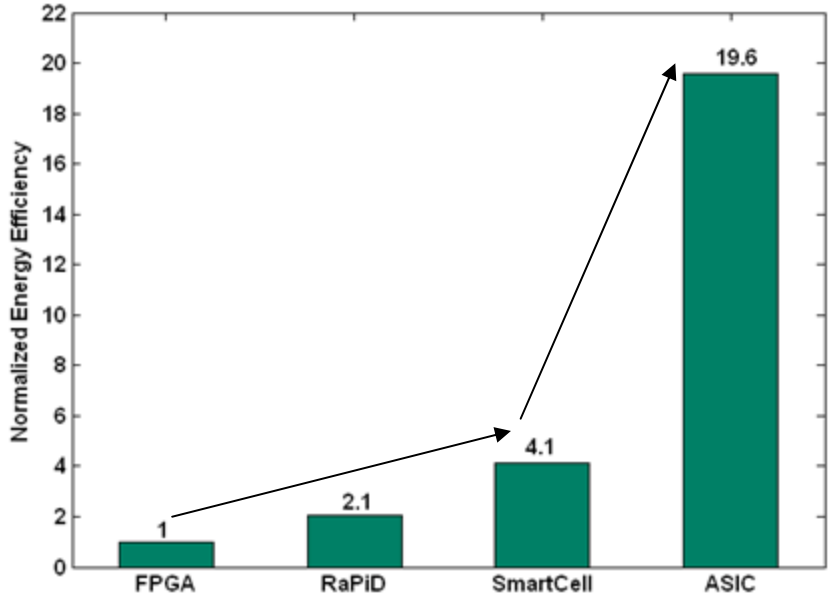


2D DCT

System Design and Performance

- Prototype chip design: 4x4 cells (64 PEs), .13 TSMC, 8.2mm^2, 1V, about 156mW @100MHz
- Benchmark with RaPiD, Stratix-II (90nm), and ASIC





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