Impact on High Performance Applications: FPGA Chip Bandwidth at 40nm

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Overview

With the arrival of 40nm FPGA devices, designers of high performance computing applications will want a high level evaluation of this technology for their applications.

The primary value propositions for the new higher density devices are:

1. Very high on-chip\off-chip bandwidth
2. Lower power per logic element
3. Much higher logic density for parallelizing operations
4. Larger memory for acceleration of matrix operations

Of these value propositions, the highest value for high performance computing applications relates to the volume of digital information that can be brought onto the chip and processed per operating cycle. An analysis of this capability is offered.

Device Overview

With the release of Quartus II 8.0 software, the characteristics of 40nm FPGA devices (Stratix IV GX FPGAs) were revealed. The family includes devices with logic counts of 110K, 230K, 310K, 370K, 530K logic elements, and a device with up to 680K logic elements without high speed transceivers.

Availability of these devices begins in late 2008 through mid-2009, depending on the device size and demand. Release priority is on transceiver devices.

New capabilities with the Stratix IV GX FPGA include a hard PCI Express IP core, mixed speed transceiver blocks with transceivers running at 8.5 Gbps and 3.2 Gbps, improved performance memory interfaces, and the ability to transition designs to a HardCopy structured ASIC with transceivers. Programmable power technology carries over from the Stratix III device family.

Transceiver Technology

The transceiver technology for 40nm devices was designed and tested for 65nm Stratix III devices, but not productized. This was to enable immediate shrinkage to 40nm, and accelerate the availability of high transceiver count devices for the Stratix IV family.

The transceiver technology being offered for the initial release of Stratix IV GX is 8.5 Gbps. This is accompanied by all of the previous transceiver advancements offered to date on Stratix class devices.

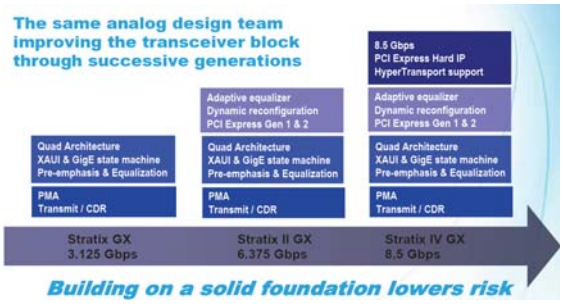

Figure 1: Altera High Speed Transceiver Technology

Test Chip Data and Results

Test chips have shown lab results for the 40nm transceiver at speeds of 8.5 Gbps, 9 Gbps, 10 Gbps, and beyond. The eye diagrams for the first two test cases are shown below.

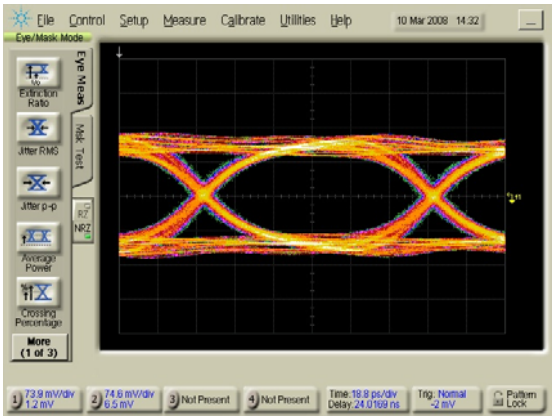

Figure 2: 40nm Transceiver Test Chip – 8.5 Gbps

These diagrams were captured from test equipment using an 800mV signal (V_{OD}) with 2 mA of pre-emphasis to account for long test-board traces.

Nine separate runs of test chips were executed at 40nm. This robust risk management strategy resulted in the ability to package more transceivers together on a single block, as well as optimal horizontal and vertical placement of transceivers to maximize user bandwidth.

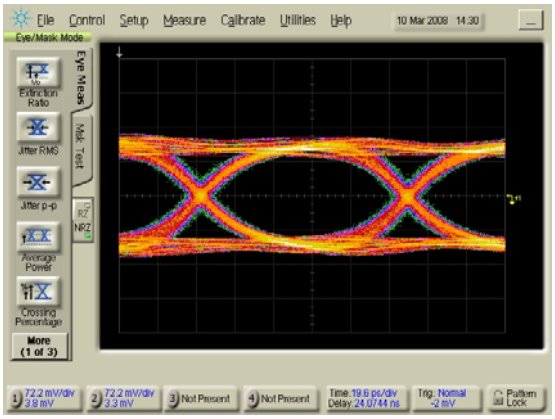

Figure 3: 40nm Transceiver Test Chip – 9 Gbps

Bandwidth Capability

For computational acceleration, the driving device feature for parallel computing is the inbound data rate ('ingest rate'). This device capability drives both how single FPGA devices can be integrated into a large HPC system, as well as the data-sharing capabilities of a multi-chip computation grid.

The largest device in the new 40nm families is the 4SGX530. This device has a total of 48 high speed transceivers; 32 operate at up to 8.5 Gbps, and another 16 operate at up to 3.2 Gbps. The transceivers are packages into blocks of (2) 8.5 Gbps and (1) 3.2 Gbps transceiver per block, with the blocks distributed among the left and right of the device (see ***Figure 4***).

The total full duplex bandwidth of this device is expected to be up to 320 Gbps. This can be compared to other families of available FPGA devices in ***Figure 4***.

Roadmap to 10 Gbps Transceivers

A future mid-term release of the Stratix IV GX FPGA will include full support of 10 Gbps transceivers.

Where test chips have shown the capability to reach 10Gbps speeds and beyond with sufficient pre-emphasis and sustained junction temperature conditions, Altera plans to continue developing this capability so that it is fully supportable for all customers across a relevant operating temperature range.

The value of 10 Gbps transceivers in directly driving optical transceivers is of high value in connecting computing devices to communications channels and increasing the ability to offload heavy computation tasks from existing operational systems.

Other HPEC Value Propositions

In addition to high bandwidth for accelerated computing, other features of the new 40nm devices will be relevant to these applications.

Further increases the on-chip\off-chip bandwidth of FPGAs in HPC applications include high speed memory interface support for DDR3 up to 1067 Mbps. This includes on-chip termination for power savings, and PVT auto-calibration for design simplicity.

Increases in density come with increases in digital signal processing capability. Processing speed ranges up to 550 MHz, with over 1000 18x18 multipliers on several FPGA devices.

Summary

Designers and users of high performance computing applications have been able to rely on a steady increase in computing density and speed that is on par or better than general purpose processing.

Of even more importance and utility to these applications, however, is a significant increase in reliable high speed transceiver technology. This has the capability to advance the role of FPGAs in HPC applications.

This presentation will elaborate on the final capabilities of 40nm devices, and application specific capabilities.

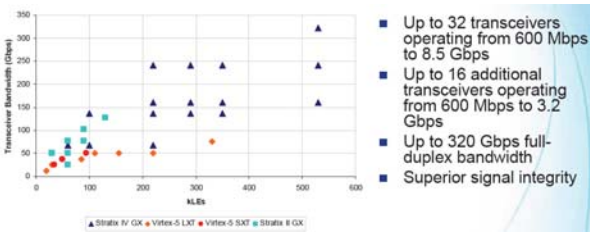

Figure 4:Transceiver Bandwidth of new 40nm FPGAs

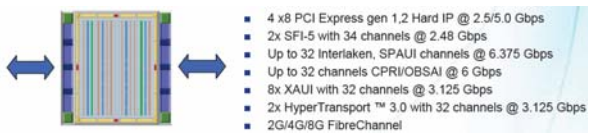

Figure 5: Channel Capabilities of new 40nm FPGA