DEFINING THE FUTURE

Designing Processing Architectures for Space Applications

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Space Applications Present Conflicting Design Challenges

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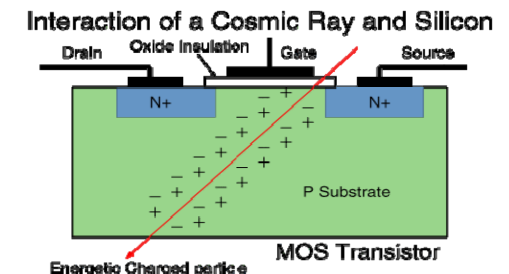
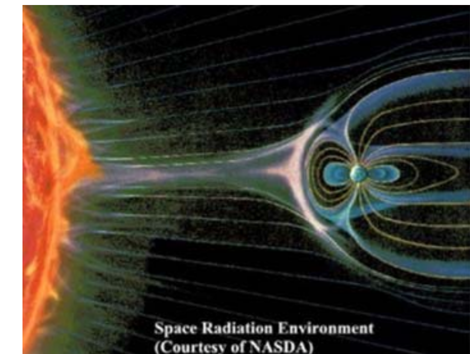
- Challenging Form Factor Requirements Constrain the Processing Design
  - Environmental
  - Thermal
  - Packaging
  - Material restrictions
  - Size, weight, and power (SWAP)



- Processing Requirements Drive Technology Selection
  - Memories
  - CPUs
  - Field programmable gate arrays (FPGA)
  - Application specific integrated circuits (ASIC)
  - High I/O packaging



Radiation Variation with Orbit due to the Earth's Magnetic Field

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Form Factor Requirements for Space

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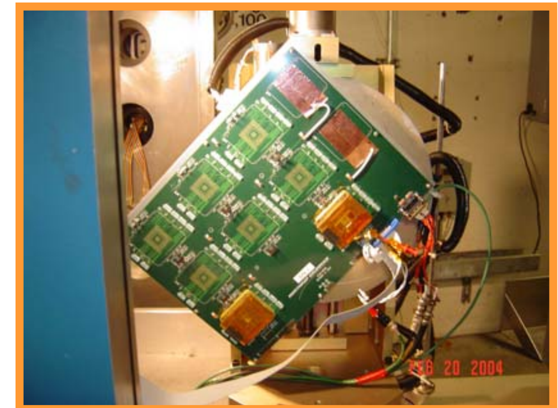
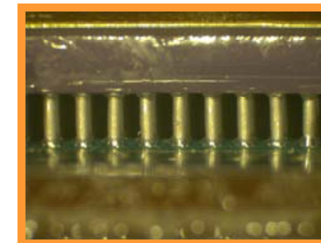
- Environment and Radiation
  - Total dose radiation and single event effects (SEE)
  - Launch vibration, vacuum & outgassing, material selection
- Thermal Management – Cooling and Heating
  - Adequate cooling path for hot components
  - Minimize cold excursions
  - Limited to conduction cooling and heat radiation
- Packaging
  - Thermal cycling limited by CTE mismatches between components and boards
  - Shielding must be considered at component, assembly, and subsystem levels
  - Good system grounding is essential
- Size, Weight, and Power (SWAP)
  - Power is critical and impacts size and weight
  - Launch weight is expensive

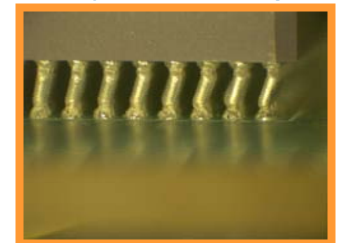


Component Radiation Testing

Ceramic Column Grid Array CTE Testing



Assembled to PCB



After 1500 Thermal Cycles

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Processing Requirements Demand Advanced Technology

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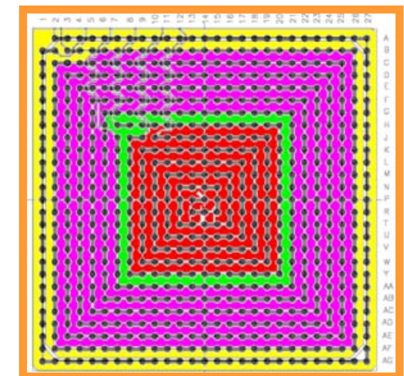
- Memories
  - Radiation hardened SRAM and EEPROM are available
  - Commercial DRAM and Flash NVM are denser and faster but require SEE mitigation
- FPGAs
  - Anti-fuse FPGAs are radiation hardened
  - Flash-based and RAM-based FPGAs require multiple SEE mitigation techniques
- ASICs
  - Radiation-hardened fabrication processes available
  - Non-rad-hard processes are more numerous, less expensive, and have more advanced feature sizes
- High I/O Packaging
  - Ball Grid Array (BGA) and thin-shrink small outline (TSSOP) packages are susceptible to thermal cycle damage

High Speed ASIC Device



BGA Daisy-chain Package for CTE Testing

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In the Poster Session

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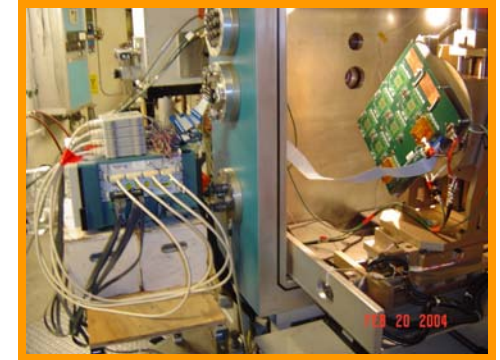
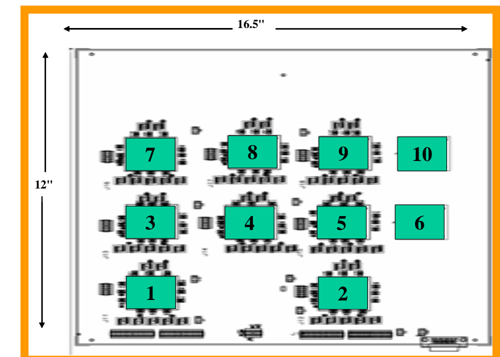
- Radiation -- Total Dose, Single Event Effects
  - Requirements, assessment, testing
- Thermal Considerations and Packaging Options
- Use of Memories in Space Applications
  - Error detection and correction (EDAC) and power control
- FPGAs
  - Anti-fuse, flash-based, and RAM-based
  - Triple module redundancy (TMR), memory checking, and memory scrubbing
- ASICs
  - Radiation hardened fabrication or upscreening & testing
- High IO Packaging – Thermal Cycle Testing





With risk assessment and risk mitigation, advanced processing technologies can be available for open system architectures.

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