

Linear Algebraic Graph Algorithms for Back End Processing

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Outline

• Introduction

- Power Law Graphs
- Graph Benchmark
- Results
- Summary

- Post Detection Processing
- Sparse Matrix Duality
- Approach



Statistical Network Detection

Problem: Forensic Back-Tracking

- Currently, significant analyst effort dedicated to manually identifying links between threat events and their immediate precursor sites
 - Days of manual effort to fully explore candidate tracks
 - Correlations missed unless recurring sites are recognized by analysts
 - Precursor sites may be low-value staging areas
 - Manual analysis will not support further backtracking from staging areas to potentially higher-value sites

Concept: Statistical Network Detection

- Develop graph algorithms to identify adversary nodes by estimating connectivity to known events
 - Tracks describe graph between known sites or events which act as sources
 - Unknown sites are detected by the aggregation of threat propagated over many potential connections



Planned system capability (over major urban area)

Event A

1st Neighbor

2nd Neighbor

3rd Neighbor

Even

- 1M Tracks/day (100,000 at any time)
- 100M Tracks in 100 day database
- 1M nodes (starting/ending points)
- 100 events/day (10,000 events in database)

- Computationally demanding graph processing
 - -~ 10⁶ seconds based on benchmarks & scale
 - $\sim 10^3$ seconds needed for effective CONOPS (1000x improvement)



Graphs as Matrices



- Graphs can be represented as a sparse matrices
 - Multiply by adjacency matrix \rightarrow step to neighbor vertices
 - Work-efficient implementation from sparse data structures
- Most algorithms reduce to products on semi-rings: C = A "+"."x" B
 - "x" : associative, distributes over "+"
 - □"+" : associative, commutative
 - Examples: +.* min.+ or.and



Distributed Array Mapping

Adjacency Matrix Types:



Distributions:





Algorithm Comparison

Algorithm (Problem)	Canonical Complexity	Array-Based Complexity	Critical Path (for array)
Bellman-Ford (SSSP)	<i>©</i> (mn)	<i>©</i> (mn)	<i>Θ</i> (<i>n</i>)
Generalized B-F (APSP)	NA	$\Theta(n^3 \log n)$	<i>Θ</i> (log <i>n</i>)
Floyd-Warshall (APSP)	<i>©</i> (<i>n</i> ³)	<i>©</i> (<i>n</i> ³)	<i>Θ</i> (<i>n</i>)
Prim (MST)	<i>©</i> (<i>m</i> + <i>n</i> log <i>n</i>)	<i>Θ</i> (<i>n</i> ²)	<i>Θ</i> (<i>n</i>)
Borůvka (MST)	$\Theta(m \log n)$	<i>Θ</i> (<i>m</i> log <i>n</i>)	<i>Θ</i> (log ² <i>n</i>)
Edmonds-Karp (Max Flow)	<i>Θ</i> (<i>m</i> ² <i>n</i>)	<i>Θ</i> (<i>m</i> ² <i>n</i>)	<i>©</i> (mn)
Push-Relabel (Max Flow)	⊖(mn²)	<i>O</i> (<i>mn</i> ²)	?
	(or <i>©</i> (<i>n</i> ³))		
Greedy MIS (MIS)	<i>©</i> (<i>m</i> + <i>n</i> log <i>n</i>)	$\Theta(mn+n^2)$	$\Theta(n)$
Luby (MIS)	<i>©</i> (<i>m</i> + <i>n</i> log <i>n</i>)	$\Theta(m \log n)$	$\Theta(\log n)$

Majority of selected algorithms can be represented with array-based constructs with equivalent complexity.

(n = |V| and m = |E|.)



A few DoD Applications using Graphs

DATA FUSION

FORENSIC BACKTRACKING



 Identify key staging and logistic sites areas from persistent surveillance of vehicle tracks



 Bayes nets for fusing imagery and ladar for better on board tracking

TOPOLOGICAL DATA ANALYSIS

 Higher dimension graph analysis to determine sensor net coverage [Jadbabaie]



Application	Key Algorithm	Key Semiring Operation
 Subspace reduction Identifying staging areas Feature aided 2D/3D fusion Finding cycles on complexes 	 Minimal Spanning Trees Betweenness Centrality Bayesian belief propagation Single source shortest path 	X +.* A +.* X ^T A +.* B A +.* B (A, B tensors) D min.+ A (A tensor)
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Approach: Graph Theory Benchmark

- Scalable benchmark specified by graph community
- Goal
 - Stress parallel computer architecture
- Key data
 - Very large Kronecker graph
- Key algorithm
 - Betweenness Centrality

😑 😑 GraphAnalysis.d	org: High Performance Computing for solving large-scale graph problems			
	HPC Graph Analysis			
Home	Benchmark			
News Benchmark	Overview			
Results Publications	We present a graph theory benchmark representative of computational kernels in computational biology, complex network analysis, and national			
People	security. This benchmark is based on the HPCS Scalable Synthetic Compact Applications graph analysis (SSCA#2) benchmark. SSCA#2 is characterized			
Links Contact	by integer operations, a large memory footprint, and irregular memory access patterns. It has multiple kernels accessing a single data structure representing a weighted, directed multigraph. In addition to a kernel to			
	construct the graph from the input tuple list, there are three additional computational kernels to operate on the graph. Each of the kernels requires irregular access to the graph's data structure, and it is possible that no single data layout will be optimal for all four computational kernels.			
	References			
	 SSCA#2 v2.0 Specification: pdf doc Sequential code: C 			
	 Parallel code: C/OpenMP 			

- Computes number of shortest paths each vertex is on
 - Measure of vertex "importance"
 - Poor efficiency on conventional computers





• Introduction



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Power Law Graphs



- Many graph algorithms must operate on power law graphs
- Most nodes have a few edges
- A few nodes have many edges



Modeling of Power Law Graphs



- Real world data (internet, social networks, …) has connections on all scales (i.e power law)
- Can be modeled with Kronecker Graphs: G^{⊗k} = G^{⊗k-1} ⊗ G
 - Where "⊗"denotes the Kronecker product of two matrices



Kronecker Product

- Let B be a N_BxN_B matrix
- Let C be a N_cxN_c matrix
- Then the Kronecker product of B and C will produce a $N_B N_C x N_B N_C$ matrix A:

$$A = B \otimes C = \begin{pmatrix} b_{1,1}C & b_{1,2}C & \dots & b_{1,M_B}C \\ b_{2,1}C & b_{2,2}C & \dots & b_{2,M_B}C \\ \vdots & \vdots & & \vdots \\ b_{N_B,1}C & b_{N_B,2}C & \dots & b_{N_B,M_B}C \end{pmatrix}$$

Kronecker Graph (Leskovec 2005 & Chakrabati 2004)

- Let G be a NxN adjacency matrix
- Kronecker exponent to the power k is:

$$G^{\otimes k} = G^{\otimes k-1} \otimes G$$



Kronecker Product of a Bipartite Graph



- Fundamental result [Weischel 1962] is that the Kronecker product of two complete bipartite graphs is two complete bipartite graphs
- More generally

 $B(n_1, m_1) \otimes B(n_2, m_2) \stackrel{P}{=} B(n_1 n_2, m_1 m_2) \cup B(n_2 m_1, n_1 m_2)$



• Kronecker exponent of a bipartite graph produces many independent bipartite graphs

$$B(n,m)^{\otimes k} \stackrel{P}{=} \bigcup_{r=0}^{k-1} \bigcup_{r=0}^{\binom{k-1}{r}} B(n^{k-r}m^r, n^rm^{k-r})$$

Only k+1 different kinds of nodes in this graph, with degree distribution

$$Count[Deg = n^r m^{k-r}] = \binom{k}{r} n^{k-r} m^r$$



Explicit Degree Distribution

- Kronecker exponent of bipartite graph naturally produces exponential distribution
- Provides a natural framework for modeling "background" and "foreground" graph signatures
- Detection theory for graphs?





Reference

- Book: "Graph Algorithms in the Language of Linear Algebra"
- Editors: Kepner (MIT-LL) and Gilbert (UCSB)
- Contributors
 - Bader (Ga Tech)
 - Chakrabart (CMU)
 - Dunlavy (Sandia)
 - Faloutsos (CMU)
 - Fineman (MIT-LL & MIT)
 - Gilbert (UCSB)
 - Kahn (MIT-LL & Brown)
 - Kegelmeyer (Sandia)
 - Kepner (MIT-LL)
 - Kleinberg (Cornell)
 - Kolda (Sandia)
 - Leskovec (CMU)
 - Madduri (Ga Tech)
 - Robinson (MIT-LL & NEU), Shah (UCSB)

Fundamentals of Algorithms

Graph Algorithms in the Language of Linear Algebra

Jeremy Kepner and John Gilbert (editors)

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Graph Processing Kernel -Vertex Betweenness Centrality-

Betweenness centrality is a measure for estimating importance of a vertex in a graph

Algorithm Description

- 1. Starting at vertex v
- · compute shortest paths to all other vertices
- for each reachable vertex, for each path it appears on, assign a token
- 2. Repeat for all vertices
- 3. Accumulate across all vertices

Vertices that appear on most shortest paths have the highest betweenness centrality measure

- Rules for adding tokens (betweenness value) to vertices
- Tokens are not added to start or end of the path
- Tokens are normalized by the number of shortest paths between any two vertices



Graph traversal starting at vertex 1

- 1. Paths of length 1
- Reachable vertices: 2, 4

2. Paths of length 2

- Reachable vertices: 3, 5, 7
 - Add 2 tokens to: 2 (5, 7)
 - Add 1 token to: 4 (3)

3. Paths of length 3

- Reachable vertex: 6 (two paths)
 - Add .5 token to: 2, 5
 - Add .5 token to: 4, 3



Array Notation

Booleans:

 \mathbf{A} : $\mathbb{R}^{N \times N}$

- Data types
 - Reals: \mathbb{R} Integers: \mathbb{N}
 - Postitive Integers: \mathbb{N}_+
- Vectors (bold lowercase): $\mathbf{a}: \mathbb{R}^N$
- Matrices (bold uppercase):
- Tensors (script bold uppercase): \mathbf{A} : \mathbb{R}^{VXNXN}
- Standard matrix multiplication

 $\mathbf{A} \mathbf{B} = \mathbf{A} + \mathbf{B}$

- Sparse matrix: $\mathbf{A}~: \mathbb{R}^{S(N) \textbf{x} N}$
- Parallel matrix: \mathbf{A} : $\mathbb{R}^{P(N) \times N}$



Matrix Algorithm

	$\mathbf{c}:\mathbb{I}$	$\mathbb{R}^N_+ = \mathrm{Betweenne}$	ESSCENTRAL	ITY $(\mathbf{A}:\mathbb{B}^{S})$	$^{(N \times N)})$
Declare Data	$\int 1$	$\mathbf{\mathfrak{T}}: \mathbb{B}^{S(d_{max}) imes \mathbf{v} imes}$	S(N) Q :	$\mathbb{N}_{+}^{ \mathbf{v} imes N}$	$\tilde{\mathbf{Q}}: \mathbb{N}_{+}^{ \mathbf{v} \times S(N)}$
Structures	2	$\mathbf{W}: \mathbb{R}_+^{ \mathbf{v} imes S(N)}$	$ ilde{\mathbf{C}}: \mathbb{R}_+^{ \mathbf{v} imes N}$	$\mathbf{c},:\mathbb{R}^N_+$	·
Loop over	$\int 3$	for $\mathbf{v} \in V$		·	
vertices	٦4	do			
	5	d:=1	$\mathbf{\mathfrak{T}}:=0$	$\tilde{\mathbf{C}} := 0$	
	6	$\mathbf{T}_d := \mathbf{C}$	$\mathbf{Q}:= ilde{\mathbf{Q}}:=\mathbf{I}(\mathbf{v})$	(r,:)	Sparse
Shortost	(7	while T	$\Gamma_d \neq 0$	1	Matrix-Matrix
	8	do			Multiply
patns	9		$\tilde{\mathbf{Q}} := (\tilde{\mathbf{Q}} \ \mathbf{A})$	$\cdot * \neg \mathbf{Q}$	
	(10)	~	$\mathbf{T}_{d+1} \coloneqq \tilde{\mathbf{Q}}$		$ ilde{\mathbf{Q}} \qquad d{++}$
	(11)	for $\tilde{d} :=$	$d \mathbf{to} 3$		
Rollback	12	do			
& Tally	$\{13$		$\mathbf{W} := \mathbf{T}_{ ilde{\mathcal{J}}}$.	$*$ $(1 + \tilde{\mathbf{C}})$./ Q
	14		$\tilde{\mathbf{C}} += (\tilde{\mathbf{A}} \mathbf{V})$	$(\mathbf{V}^T)^T$. *	$\mathbf{T}_{ ilde{d}-1}$.* \mathbf{Q}
	15	\mathbf{c} += \sum	$\sum_v \widetilde{\mathbf{c}}_v$ —		



Parallel Algorithm

	$\mathbf{c}: \mathbb{I}$	$\mathbb{R}^{N}_{+} = \text{BetweennessCentrality}(\mathbf{A} : \mathbb{B}^{P_{c}(S(N \times N))})$
Change	1	$\boldsymbol{\mathfrak{T}}: \mathbb{B}^{S(d_{max}) \times \mathbf{v} \times P(S(N))} \qquad \mathbf{Q}: \mathbb{N}_{+}^{ \mathbf{v} \times P(N)} \qquad \tilde{\mathbf{Q}}: \mathbb{N}_{+}^{ \mathbf{v} \times P(S(N))}$
matrices to	2	$\mathbf{W}: \mathbb{R}_{+}^{ \mathbf{v} \times P(S(N))} \qquad \tilde{\mathbf{C}}: \mathbb{R}_{+}^{ \mathbf{v} \times P(N)} \qquad \mathbf{c}, : \mathbb{R}_{+}^{N}$
parallel	3	for $\mathbf{v} \in V$
arravs	4	do
anays	5	$d := 1$ $\mathfrak{T} := 0$ $\tilde{\mathbf{C}} := 0$
	6	$\mathbf{T}_d := \mathbf{Q} := ilde{\mathbf{Q}} := \mathbf{I}(\mathbf{v},:)$ Parallel Sparse
	7	while $\mathbf{T}_d \neq 0$ Matrix-Matrix
	8	do
	9	$ ilde{\mathbf{Q}} := \left[ilde{\mathbf{Q}} \ \mathbf{A} ight]$. * $\neg \mathbf{Q}$
	10	$\mathbf{T}_{d+1} \coloneqq \tilde{\mathbf{Q}} \mathbf{Q} \not\models = \tilde{\mathbf{Q}} d++$
	11	for $\tilde{d} := d$ to 3
	12	do
	13	$\mathbf{W} := \mathbf{T}_{\tilde{i}} \cdot \mathbf{*} (1 + \tilde{\mathbf{C}}) \cdot \mathbf{V} \mathbf{Q}$
	14	$ ilde{\mathbf{C}} \mathrel{+}= (ilde{\mathbf{A}} \; \mathbf{W}^{T})^{T}$. * $\mathbf{T}_{ ilde{d}-1}$. * \mathbf{Q}
	15	$\mathbf{c} \mathrel{+}= \sum_v \widetilde{\mathbf{c}}_v$



- Do all vertices at once (i.e. |v|=N)
 - N = # vertices, M = # edges, k = M/N
- Algorithm has two loops each containing d_{max} sparse matrix multiplies. As the loop progresses the work done is
 - d=1 (2kM)
 - d=2 (2k²M) (2kM)
 - d=3 (2k³M 2k²M) (2k²M 2kM)
- Summing these terms for both loops and approximating the graph diameter by d_{max} ≈ log_k(N) results in a complexity

 $4 \text{ k}^{\text{dmax}} \text{ M} \approx 4 \text{ N} \text{ M}$

• Time to execute is

 $T_{BC} \approx 4 \text{ N M}$ / (e S) where S = processor speed, e = sparse matrix multiply efficiency

• Official betweenness centrality performance metric is Traversed Edges Per Second (TEPS)

TEPS = $NM/T_{BC} \approx (e S) / 4$

Betweenness Centrality tracks Sparse Matrix multiply performance



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Matlab Implementation

- Array code is very compact
- Lingua franca of DoD engineering community
- Sparse matrix matrix multiply is key operation

```
function BC = BetweennessCentrality(G,K4approx,sizeParts)
  declareGlobals;
  A = logical(mod(G.adjMatrix,8) > 0);
  N = length(A); BC = zeros(1,N); nPasses = 2^K4approx;
 numParts = ceil(nPasses/sizeParts);
  for(p = 1:numParts)
   BFS = [];
                    depth = 0;
   nodesPart = ((p-1).*sizeParts + 1):min(p.*sizeParts,N);
    sizePart = length(nodesPart);
   numPaths = accumarray([(1:sizePart)',nodesPart']...
       ,1,[sizePart,N]);
    fringe = double(A(nodesPart,:));
    while nnz(fringe) > 0
        depth = depth + 1;
        numPaths = numPaths + fringe;
        BFS(depth).G = logical(fringe);
        fringe = (fringe * A) .* not(numPaths);
    end
    [rows cols vals] = find(numPaths);
    nspInv = accumarray([rows,cols],1./vals,[sizePart,N]);
   bcUpdate = ones(sizePart,N);
    for depth = depth: -1:2
        weights = (BFS(depth).G .* nspInv) .* bcUpdate;
        bcUpdate = bcUpdate + ...
          ((A * weights')' .* BFS(depth-1).G) .* numPaths;
    end
   bc = bc + sum(bcUpdate,1);
  end
  bc = bc - nPasses;
```



Matlab Profiler Results

g Window Help				
A				
n this code: RUN_graphAnalysis			Pro	ofile time: 4
re the most time was spent				
Code	Calls	Total Time	% Time	Time Plot
<pre>fringe = (fringe * adjacencyMa</pre>	20	11.443 s	37.0%	-
bcUpdate = bcUpdate +	18	9.878 s	31.9%	-
weights = (BFS(depth).G .* nsp	18	6.717 s	21.7%	-
<pre>numShortestPaths = numShortest</pre>	20	1.603 s	5.2%	1 - C
<pre>nspInv = accumarray([rows,cols</pre>	2	0.341 s	1.1%	1
		0.979 s	3.2%	r.
		30.962 s	100%	
	g Window Help M n this code: RUN_graphAnalysis re the most time was spent Code fringe = (fringe * adjacencyMa bcUpdate = bcUpdate + weights = (BFS(depth).G .* nsp numShortestPaths = numShortest nspInv = accumarray([rows,cols	g Window Help M in this code: RUN_graphAnalysis re the most time was spent Code Code Calls fringe = (fringe * adjacencyMa 20 bcUpdate = bcUpdate + 18 weights = (BFS(depth).G .* nsp 18 numShortestPaths = numShortest 20 nspInv = accumarray([rows,cols 2	g Window Help Help M Code: RUN_graphAnalysis re the most time was spent Code Calls Total Time fringe = (fringe * adjacencyMa 20 11.443 s bcUpdate = bcUpdate + 18 9.878 s weights = (BFS(depth).G .* nsp 18 6.717 s numShortestPaths = numShortest 20 1.603 s nspInv = accumarray([rows,cols 2 0.341 s 30.962 s 30.962 s	Window Help # Image: Colspan="2">Image: Colspan="2">Image: Colspan="2" Processing of the most time was spent Code Calls Total Time % Time fringe = (fringe * adjacencyMa 20 11.443 s 37.0% bcUpdate = bcUpdate + 18 9.878 s 31.9% weights = (BFS(depth).G .* nsp 18 6.717 s 21.7% numShortestPaths = numShortest 20 1.603 s 5.2% nspInv = accumarray([rows,cols 2 0.341 s 1.1% 0.979 s 3.2% 30.962 s 100%

• Betweenness Centrality performance is dominated by sparse matrix matrix multiply performance



• Software Lines of Code (SLOC) are a standard metric for comparing different implementations

Language	SLOCs	Ratio to C
C	86	1.0
C + OpenMP (parallel)	336	3.9
Matlab	28	1/3.0
pMatlab (parallel)	50 (est)	1/1.7 (est)
pMatlabXVM (parallel out-of-core)	75 (est)	1 (est)

- Matlab code is small than C code be the expected amount
- Parallel Matlab and parallel out-of-core are expected to be smaller than serial C code





- Canonical graph based implementations
- Performance limited by low processor efficiency (e ~ 0.001)
 - Cray Multi Threaded Architecture (1997) provides a modest improvement

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COTS Serial Efficiency



 COTS processors are 1000x more efficient on sparse operations than dense operations

Parallel Results (canonical approach)



- Graph algorithms scale poorly because of high communication requirements
- Existing hardware has insufficient bandwidth

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Performance vs Effort



Relative Code Size (i.e Coding Effort)

- Array (matlab) implementation is short and efficient
 - 1/3 the code of C implementation (currently 1/2 the performance)
- Parallel sparse array implementation should match parallel C performance at significantly less effort



Why COTS Doesn't Work?



- Standard COTS architecture requires algorithms to have regular data access patterns
- Graph algorithms are irregular, caches don't work and even make the problem worse (moving lots of unneeded data)



Summary Embedded Processing Paradox

- Front end data rates are much higher
- However, back end correlation times are longer, algorithms are more complex and processor efficiencies are low
- If current processors scaled (which they don't), required power for back end makes even basic graph algorithms infeasible for embedded applications

	Front End	Back End
Data input rate	Gigasamples/sec	Megatracks/day
Correlation time	seconds	months
Algorithm complexity	O(N log(N))	O(N M)
Processor Efficiency	50%	0.05%
Desired latency	seconds	minutes
Total Power	~1 KWatt	>100 KWatt

Need fundamentally new technology approach for graph-based processing



Backup Slides



Motivation: Graph Processing for ISR



Algorithms	Signal Processing	Graph	
Data	Dense Arrays	Graphs	
Kernels	FFT, FIR, SVD,	BFS, DFS, SSSP,	
Parallelism	Data, Task,	Hidden	
Compute Efficiency	10% - 100%	< 0.1%	

- Post detection processing relies on graph algorithms

 Inefficient on COTS hardware
 - Difficult to code in parallel

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FFT = Fast Fourier Transform, FIR = Finite Impulse Response, SVD = Singular Value Decomposition BFS = Breadth First Search, DFS = Depth First Search, SSSP = Single Source Shortest Paths