Designing Processing Architectures for Space Applications

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Abstract

Designing processors for space presents unique challenges. Challenging form factors, environmental requirements, packaging demands, thermal limits, material restrictions, and size, weight, and power goals all contribute to the complexity of the design trade space and limit component choices within the trade space. Testing and screening parts and components for space applications is limited within the market – a component that is functionally suitable for the processor might not have the screening pedigree to allow its use without research and testing. This paper will address these obstacles, give guidance for solutions, and provide some examples.

Space Application Considerations

This paper will address the requirements and issues in the following areas:

- Environmental
- Thermal
- Packaging
- SWAP (size, weight and power)

This paper will also address issues with components and technologies commonly used in open systems architectures such as:

- Memories – SRAM, DRAM, EEPROM, and Flash
- Field programmable logic devices (FPGA) – RAM-based, anti-fuse, and Flash-based
- Application Specific Integrated Circuits (ASIC)
- High IO packaging – Ball grid arrays (BGA) and column grid arrays (CGA)
- Future trends

Environment and Radiation

Radiation is the most challenging of the environmental considerations. Total dose radiation requirements depend on the operation and the orbit of the spacecraft and range from radiation tolerant ($<50 \times 10^3$ rads) to radiation hardened (1×10^6 rads) [1]. Radiation requirements depend on orbit altitude, electronics packaging or shielding, and mission profile.

Another consideration of the radiation environment is single event effects (SEE). These effects include single event upset (SEU), single event latch-up (SEL; both destructive and non-destructive), and single event functional interrupt (SEFI).

In the past, both total radiation dose and SEEs were major considerations. Now, as integrated circuit feature sizes have become smaller, total dose radiation tolerance has improved and SEEs have become a more dominant consideration.

Thermal

Because of the vacuum in space, computing technologies for space must be conduction cooled. This is a more challenging form factor than many commercial off-the-shelf (COTS) technologies which are air-cooled. The conventional conduction-cooled approach to electronics packaging has thermal conduction on the bottom (or PC board) side of the components, with thermal conduction through the PC board to a bonded heat sink.

Today's computing technologies – both processors and large field programmable gate arrays (FPGA) – use flip-chip packaging where heat conduction is through the *top* of the package making conventional thermal management methods less efficient. New approaches, such as bathtub heat sinks or thermal pads and cooling rails, are required in order to use the new computing technologies.

Spacecraft electronics can be subject to a high number of temperature cycles over the course of the mission duration. A typical low earth orbit spacecraft will orbit 15 times a day, cycling between exposure to direct solar radiation and deep space on each orbit. For a 5 year mission, the total is over 25,000 thermal cycles. The thermal, mechanical, electrical, and component engineers must work closely to mitigate the effects of the thermal cycling.

Packaging

Packaging for space applications presents unique challenges because of the heat conduction and shielding requirements and the challenging form factors needed to minimize size, weight and power. Heat conduction in the space environment requires conduction cooling to radiation fins or liquid cooling thermal interfaces. Shielding is required to meet radiation requirements and shielding can be applied at the component, assembly, and subsystem levels. Shielding can improve total dose susceptibility but is generally ineffective and impractical for SEE reduction.

Minimizing size, weight, and power requires unique packaging techniques and materials. Maintaining good system grounding becomes a challenge as some desirable light-weight materials are not conductive.

Size, Weight, and Power (SWAP)

Size, weight and power (SWAP) are each important considerations, but often for computing technologies power is the primary consideration. Reducing power for electronics assemblies reduces the mass required for thermal conduction (reducing size and weight) and reduces the power supply requirements (reducing size and weight). Power is an important factor in the trade space when

selecting components. FPGAs have a number of advantages over application-specific integrated circuits (ASIC) in terms of reprogrammability, lead time, simulation and verification time, and fabrication time but require more circuit board area to support reprogrammability. In general, ASICs consume less power than FPGAs, especially for processing-intensive applications.

Memories

Memory devices require tradeoffs between size and radiation susceptibility for both volatile and nonvolatile storage. In general, radiation hardened SRAM and EEPROM memories are available but are smaller and slower than DRAM and Flash respectively. In many applications, commercial devices can be used in concert with mitigation techniques such as error detection and correction (EDAC). Space applications can use powerful EDAC techniques combined with memory scrubbing and device screening to create a robust memory implementation for relatively low recurring cost.

Processing architectures that minimize the amount of memory have the advantages of reduced SWAP and radiation susceptibility, and thereby reduced cost.

FPGAs

Field programmable logic devices (FPGA) are available in a variety of technologies – anti-fuse, Flash-based, and RAM-based. The logic configuration mechanism of an anti-fuse FPGA is inherently radiation hard. Radiation hardened products are readily available with built-in mitigation for SEE. However, anti-fuse devices are one-time programmable. Flash-based FPGAs are reprogrammable but currently require appropriate testing and SEE mitigation; their total dose tolerance is currently low compared with anti-fuse and RAM-based devices.

RAM-based FPGAs are faster, easily reprogrammable, and available with mitigation for SEL. However, both the logic and the configuration have the same issues as volatile memory devices and require SEU and SEFI mitigation techniques such as triple module redundancy (TMR), EDAC, memory checking, and memory scrubbing. A large nonvolatile memory is required for storing the RAM-based FPGA configuration, which adds to the SEU challenge.

ASICs

A small number of radiation-hardened fabrication processes are available for application specific integrated circuits (ASIC). Commercial fabrication lines are more numerous and have more advanced integrated circuit feature sizes and technologies. ASIC design and fabrication options for space applications include utilizing a radiation-hardened process or using a commercial process and testing or screening parts for the appropriate environmental levels. Some projects might choose the option of fabricating engineering components in a commercial process for prototypes and then migrating the design to a radiation hardened process.

High IO Packaging

High Input-Output (IO) ball grid array (BGA) and column grid array (CGA) packages provide the user with large numbers of input, output, and power connections but in a form factor more susceptible to damage from the expansion and contraction of thermal cycles. Ceramic packages meet the hermeticity requirements of some space applications but are incompatible with the coefficient of expansion for common circuit board materials. Plastic packages are more compatible with common plastic board materials but are not hermetically sealed. High IO packaging requires material reviews as well as thermal cycle testing with the intended circuit board material.

Dense memory devices are often packaged in plastic thin-shrink small outline packages (TSSOP). These packages might be only slightly larger than the die and have very short leads. The result is that the package provides little or no compliance and the silicon die does not provide a good thermal match for the circuit board material. Thus TSSOPs also present a thermal cycling problem.

Future Trends

Advanced nonvolatile memory technologies promise higher storage density with increased radiation tolerance than current devices. Ferroelectric and phase-change technologies are quickly moving from the laboratory into production, though densities will need to increase to gain acceptance.

The trend towards reduced feature sizes in processors has the added benefit, besides higher performance, of decreasing the total dose susceptibility of advanced devices. However, the devices are more susceptible to single event effects since lower-energy particles cause upsets.

Efforts to design reprogrammable FPGAs that are inherently radiation-tolerant are underway for both RAM-based and Flash-based devices.

Packaging issues will become more difficult. Commercial packages will continue to become denser with higher pin counts and smaller contact pitches. Large ceramic column grid array packages with flip chips already are being delivered without hermetic sealing. Chip scale packaging is the final evolution.

Summary

Designing processors for space presents unique challenges such as challenging form factors, environmental requirements, packaging demands, thermal limits, material restrictions, and size, weight, and power limits. These challenges limit component choices, but appropriate risk mitigation and testing programs can expand component selection and make use of more of the processing technologies available for open system architectures.

References

[1] J. Wertz and W. Larson, *Space Mission Analysis and Design*, Third Edition, Microcosm Press, 1999.