High-Performance, Parallel Embedded Architectures Using Acalis® CPU872 PowerPC® Multicore

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Introduction

The demand for computing capacity continues to climb for embedded computing. Sensor fusion, autonomous operation, and more advanced radar processing, for example, are all driving the need for more throughput than previously. However, the size, power, and weight constraints remain. In fact, for some applications such as mini UAVs, the requirements have become even more stringent. Multicore System-on-Chips (SOCs) are becoming available that offer high performance and integration with significantly lower power dissipation. These devices meet the needs of applications with challenging form factors as well as other less strenuous uses. This paper discusses one such multicore SOC, the Acalis CPU872, including specifications, benchmark results, how it is currently being applied and how it can be configured for various types of computing. Currently available, the SOC is fabricated at the TAPO/ IBM Trusted foundry under Navy sponsorship.

CPU872 Architecture Overview

Traditional architectures rely on brute force, high frequency clocking to achieve their performance at the expense of computing efficiency and power. For real-world applications, external transactions to a processor's I/O subsystems, DRAM memory, or another processor can cause the average sustained performance to drop down to 20% of the peak. Disabling the clocks on unused functions helps reduce the power, but does nothing to address the efficiency issue. The streaming-based architecture of the Acalis CPU872 enables it to achieve comparable sustained performance at a lower frequency and a much lower power. The maximum sustained performance is 3.6 GOPS/GFLOPS using only 8 Watts under typical conditions. As shown in figure 1, it is implemented with two PowerPC 440 cores, embedded DRAM, and routing hardware. Each dual-issue PowerPC 440 core has its own double precision floating point unit, a 32KBI/32KBD Level 1 cache, a 256KB Level 2 Cache, a 4MB embedded DRAM, an interface to external DDR2 RAM, a streaming processor, a DMA engine, and hardware accelerators for MPI. A shared, programmable, data router communicates with other chips via five, 10 Gb/sec data links using 64-bit addresses. A 10/100/1000 Ethernet controller provides a connection to a host computer or other external computing device. The built-in anti-tamper and anti-reverse-engineering hardware is further supported by a secure bootstrap interface. The chip has a 31 x 31 mm, 899-pin package.

More details of the Acalis CPU872 chip architecture will be described during the conference presentation.

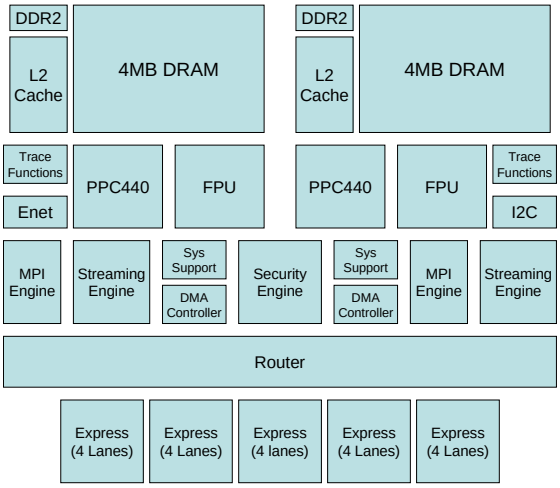

Figure 1: CPU872 Block Diagram.

CPU872 System Operations

The Acalis CPU872 can operate with or without external DDR2 RAM. Applications with moderate code and data requirements that can fit within 4 MB per processor allow very dense hardware implementations; an n-processor parallel architecture requires only n/2 CPU872 chips and clock drivers, one application-specific data interface chip, plus a constant (and small) number of bootstrap and system control chips. Applications with larger code and data requirements can have up to 4 GB of DDR2 ECC RAM per processor (thus, two, 4GB DDR2 RAM DIMMs per CPU872 chip).

The Acalis CPU872 supports a non-uniform-memory-access (NUMA) memory model with 64-bit addressing. The data routers can be configured to allow any processor to directly access the memory of any other processor in the parallel architecture. Alternatively, the data routers can be configured to isolate subsets of the architecture; this would enable multiple developers to concurrently test software running on a parallel architecture, without interfering with each others' computational results or performance.

Controlled communication among processors, via the Message Passing Interface (MPI) standard [1], are supported by an MPI accelerator for each processor that implements low-level MPI functions, including barrier synchronization, in hardware.

As with any NUMA architecture, the highest performance will be achieved when the parallel architecture's datapaths match the communication requirements of the parallel algorithms.

Configuration Examples

With five high-speed links per Acalis CPU872 chip, plus a 10/100/1000 Ethernet link per chip, a multitude of network topologies can be constructed, supporting a wide variety of parallel algorithms. These links also provide considerable flexibility in connecting the network processors to host computers or other external devices. A few configurations are shown as examples.

A 2-dimensional mesh can be built with arbitrary dimension, without increasing the length of interconnecting wires. Furthermore, many physical processes operate in two dimensions, so it is straightforward to design parallel algorithms that map, well, into two-dimensional meshes. The 12-processor, 2x3, toroidal mesh, shown in figure 2, has direct links between every processor and its neighbor in the X or Y dimension. Here, the extra link at each CPU872 chip is used to connect to external devices sending and/or receiving data.

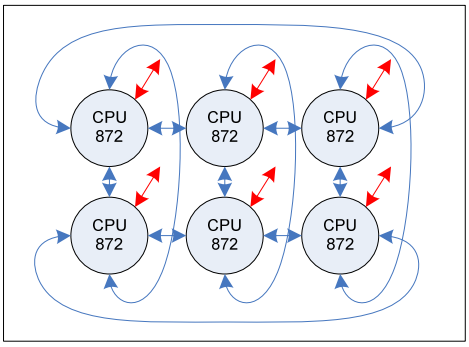

Figure 2: 2x3 Toroidal Mesh with Parallel Datapaths to External Devices

Note that, for larger meshes, the longer "end-around" links do not grow in length, because the mesh is folded over on itself, such that the physical distance between any two logically-adjacent nodes is no longer than twice the minimum physical distance, as shown in figure 3.

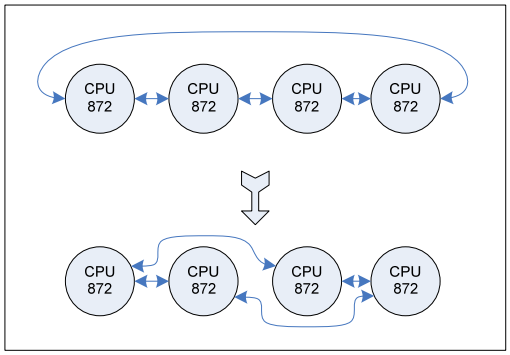

Figure 3: Folding to Reduce Maximum Link Length

In a development environment, productivity can be substantially enhanced if multiple developers can work on the same hardware simultaneously, but without interfering with each other. Figure 4 shows how a 12-processor toroidal mesh can be temporarily configured as two, 6-processor toroidal meshes by disabling the north and south links of each chip. Here, the red links connect to one or more host computers in the development environment.

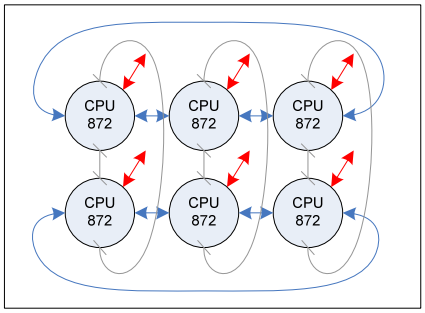

Figure 4: 2x1x3 Toroidal Mesh, with Connections to Host Computers.

For algorithms that consist of several stages of independent processing of parallel data, pairs of links can be combined to double not only the inter-stage bandwidth, but the data throughput into and out of the parallel processing array, as well. Figure 5 illustrates one such multi-stage network.

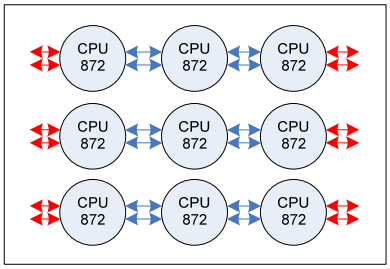

Figure 5: 3-Stage Network with Double Inter-stage Datapaths

Other topologies possible with the Acalis CPU872 chip include three-dimensional meshes, tree structures, and three-, four-, and five-dimensional hypercubes. Some of these additional topologies will be illustrated during the conference presentation.

Performance Benchmarks

The Acalis CPU872 provides, in a single chip, a two-node building block for a variety of parallel architectures of arbitrary size. Multiple high-speed interconnects and hardware support for MPI, message routing, DMA, and data streaming ensure that data communication within the parallel architecture operate with high bandwidth and low latency to maximize efficiencies. Hardware support for tamper protection and anti-reverse-engineering, as well as fabrication at the TAPO/IBM Trusted Foundry, supports the implementation of the most sensitive of applications.

We shall present performance measurements for a number of single-processor and multiprocessor benchmarks, including the hpecChallenge-1.0 benchmarks and the MPI Bandwidth-Latency-Benchmark from the University of Stuttgart. In particular, we will evaluate those which represent realistic applications such as the HPEC Challenge SAR benchmark. Preliminary results from Navy sponsored STAP evaluation will also be presented.

References

[1] http://www-unix.mcs.anl.gov/mpi/

Acknowledgements

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