Experience and results porting HPEC Benchmarks to MONARCH

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The MONARCH Processor

MONARCH is a high performance processing chip developed by Raytheon and USC ISI, under the DARPA XMONARCH contract. MONARCH provides high throughput (up to 64 GFLOPS) in a power efficient balanced architecture [1].

The MONARCH chip includes six RISC processors, 12 Mbytes of on chip dynamic RAM (DRAM), two DDR2 ports, two serial RapidIO ports, sixteen 2.6 Gbyte/s streaming I/O ports, and a reconfigurable compute array (FPCA) – see Figure 1. MONARCH chips can boot from a single commercial Flash part, providing a highly embeddable System on a Chip (SOC) processing solution; or they can be gluelessly tiled to provide a teraFLOP embedded processor.

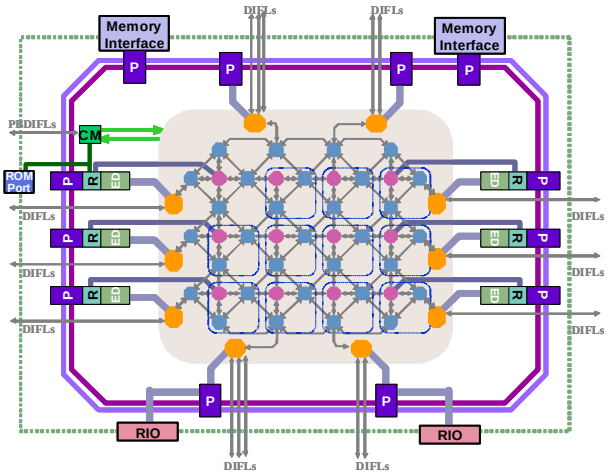

Figure 1 – MONARCH Chip Architecture

The Field Programmable Compute Array (FPCA) is key to the MONARCH chip's high performance, efficiency and morphability. The FPCA contains 96 Multiplier-ALUs, 124 dual-port memories, 248 address generators, and 20 DMA engines all connected through a rich, dynamically switched, interconnect. The architecture of the FPCA has been optimized for signal processing algorithms, for example FFT and FIR, using 16 and 32 bit integer, and 32 bit IEEE floating data. The FPCA supports streaming data with hardware support for dataflow synchronization, and uses a novel distributed programming paradigm.

MONARCH is a scalable processing solution for many DoD systems, including Radar, E/O, Missile, Communications and SIGINT. MONARCH chips are in the lab and being used to run software and perform demonstrations.

HPEC Benchmarks

The High Performance Embedded Computing (HPEC) Challenge benchmark suite consists of a set of single-processor kernel benchmarks and a multiprocessor application benchmark. The kernel benchmarks address important operations across a broad range of DoD signal and image processing applications. The application benchmark implements a scalable Synthetic Aperture Radar (SAR) application that is representative of one of the most common functions in DoD surveillance systems.

Our presentation will describe the results of running three of the HPEC kernels on MONARCH: Large matrix transpose (corner turn), Constant False-Alarm Rate detection (CFAR) and QR factorization. We will provide an overview of each of the benchmarks, the implementation approach we used, and the performance results we obtained on MONARCH.

In addition, we will focus on one of the benchmarks (QR factorization) in more detail – discussing the details of the implementation such as: trade-offs between implementation options, theoretical limits imposed by on chip EDRAM bandwidth, implementation of floating point division and square root in the FPCA.

This talk should be of interest to those considering using MONARCH as an enabler for next generation systems, and also for anyone interested in techniques for performing QR factorization on parallel, and in particular reconfigurable processors.

References

References should be listed in the format shown below with numbering in square brackets. References ("Reference" style) should be set at Times 9 pt font and fully justified within the column.

[1] L. Lewins et al., *"World's First Polymorphic Computer – MONARCH"*, HPEC, 2007.

[2] R Haney et al., *"The HPEC Challenge Benchmark Suite"*, HPEC, 2005.