Using MONARCH for High Performance Processing
A Case Study for CT Reconstruction

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The Compact VAC System

An advanced Computed Tomography (CT) system is being developed by Multi-Dimensional Imaging, under a DARPA contract. This CT system will allow combat casualty assessment techniques in forward battlefield mobile vans and deployable medical systems. In order to achieve these medical capabilities it is essential to provide CT volume images in real time. To achieve this real-time goal it is necessary to develop a computational platform that can supply 5-10 trillion floating point operations per second (TFLOP/S).

However, this compute capacity must be made available in a mobile environment where only kilowatts of capacity are available in the compute power budget. Traditionally, computers capable of supplying this much throughput reside in air-conditioned data centers with power systems supplying thousands of kilowatts.
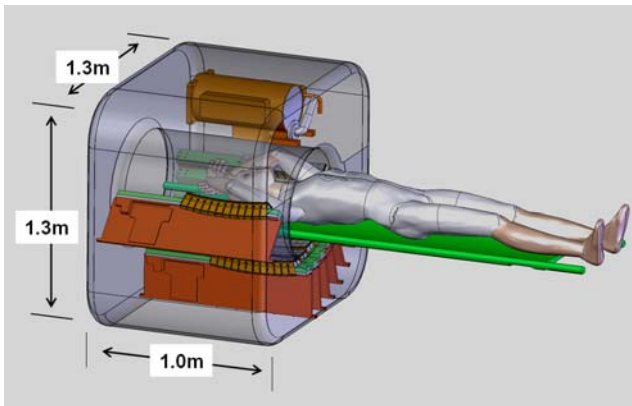

Figure 1 – Compact VAC Scanner

The MONARCH Processor

MONARCH is a high performance processing chip developed by Raytheon and USC ISI, under the DARPA XMONARCH contract. MONARCH is a scalable processing solution for many DoD systems and provides exceptional compute capacity and highly flexible data bandwidth capability coupled with state-of-the-art power efficiency and full programmability. Laboratory tests have demonstrated that the MONARCH processor can sustain 64 GFLOP/S of throughput while consuming less than 20 Watts, resulting in one of the most power-efficient processors available [1].

Real-time CT Reconstruction

Using MONARCH to provide a mobile, low power solution for real-time CT Reconstruction is a natural fit. In this presentation we will discuss the steps involved in CT cone-beam reconstruction with special emphasis on the backprojection mapping process. Next we will review the processing requirements of this algorithm, for a particular set of system parameters, and then demonstrate how these requirements were mapped to a MONARCH-based solution. We will also review some of the unique features of MONARCH and show how they might be applied to other systems what require high throughput at low power.

This presentation will be of interest to anyone designing high performance, embedded processing systems, especially those based on the MONARCH chip.
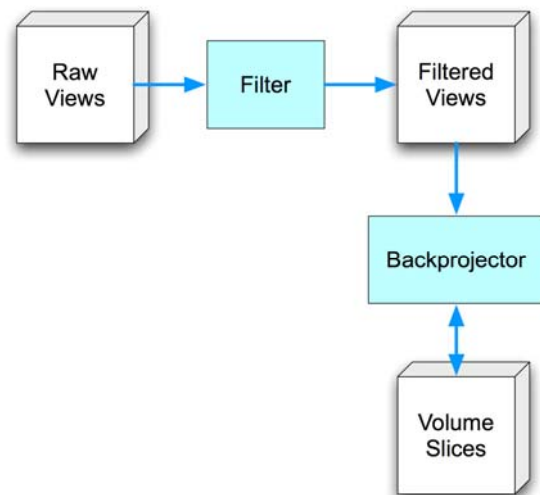

Figure 2 – CT Cone-beam Reconstruction Overview

References

[1] L. Lewins et al., "*World's First Polymorphic Computer – MONARCH*", HPEC, 2007.