

Challenges Drive Innovation



Implementation of Polar Format SAR Image Formation on the IBM Cell Broadband Engine

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Hardware and Software Platforms

- Benchmark Implementation
- Performance Estimate
- Summary

Hardware: Cell Processor



Synergistic Processing Unit

with SIMD engine

Memory Flow Controllers and

Processing •

- 1 PowerPC Processing Element (PPE) and 8 Synergistic Processing Elements (SPE)
- Memory
 - External XDR
 - SPE local store of 256 kB for instructions and data
- **Data Transfer Rates**
 - Maximum transfer rate of XDR is 25.6 GBps
 - Maximum transfer rate of EIB is 192 GBps
- **Memory Alignment Restrictions** •
 - 128 bytes DMA packets



Hardware: Dual Cell Blade



DCBB1 Dual Cell-Based Blade

- 2 Cell BE processors directly mounted on the board
- 7 double-width Dual Cell-Based Blades fit in one 9U BladeCenter H chassis
- 512 MB of XDRTM DRAM per Cell BE processor
- PCI Express® x4 interface to two daughtercard locations



Software: MultiCore Framework -- MCF



- PPE acts as manager and coordinator
- SPEs do all the hard work in teams



MCF – Features



- PPE Manager creates a Network of 1 to 8 Worker SPEs
 - An SPE can belong to only 1 MCF network
- PPE Manger directs Teams of Worker SPEs to run Tasks
 - Tasks have a main()
 - An SPE runs one task at a time (run to completion model)
 - SPEs may belong to multiple teams

MCF Network enables

- Barrier synchronization
- Semaphores
- Access to remote "named" memory
- Message queues
- Mailboxes
- Tile channels
- Low level DMA control
- SPE Tasks may dynamically load & un-load Plug-In code
 - Plug-Ins do not have a main()
 - Currently limited to single object file per Plug-In
- MCF Profiler permits post mortem analysis of execution profile
 - Quick location of software bugs
 - Isolate areas for optimization

MCF – Tile Channels



• Tile channels provide simplified dataflow management

- Tile channel automatically distributes data to and collects data from SPEs
- Overlap computation and communication
- Multi-buffering
- Global data reorganization



MCF – Tile Channel -- Processing Loop



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Lightweight functions used to maximize performance during processing



Presentation Outline



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SAR Data Collection Geometry



Image resolution depends on scenario geometry

- Low azimuth resolution requires a small aperture
 - Radar beams are approximately parallel when aperture is small and distance to scene is large
 - Data samples fall approximately on a rectangular grid
 - Only a 2D FFT is required to form the image
- High azimuth resolution requires a large aperture
 - Radar beams are not approximately parallel when aperture is large or distance to scene is small
 - Using rectangular approximation causes too much image distortion
 - Geometric correction of data required
 - Polar Format 🚤
 - Range Migration
 - Wavefront Reconstruction
 - Backprojection

Polar format uses the same building blocks as many other algorithms Computer Systems, Inc

Polar Format Algorithm



• Data is interpolated from a polar grid onto a rectangular grid

- Plot range samples for each pulse along k_R vectors
- Project k_R vectors onto k_x-k_y plane
- Interpolate k_P vectors in range
- Interpolate in azimuth between interpolated range samples
- Perform 2D FFT on interpolated samples



Based on "Spotlight Synthetic Aperture Radar, Signal Processing Algorithms" Carrara, Goodman, Majewski

Polar Format Algorithm - Implementation

Create interpolation grids -- PPE

- Create azimuth & elevation vectors
- Create U & V vectors

Range interpolate along each pulse -- SPE

- Compute k_R vector
- Compute k_p vector
- Upsample range along k_p by FFT interpolation
- Choose nearest neighbor range in V dimension
- Cornerturn range-sequential to azimuth-sequential
- Azimuth interpolate along each range line -- SPE
 - Upsample azimuth along k_v dimension by FFT interpolation
 - Choose nearest neighbor azimuth U dimension
- Cornerturn azimuth-sequential to range-sequential
- Range compression -- SPE
 - Single SPE for up to 10K point FFT
 - Distributed FFT using Cooley-Tukey algorithm for larger sizes
- Cornerturn range-sequential to azimuth-sequential
- Azimuth compression -- SPE
 - Single SPE for up to 10K point FFT
 - Distributed FFT using Cooley-Tukey algorithm for larger sizes
- Cornerturn azimuth-sequential to range-sequential

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Range and Azimuth Interpolation



Data is partitioned into tiles of 512 range samples with overlap (32 before, 32 after) Loop for each pulse (each SPE gets a group of pulses)

- Loop for each range tile in a pulse (all tiles for a pulse processed in same SPE) Send range tile to SPEs
 - Upsample range block by 8
 - **512 point FFT performed on range block**
 - Zero-pad range block to 4096 points
 - 4096 point IFFT performed on zero-padded range block
- Choose interpolated range points closest to output vector coordinates

Send interpolated range points back to XDR



Range interpolation shown in diagram. For azimuth interpolation, switch range and pulse dimensions

Tiling Computations



• Tile overlap overhead

- Must overlap by 1 sample to avoid skipping interpolation points between tiles
- Overlap by 128 bytes (32 floats) for optimum DMA performance
- Overlap before and after to allow Gibb's ripples from FFT upsampling to be discarded
- Creates overhead in upsampling process slight decrease in efficiency

• Tiles in input and output are not one-to-one due to offset and scaling

- Interpolation indices computed on the fly to maximize allocation of main memory for image planes
- Zero, one, or more output tiles may be generated for any one input tile
- Only complete tiles are sent back through return channel (last tile may be padded)



SPE Memory Allocation



- Input buffer oversized to reuse as interpolator buffer
- Index buffer directs subsampled interpolated sequence to output buffer
- Output buffer is aligned and padded for efficient DMA
- Roughly 1/2 of the 256 kB SPE local store used for code
 - Further optimization for smaller code footprint would allow for bigger buffers, decreased tile overlap and better efficiency



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Interpolation Performance - 3.2 GHz Cell Processor



SAR Scenario – 0.3 m Resolution



- Analysis of specifications determines video phase history dimensions
- Benchmark 10K x 10K video phase history chosen for consistency with scenario

Specifications	
Frequency (GHz)	10
Bandwidth (MHz)	600
Range to Scene Center (km)	200
Az Resolution (m)	0.3
Range Resolution (m)	0.3
Squint Angle (deg)	90
Cross-Range Width (m)	2000
Range Width (m)	2000

Assumed Parameters	
Aircraft Velocity (m/s)	176
A/D Complex Sample Rate (MSps)	100
Pulse Width (usec)	100
PRF (Hz)	150

Derived Parameters	
Synthetic Aperture Length (m)	13000
Synthetic Aperture Time (sec)	73.86
Coherent Integration Angle: ∆Θ (deg)	3.7
Two-Way Travel Time to Scene Center (usec)	1333.3
Patch Propagation Time (usec)	6.7
Azimuth Chirp Rate (Hz/sec)	10.3
Doppler Bandwidth for Scene Center (Hz)	762.7
De-chirped Doppler Bandwidth (Hz)	117.3
Range Bandwidth after Dechirp (MHz)	80.0
Complex Samples per Pulse	11334
Pulses per Aperture	11080
Video Phase History Memory (MB)	958.1

Analysis based on "Spotlight Synthetic Aperture Radar, Signal Processing Algorithms" Carrara, Goodman, Majewski

SAR Scenario – 0.3 m Resolution



Processing time estimate for 10K x 10K video phase history

- Interpolation c-code developed using MCF Tile Channels and SAL
- *Compression FFT estimates based on current SAL library for Cell*
- Cornerturn c-code developed using MCF DMA features and SAL

Large margin available in Cell for additional processing

Synthetic Aperture Time (sec): 73.86 sec.

- Estimate for 10K x 10K SAR VPH input:
- Range Interpolation: 1.86 sec (53.8 Mpixel/sec)
- Cornerturn: 0 11 sec
- Azimuth Interpolation: 1.86 sec (53.8 Mpixel/sec)
- Cornerturn: 0.11 sec
- Range Compress: 0.08 sec (1250 Mpixel/sec)
- Cornerturn: 0.11 sec
- Azimuth Compress: 0.08 sec (1250 Mpixel/sec)
- Total processing time: 4.21 sec.

- (909 Mpixel/sec)
 - (909 Mpixel/sec)
- (909 Mpixel/sec)

 - (23.8 Mpixel/sec)

SAR Scenario – 0.1 m Resolution



- Analysis of specifications determines video phase history dimensions
- Benchmark 4K x 4K video phase history chosen for consistency with scenario

Specifications	
Frequency (GHz)	16.7
Bandwidth (MHz)	2000
Range to Scene Center (km)	24
Az Resolution (m)	0.1
Range Resolution (m)	0.1
Squint Angle (deg)	90
Cross-Range Width (m)	300
Range Width (m)	300

Assumed Parameters	
Aircraft Velocity (m/s)	40
A/D Complex Sample Rate (MSps)	100
Pulse Width (usec)	40
PRF (Hz)	60

Derived Parameters	
Synthetic Aperture Length (m)	2812
Synthetic Aperture Time (sec)	70.30
Coherent Integration Angle: ∆Θ (deg)	6.7
Two-Way Travel Time to Scene Center (usec)	160.6
Patch Propagation Time (usec)	1.0
Azimuth Chirp Rate (Hz/sec)	7.4
Doppler Bandwidth for Scene Center (Hz)	520.0
De-chirped Doppler Bandwidth (Hz)	55.5
Range Bandwidth after Dechirp (MHz)	100.0
Complex Samples per Pulse	4200
Pulses per Aperture	4219
Video Phase History Memory (MB)	135.2

Analysis based on "Spotlight Synthetic Aperture Radar, Signal Processing Algorithms" Carrara, Goodman, Majewski

SAR Scenario – 0.1 m Resolution



Processing time estimate for 4K x 4K video phase history

- Interpolation c-code developed using MCF Tile Channels and SAL
- Compression FFT estimates based on current SAL library for Cell
- Cornerturn c-code developed using MCF DMA features and SAL

Large margin available in Cell for additional processing

Synthetic Aperture Time (sec): 70.30 sec.

- Estimate for 4K x 4K SAR VPH input:
- Range Interpolation: 0.30 sec
- Cornerturn: 0.02 sec
- Azimuth Interpolation: 0.30 sec
- Cornerturn: 0.02 sec
- Range Compress: 0.02 sec
- Cornerturn: 0.02 sec
- Azimuth Compress: 0.02 sec (1250 Mpixel/sec)
- Total processing time: 0.70 sec.

(53.8 Mpixel/sec)

- (909 Mpixel/sec) (53.8 Mpixel/sec)
- (909 Mpixel/sec)
- (1250 Mpixel/sec)
- (909 Mpixel/sec)
- (23.8 Mpixel/sec)

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Summary



- The Cell processor can implement SAR polar format image formation to provide 0.3 meter resolution over 2000 meter diameter scenes at 200 kilometer range in a fraction of the aperture collection time.
- The Cell SPE local store must be treated similarly to the cache in a conventional processor – data must be strip-mined into tiles. The use of the "MultiCore Framework" facilitates this data distribution and reorganization, provides high parallelization efficiency, and easily accommodates asynchronous input and output tiles.
- Efficient DMA using 128 byte rule adds only a small amount of overhead due to overlap which is already necessary to accommodate discarding Gibb's ripples in upsampling process using FFT/IFFT.
- An SPE distributed FFT* using 2D Cooley-Tukey approach would be needed for larger upsampling ratios to avoid too much overlap. 2D distributed FFTs would also be necessary for compressing dimensions larger than 10k.