Announcing PWRficient Processors from PA Semi, the Most Power Efficient, High Performance Processors Available

PA SEMI

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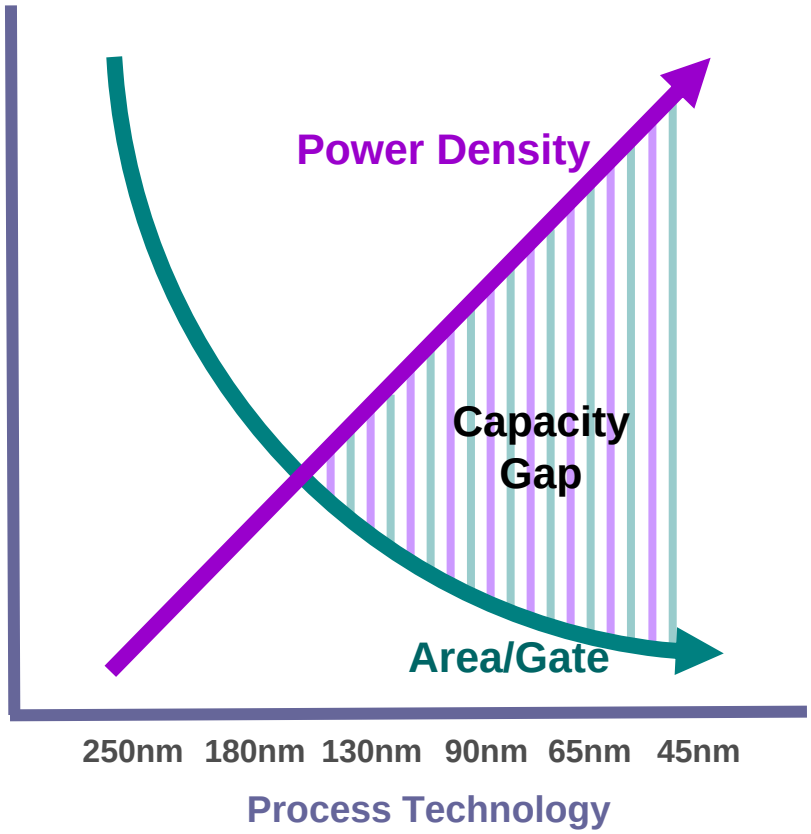
PWRficient™
Cool, High-Performance
MICROPROCESSORS

COOL IS THE NEW HOT

The Escalating Power Problem



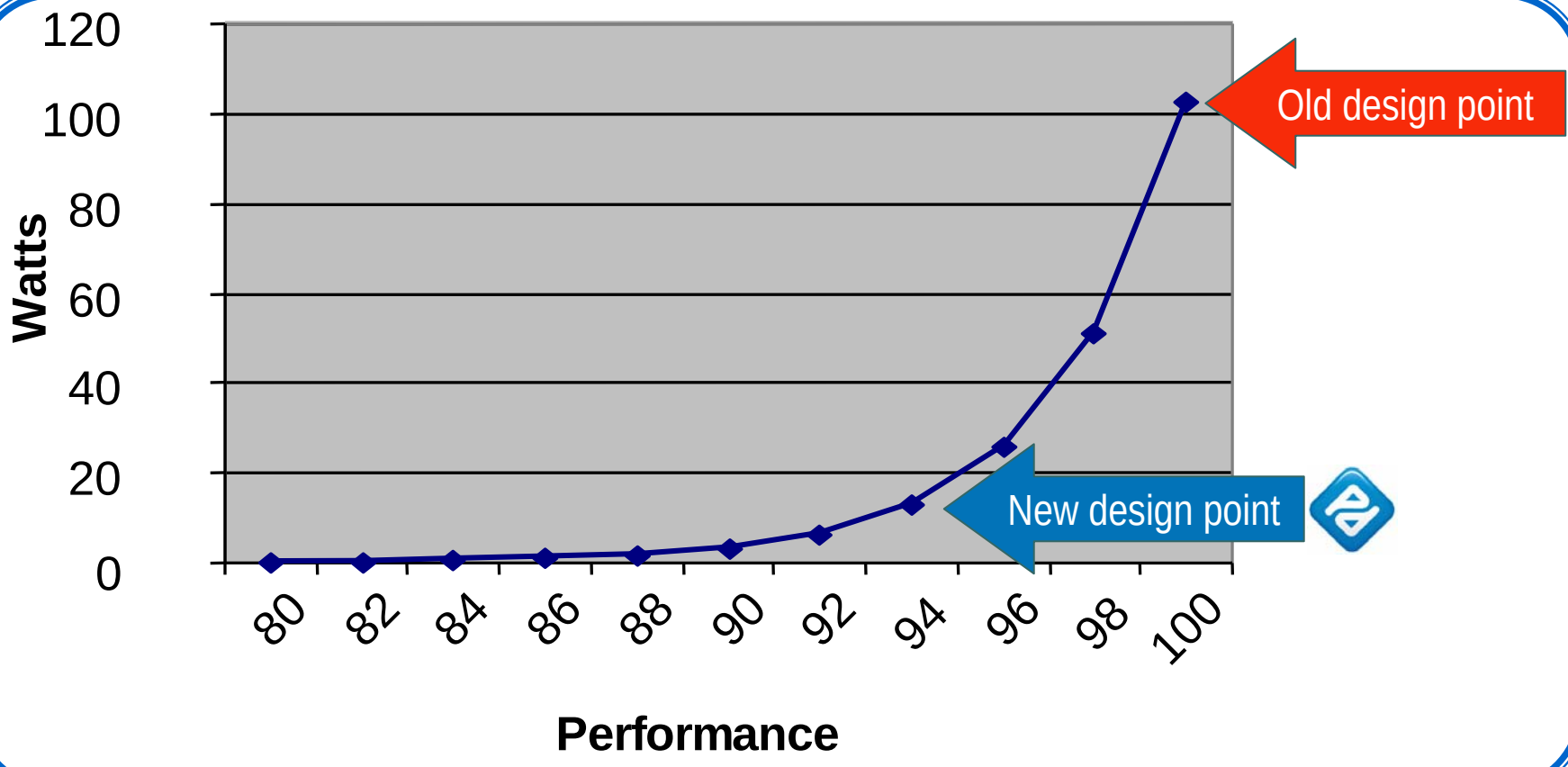
- Shrinking device geometries provides
  - Faster gates
  - Increased density

BUT

- Moore's Law means more power

EXCESSIVE POWER DISSIPATION LIMITS USABLE GATE CAPACITY

Choosing Power Over Ultimate Performance

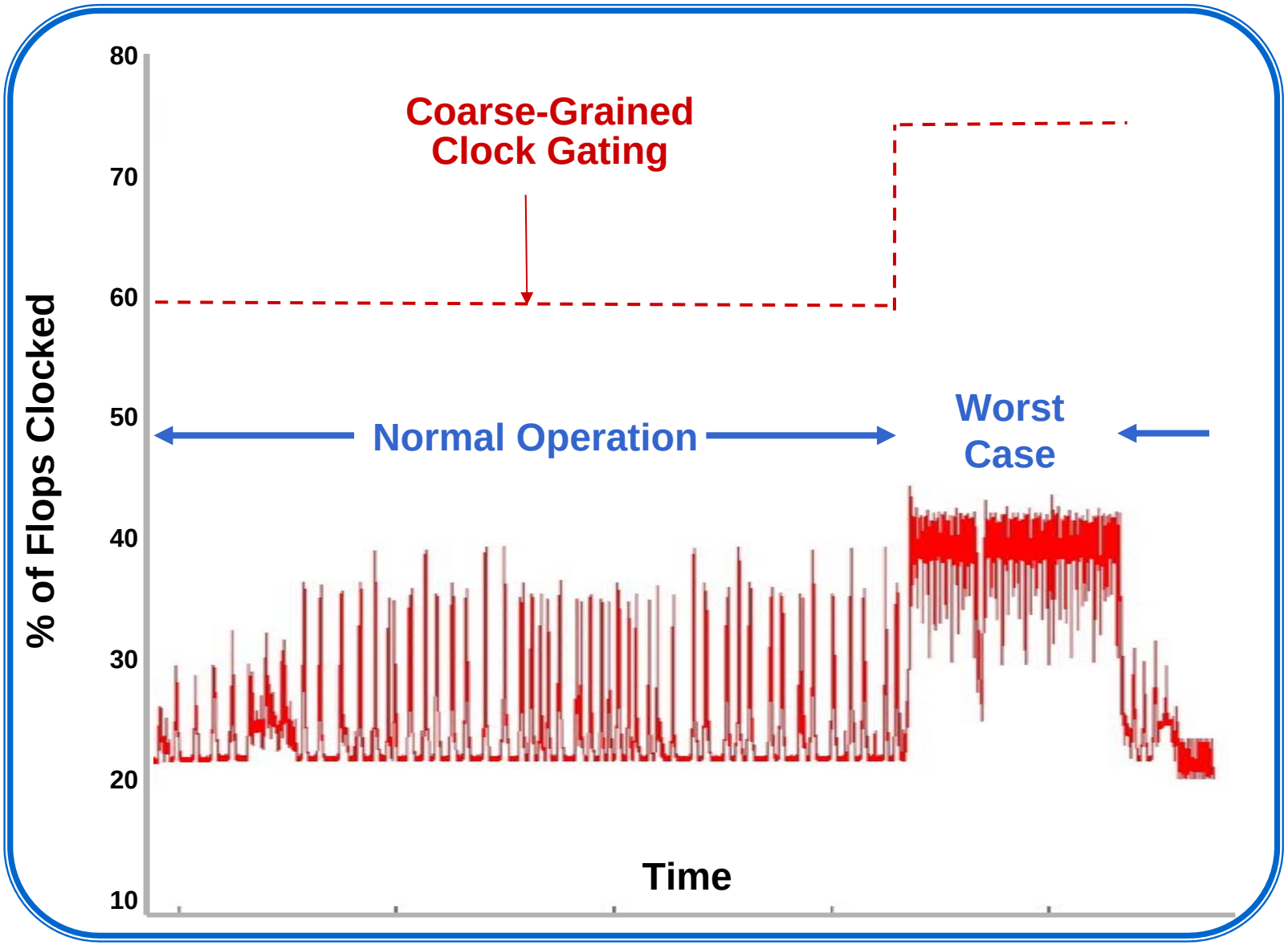


- Look for the exponential opportunities in power/performance
- Give up some performance for substantial power decrease

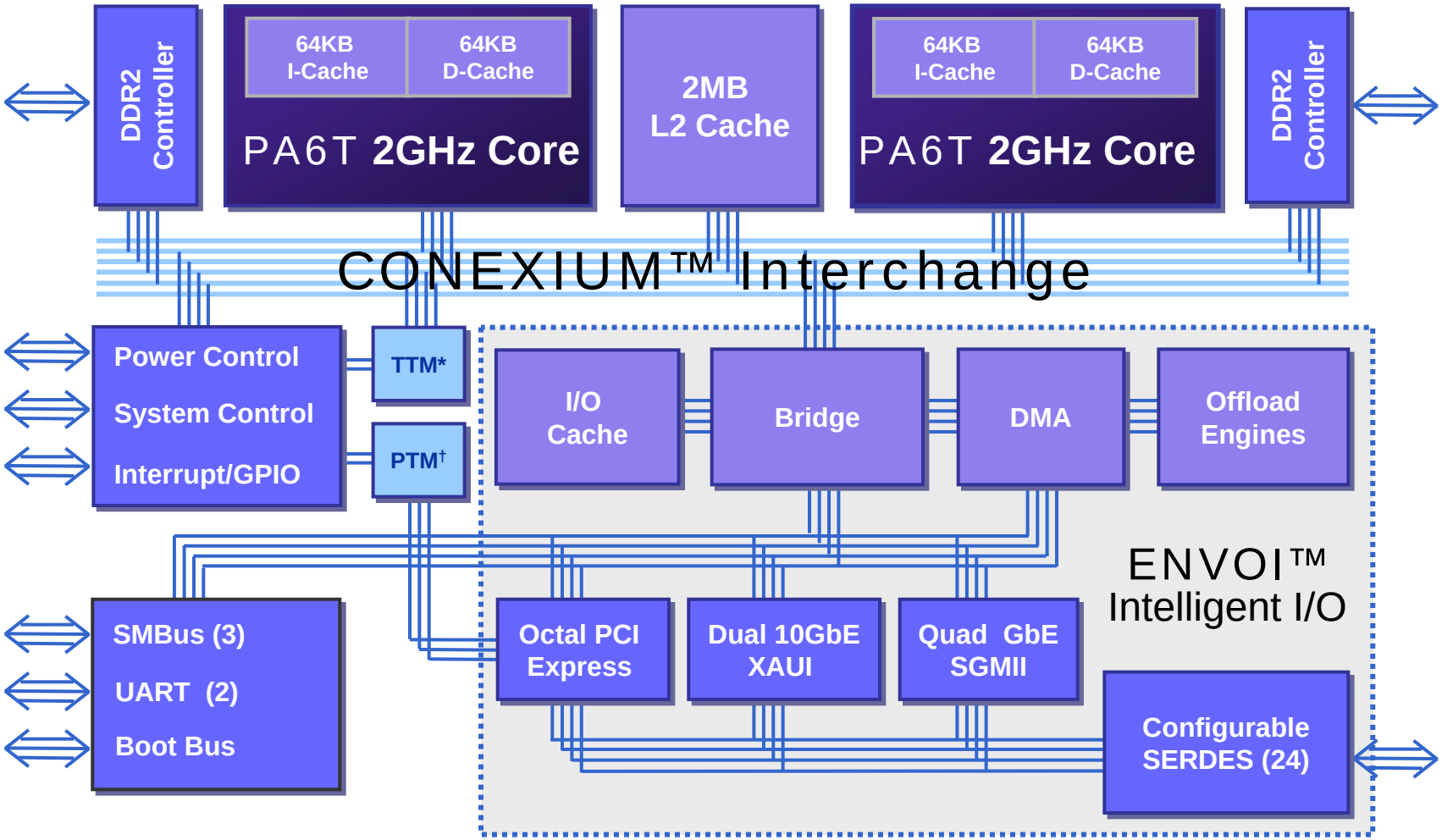
Design Choices for Low Power

- Design choices at several levels favor low power
  - CMOS process target
  - Circuit design style and sizing
  - Micro-architecture features
- Integration
  - Saves interface power
- Management
  - Voltage/frequency scaling
  - Multiple power planes for optimal voltage selection per region
  - Clock gating to reduce power of idle circuits
  - Active and pre-charge standby modes in DRAM array
  - PCIe power saving modes
  - Nap and Sleep modes for CPU

Fine-Grained Clock Gating Reduces Dynamic Power

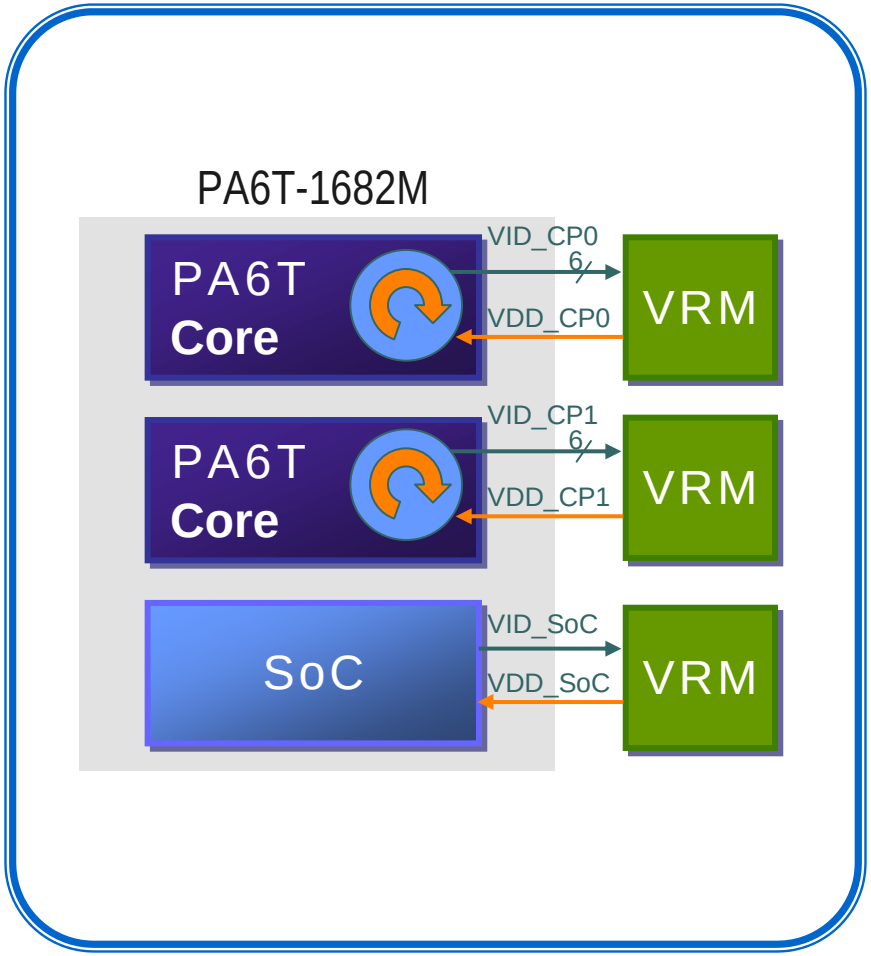


PWRficient PA6T-1682M Block Diagram



*Transaction trace memory †Peripheral trace memory

Voltage/Frequency Scaling



- Multiple power planes for maximum control
  - VID regulators for cores, SoC
- Ability to scale both Vdd and frequency on demand results in highly optimized total power

	Max Freq	Typ	Max
PA6T-1682M-FCN	2.0GHz	17W	25W
PA6T-1682M-FCG	1.5GHz	8W	15W
PA6T-1682M-FCD	1.0GHz	6W	10W
I/O coherent nap			2W*

*PA6T-1682M-FCN nap power may be higher

Summary – The Green Computing Advantage

- PWRficient processors set the bar for ultimate energy conservation at full performance
  - Lowest total energy for a computation or transaction
- PWRficient processors are designed to reduce system power
  - Optional use of power standby mode in DDR2 memories
- Only minimal performance compromises to meet power-efficiency goals
- Significant operating-cost savings for cluster-based computing
- Power conservation a key initiative from architectural concept though design