Announcing PWRficient Processors from PA Semi, the most power-efficient, high-performance processors available

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Overview

PA Semi has as it's mission to provide the embedded computing marketplace with the highest performing, lowest possible power processor available. The initial product, the PA6T-1682M delivers a 300-400% performance per watt advantage over any other high performance general purpose processor available.

This poster session will address:

- Use of fine grain clock gating to manage power on a highly granular basis.
- Innovative circuit design techniques that help minimize power while delivering high performance.
- Variable voltage and dynamic frequency shifting techniques which help insure minimal power use during operation.

Background

PA Semi processors are based on the POWER Architecture and conform to version 2.04 of that architecture.

The PWRficient PA6T-1682M combines two high performance 64-bit Power Architecture CPUs with a system controller and high bandwidth I/O system to give the central building block for high performance mobile and embedded computer systems. Single and dual CPU versions are available with additional multi-core devices planned.

Each processor core also includes VMX, a high performance vector processing engine which is code compatible with AltiVec.

Dynamic power management allows the part to consume a maximum of 25W when both CPUs are running at 2GHz with all interfaces active. Typical power consumption is between 5W and 13W depending on workload and I/O configuration.

Each CPU includes 64KB of L1 data cache and 64KB of L1 instruction cache. The part has a 2MB shared level 2 cache and two DDR-2 memory controllers.

Integrated I/O includes 24 serial lanes (SERDES) which may be flexibly allocated between up to 8 individual PCI Express links, up to 4 GbE interfaces and up to 2 Xaui interfaces.

A DMA engine is provided to move data to and from the interfaces and perform block moves. The source address may be either in memory or on the PCI-Express, as can the destination. Multiple channels allow several operations to run in parallel. Functions may be performed on the data as it is moved. Bulk encryption/decryption can be performed using AES, DES, triple-DES, ARC4 or Kasumi-f8. Signatures (hashes) can be calculated using the MD-5, SHA-1, SHA-256, Kasumi-f9 or generic CRC algorithms. Alternatively data blocks may be XORed to generate a parity stripe.

The system controller includes the power and CPU frequency management, watchdog and regular timers, an interrupt controller compatible with the OpenPIC standard, two UARTs, three SMBus channels and a debug controller. The local/boot bus supports LPC, CompactFlash (including TrueIDE mode), NAND flash and general multiplexed AD protocols and supports booting from LPC.

Development platforms

As part of the poster session PA Semi would like to display a demo system that will demonstrate the voltage and frequency scaling capabilities varying over workload with actual measured power displayed on a window while the demo runs.