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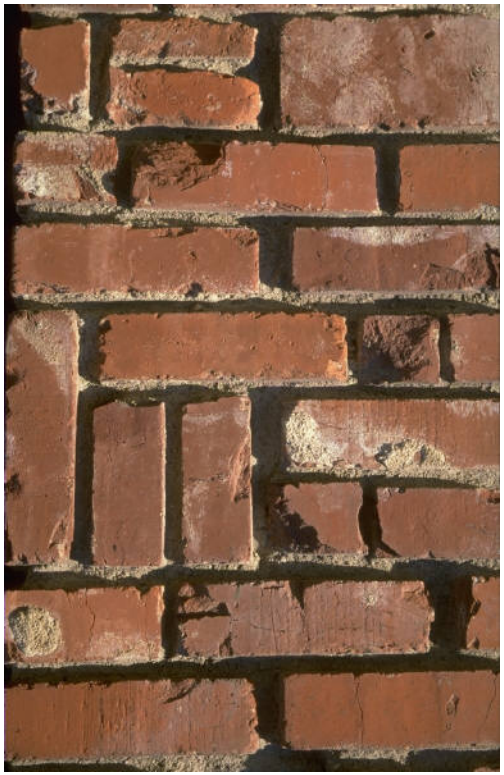
Introduction of Error Correcting Schemes in the Design Process of Self-Healing Circuits for Nanoscale Fabrics

Why nanoelectronics?

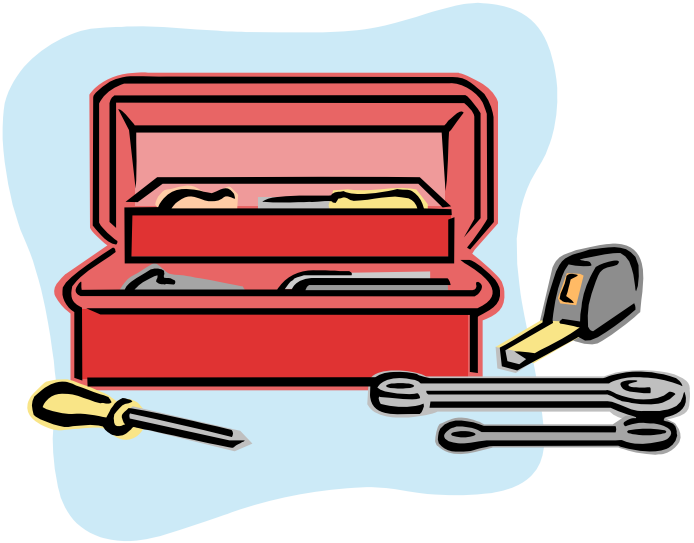
- CMOS is rapidly approaching the “red brick wall”
- We want to continue scaling power/MIPS down, price down, and performance up
- Nanoelectronics promises to allow this



Defects and Design

- Nanoelectronics uses bottom-up manufacturing processes which are expected to produce many defects
- Thus, we need defect tolerance in designs
- Also, bottom-up manufacturing is limited in the topologies it can produce, making design more complicated

The Need for Tools



- In order to design and evaluate systems using these next-generation technologies, we need CAD tools which can handle them
- Must also integrate support for defect tolerance techniques

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- Prototyping CAD tool, originally for FPGA
- Input logic using a high-level language
- Support for NASIC, a nanowire crossbar circuit design
- Support for fault-tolerance techniques on NASIC